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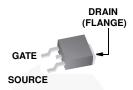


Data Sheet October 2013

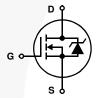
N-Channel Logic Level UltraFET Power MOSFET 100 V, 10 A, 165 $m\Omega$

Packaging

JEDEC TO-252AA



Symbol



Features

- · Ultra Low On-Resistance
 - $r_{DS(ON)} = 0.160\Omega$, $V_{GS} = 10V$
 - $r_{DS(ON)} = 0.165\Omega, V_{GS} = 5V$
- · Simulation Models
 - Temperature Compensated PSPICE® and SABER™ Electrical Models
 - Spice and SABER Thermal Impedance Models
 - www.Fairchildsemi.com
- · Peak Current vs Pulse Width Curve
- UIS Rating Curve
- Switching Time vs R_{GS} Curves

Ordering Information

PART NUMBER	PACKAGE	BRAND
HUF76609D3ST	TO-252AA	76609D

Absolute Maximum Ratings $T_C = 25^{\circ}C$, Unless Otherwise Specified

	HUF76609D3ST	UNITS
Drain to Source Voltage (Note 1)	100	V
Drain to Gate Voltage ($R_{GS} = 20k\Omega$) (Note 1)	100	V
Gate to Source Voltage	±16	V
Drain Current		
Continuous ($T_C = 25^{\circ}C$, $V_{GS} = 5V$)	10	Α
Continuous (T _C = 25 ^o C, V _{GS} = 10V) (Figure 2)	10	Α
Continuous ($T_C = 100^{\circ}$ C, $V_{GS} = 5$ V)	7	Α
Continuous ($T_C = 100^{\circ}$ C, $V_{GS} = 4.5$ V) (Figure 2)	7	Α
Pulsed Drain Current	Figure 4	
Pulsed Avalanche Rating UIS	Figures 6, 17, 18	
Power Dissipation	49	W
Derate Above 25°C	0.327	W/ ^o C
Operating and StorageTemperature	-55 to 175	°C
Maximum Temperature for Soldering		
Leads at 0.063in (1.6mm) from Case for 10s	300	°C
Package Body for 10s, See Techbrief TB334T _{pkq}	260	°C
NOTE:		

1. $T_J = 25^{\circ}C$ to $150^{\circ}C$.

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Product reliability information can be found at http://www.fairchildsemi.com/products/discrete/reliability/index.html For severe environments, see our Automotive HUFA series.

All Fairchild semiconductor products are manufactured, assembled and tested under ISO9000 and QS9000 quality systems certification.

HUF76609D3S

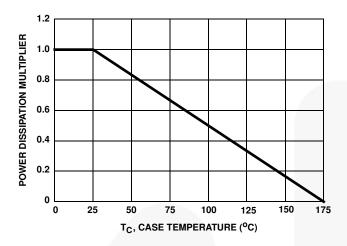
Electrical Specifications $T_C = 25^{\circ}C$, Unless Otherwise Specified

Description	PARAMETER	SYMBOL	TEST	CONDITIONS	MIN	TYP	MAX	UNITS
The Serial Resistance Junction to Case Rouch Rou	OFF STATE SPECIFICATIONS		+			+		
Vos = 95V, Vos = 90V Vos = 95V, Vos = 90V Vos = 90V Vos = 90V Vos = 90V, Vos	Drain to Source Breakdown Voltage	BV _{DSS}	$I_D = 250 \mu A, V_{GS} = 0$	V (Figure 12)	100	-	-	V
V _{DS} = 90V, V _{GS} = 0V, T _C = 150°C			$I_D = 250 \mu A, V_{GS} = 0$	V, T _C = -40 ^o C (Figure 12)	90	-	-	V
Gate to Source Leakage Current IGSS VGS = ±16V - - ±100 nA	Zero Gate Voltage Drain Current	I _{DSS}	$V_{DS} = 95V, V_{GS} = 0V$	l	-	-	1	μΑ
ON STATE SPECIFICATIONS Gate to Source Threshold Voltage V _{GS} (TH) V _{GS} = V _{DS} , I _D = 250µA (Figure 91) 1 - 3 V Drain to Source On Resistance I _D = 10A, V _{GS} = 10V (Figure 9, 10) - 0.130 0.160 Ω I _D = 7A, V _{GS} = 5V (Figure 9) - 0.135 0.165 Ω THERMAL SPECIFICATIONS Thermal Resistance Junction to Case R _{BUC} TO-252 - - 0.130 0.160 Ω Thermal Resistance Junction to Ambient R _{BUA} TO-252 - - 0.306 °C/W Turn-On Time I _O N V _D D = 50V, I _D = 7A V _D D = 50V, I _D = 7A - - 0.7 ns Turn-Off Delay Time I _I (ON) I _I (GFF) - - 10 - ns Turn-Off Time I _I (OFF) I _I - - - - - - - - - - - - - - - - - - <			$V_{DS} = 90V, V_{GS} = 0V$	/, T _C = 150 ^o C	-	-	250	μΑ
Case to Source Threshold Voltage VGS(TH) VGS = VDS, ID = 250μA (Figure 11) 1 - 3 V	Gate to Source Leakage Current	I _{GSS}	$V_{GS} = \pm 16V$		-	-	±100	nA
Drain to Source On Resistance Interpretation Inte	ON STATE SPECIFICATIONS							1
Date	Gate to Source Threshold Voltage	V _{GS(TH)}	$V_{GS} = V_{DS}, I_D = 250$	μA (Figure 11)	1	-	3	V
THERMAL SPECIFICATIONS	Drain to Source On Resistance		I _D = 10A, V _{GS} = 10V	(Figures 9, 10)	-	0.130	0.160	Ω
Thermal Resistance Junction to Case ReJC TO-252 3.06 °C/W		, ,	I _D = 7A, V _{GS} = 5V (F	igure 9)	-	0.135	0.165	Ω
Thermal Resistance Junction to Case R _{BUC} TO-252 TO-252					-	0.140	0.168	Ω
Thermal Resistance Junction to Ambient RaµA	THERMAL SPECIFICATIONS					-		
Thermal Resistance Junction to Ambient ReJA Ambient Ambi	Thermal Resistance Junction to Case	$R_{\theta JC}$	TO-252		-	-	3.06	oC/W
Turn-On Time	Thermal Resistance Junction to Ambient				-	-	100	°C/W
Turn-On Delay Time	SWITCHING SPECIFICATIONS (VGS =	= 4.5V)						1
Figures 15, 21, 22 - 10 - 18 18 18 19 19 19 19 19	Turn-On Time	ton			-	-	77	ns
Fise Time tr tr tr tr tr tr tr t	Turn-On Delay Time	t _d (ON)	$V_{GS} = 4.5V$, $R_{GS} = 20\Omega$		-	10	-	ns
Fall Time ty	Rise Time				-	41	-	ns
Fall Time t t	Turn-Off Delay Time	t _{d(OFF)}			-	30	-	ns
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Fall Time				-	28	-	ns
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Turn-Off Time	t _{OFF}			-	-	87	ns
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	SWITCHING SPECIFICATIONS (VGS	= 10V)						1
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Turn-On Time	ton			-	-	36	ns
Rise Time	Turn-On Delay Time		$R_{GS} = 24\Omega$		-	6	-	ns
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Rise Time				-	18	-	ns
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Turn-Off Delay Time	t _{d(OFF)}		(· · · · · · · · · · · · · · · · · · ·		55	-	ns
Total Gate Charge $Q_g(TOT)$ $V_{GS} = 0V$ to $10V$ $V_{DD} = 50V$, $V_{DD} = 50V$, $V_{DD} = 50V$, $V_{DD} = 7A$, $V_{DD} = $	Fall Time				-	39	-	ns
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Turn-Off Time	toff			/ -	-	141	ns
Gate Charge at 5V $Q_{g(5)} V_{GS} = 0V \text{ to } 5V$ Threshold Gate Charge $Q_{g(TH)} V_{GS} = 0V \text{ to } 1V$ Gate to Source Gate Charge $Q_{gS} Q_{gG} Q_{gG$	GATE CHARGE SPECIFICATIONS							1
Gate Charge at 5V $Q_{g(5)} V_{GS} = 0V \text{ to } 5V$ Threshold Gate Charge $Q_{g(TH)} V_{GS} = 0V \text{ to } 1V$ Gate to Source Gate Charge $Q_{gS} - 0.5 0.6 nC$ Gate to Drain "Miller" Charge $Q_{gd} - 1.4 - nC$ $CAPACITANCE SPECIFICATIONS$ Input Capacitance $C_{ISS} V_{DS} = 25V, V_{GS} = 0V, find the sum of $	Total Gate Charge	Q _{g(TOT)}	V _{GS} = 0V to 10V		-	13	16	nC
Threshold Gate Charge $Q_{g(TH)}$ $V_{GS} = 0V$ to $1V$ $(Figures 14, 19, 20)$ $ 0.5$ 0.6 nC $ 1.4$ $ nC$ $ -$	Gate Charge at 5V		$V_{GS} = 0V \text{ to } 5V$ $I_{D} = 7A,$ $I_{g(REF)} = 1.0\text{mA}$	-	7.3	8.8	nC	
Gate to Source Gate Charge Q_{gs} $-$ 1.4 - nC Gate to Drain "Miller" Charge Q_{gd} $-$ 3.4 - nC CAPACITANCE SPECIFICATIONS Input Capacitance C_{ISS} $V_{DS} = 25V$, $V_{GS} = 0V$, $-$ 425 - pF Output Capacitance C_{OSS} $f = 1MHz$ (Figure 13)	Threshold Gate Charge			-	0.5	0.6	nC	
Gate to Drain "Miller" Charge Q_{gd} - 3.4 - nC CAPACITANCE SPECIFICATIONS Input Capacitance C_{ISS} $V_{DS} = 25V$, $V_{GS} = 0V$, F_{ISS}	Gate to Source Gate Charge		(i iguies 14, 19, 20)		-	1.4	-	nC
	Gate to Drain "Miller" Charge				-	3.4	-	nC
Output Capacitance Coss f = 1MHz - 75 - pF	CAPACITANCE SPECIFICATIONS		1		1			
Output Capacitance Coss f = 1MHz - 75 - pF	Input Capacitance	C _{ISS}	V _{DS} = 25V, V _{GS} = 0V	Ι,	-	425	-	pF
(Tigure 13)	Output Capacitance		f = 1MHz		-	75	-	pF
	Reverse Transfer Capacitance				-	22	.	pF

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	V_{SD}	I _{SD} = 7A	-	-	1.25	V
		I _{SD} = 4A	-	-	1.0	V
Reverse Recovery Time	t _{rr}	$I_{SD} = 7A$, $dI_{SD}/dt = 100A/\mu s$	-	-	92	ns
Reverse Recovered Charge	Q _{RR}	$I_{SD} = 7A$, $dI_{SD}/dt = 100A/\mu s$	-	ı	273	nC

Typical Performance Curves



12 ID, DRAIN CURRENT (A) 9 $V_{GS} = 10V$ $V_{GS} = 4.5V$ 6 3 0 25 50 75 100 125 150 175 T_C, CASE TEMPERATURE (°C)

FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

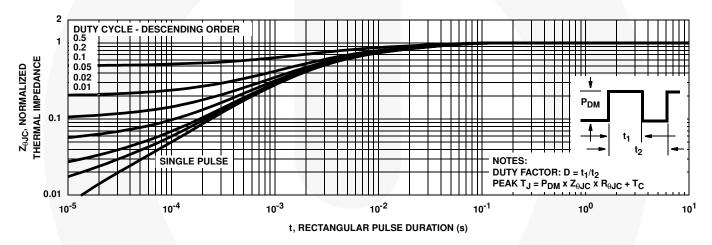


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

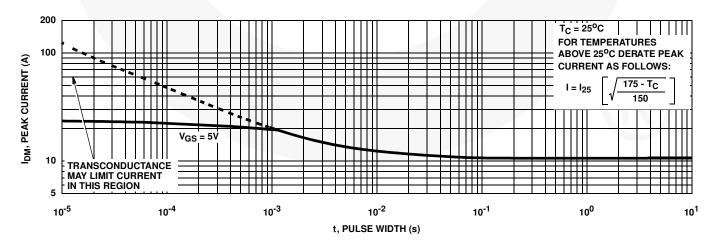


FIGURE 4. PEAK CURRENT CAPABILITY

Typical Performance Curves (Continued)

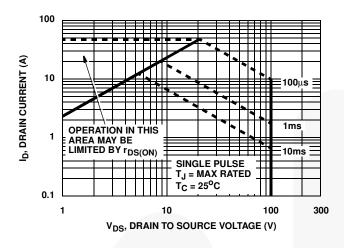


FIGURE 5. FORWARD BIAS SAFE OPERATING AREA

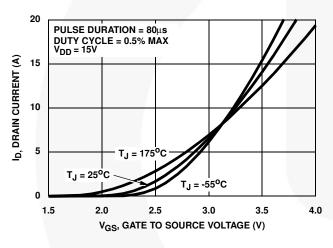


FIGURE 7. TRANSFER CHARACTERISTICS

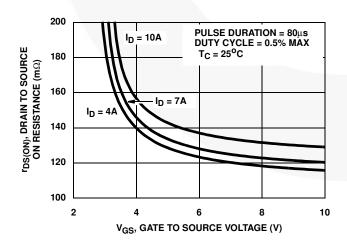
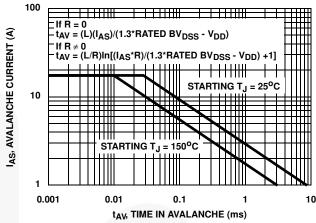


FIGURE 9. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT



NOTE: Refer to Fairchild Application Notes AN9321 and AN9322.

FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

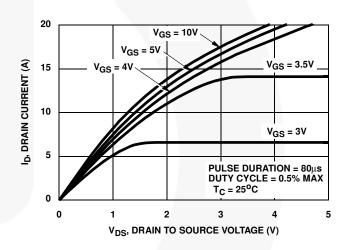


FIGURE 8. SATURATION CHARACTERISTICS

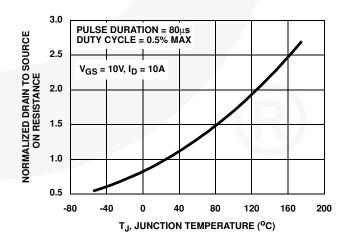


FIGURE 10. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

Typical Performance Curves (Continued)

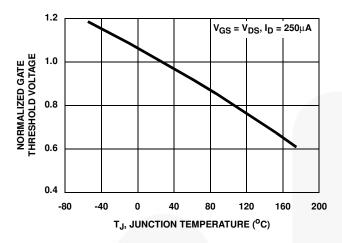


FIGURE 11. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

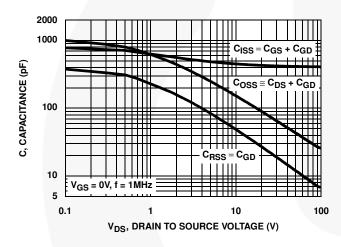


FIGURE 13. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

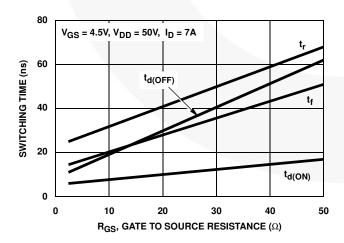


FIGURE 15. SWITCHING TIME vs GATE RESISTANCE

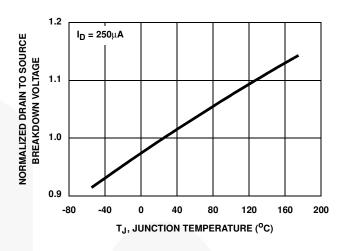
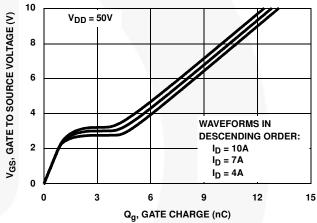


FIGURE 12. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE VS JUNCTION TEMPERATURE



NOTE: Refer to Fairchild Application Notes AN7254 and AN7260.

FIGURE 14. GATE CHARGE WAVEFORMS FOR CONSTANT GATE CURRENT

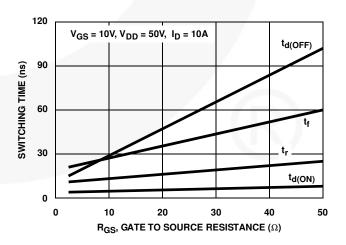


FIGURE 16. SWITCHING TIME vs GATE RESISTANCE

Test Circuits and Waveforms

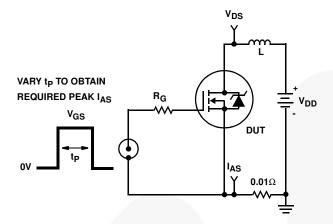


FIGURE 17. UNCLAMPED ENERGY TEST CIRCUIT

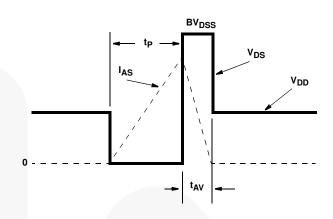


FIGURE 18. UNCLAMPED ENERGY WAVEFORMS

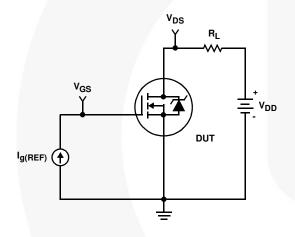


FIGURE 19. GATE CHARGE TEST CIRCUIT

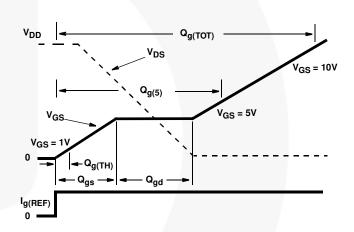


FIGURE 20. GATE CHARGE WAVEFORMS

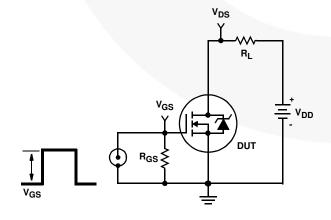


FIGURE 21. SWITCHING TIME TEST CIRCUIT

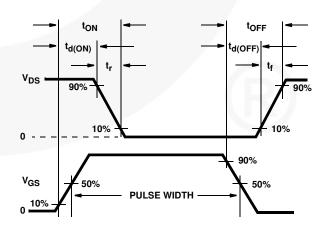


FIGURE 22. SWITCHING TIME WAVEFORM

PSPICE Electrical Model

.SUBCKT HUF76609D3 2 1 3; rev 23 August 1999

CA 12 8 7.5e-10 CB 15 14 7.6e-10 CIN 6 8 4.03e-10 LDRAIN DPLCAP DRAIN -02 DBODY 7 5 DBODYMOD 10 DBREAK 5 11 DBREAKMOD **RLDRAIN** RSLC1 **DPLCAP 10 5 DPLCAPMOD** DBREAK T 51 RSLC₂ EBREAK 11 7 17 18 116.7 **ESLC** 11 EDS 14 8 5 8 1 EGS 13 8 6 8 1 ່ 50 ESG 6 10 6 8 1 DBODY RDRAIN EVTHRES 6 21 19 8 1 <u>6</u> 8 **EBREAK ESG** EVTEMP 20 6 18 22 1 **EVTHRES** 16 19 8 **MWEAK EVTEME** I GATE IT 8 17 1 RGATE GATE MMED LDRAIN 2 5 1e-9 9 20 **←**MSTRO LGATE 1 9 3.7e-9 RLGATE LSOURCE 3 7 3.4e-9 **LSOURCE** CIN SOURCE 8 MMED 16 6 8 8 MMEDMOD MSTRO 16 6 8 8 MSTROMOD **RSOURCE** RLSOURCE MWEAK 16 21 8 8 MWEAKMOD S₁A S24 **RBREAK** 12 F RBREAK 17 18 RBREAKMOD 1 <u>13</u> 8 <u>14</u> 13 15 17 18 RDRAIN 50 16 RDRAINMOD 9.4e-2 RGATE 9 20 3.3 **RVTEMP** RLDRAIN 2 5 10 S₁B S2B RLGATE 1 9 37 CB 19 CA IT RLSOURCE 3 7 34 RSLC1 5 51 RSLCMOD 1e-6 **VBAT** 8 <u>5</u> RSLC2 5 50 1e3 EGS **EDS** RSOURCE 8 7 RSOURCEMOD 1.3e-2 8 RVTHRES 22 8 RVTHRESMOD 1 22 **RVTEMP 18 19 RVTEMPMOD 1 RVTHRES** S1A 6 12 13 8 S1AMOD S1B 13 12 13 8 S1BMOD S2A 6 15 14 13 S2AMOD S2B 13 15 14 13 S2BMOD VBAT 22 19 DC 1 ESLC 51 50 VALUE={(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)/(1e-6*17.3),3.5))} .MODEL DBODYMOD D (IS = 1.2e-12 RS = 1.2e-2 TRS1 = 1.2e-3 TRS2 = 1.03e-6 CJO = 6.7e-10 TT = 6.9e-8 M = 0.77) .MODEL DBREAKMOD D (RS = 9.9e- 1TRS1 = 1e- 3TRS2 = -2e-5) .MODEL DPLCAPMOD D (CJO = 4.3e-1 0IS = 1e-3 0M = 0.9 N = 10) MODEL MMEDMOD NMOS (VTO = 1.88 KP = 5 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 3.3) .MODEL MSTROMOD NMOS (VTO = 2.13 KP = 12.4 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u) MODEL MWEAKMOD NMOS (VTO = 1.59 KP = 0.12 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 33 RS = 0.1) MODEL RBREAKMOD RES (TC1 = 1.05e- 3TC2 = -5e-7) .MODEL RDRAINMOD RES (TC1 = 8.1e-3 TC2 = 2.4e-5) .MODEL RSLCMOD RES (TC1 = 3e-3 TC2 = 2e-6) MODEL RSOURCEMOD RES (TC1 = 1e-3 TC2 = 1e-6)

MODEL RVTHRESMOD RES (TC1 = -1.5e-3 TC2 = -4.3e-6) .MODEL RVTEMPMOD RES (TC1 = -1.6e- 3TC2 = 1.5e-6) .MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -4.5 VOFF= -2.5) MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -2.5 VOFF= -4.5) .MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -0.3 VOFF= 0.2) .MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 0.2 VOFF= -0.3)

NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.

.ENDS

SABER Electrical Model

```
REV 23 August 1999
template huf76609d3 n2,n1,n3
electrical n2,n1,n3
var i iscl
d..model dbodymod = (is = 1.2e-12, n = 1.05, cjo = 6.7e-10, tt = 6.9e-8, m = 0.77)
d..model dbreakmod = ()
d..model dplcapmod = (cio = 4.3e-10, is = 1e-30, n = 10, m = 0.9)
m..model mmedmod = (type=_n, vto = 1.88, kp = 5, is = 1e-30, tox = 1)
m..model mstrongmod = (type=_n, vto = 2.13, kp = 12.4, is = 1e-30, tox = 1)
m..model mweakmod = (type=_n, vto = 1.59, kp = 0.12, is = 1e-30, tox = 1)
                                                                                                                                    LDRAIN
sw_vcsp..model s1amod = (ron = 1e-5, roff = 0.1, von = -4.5, voff = -2.5)
                                                                                    DPLCAP
                                                                                                                                               DRAIN
sw_vcsp..model s1bmod = (ron =1e-5, roff = 0.1, von = -2.5, voff = -4.5)
sw_vcsp..model s2amod = (ron = 1e-5, roff = 0.1, von = -0.3, voff = 0.2)
                                                                                10
                                                                                                                                   RLDRAIN
sw_vcsp..model s2bmod = (ron = 1e-5, roff = 0.1, von = 0.2, voff = -0.3)
                                                                                                 RSLC<sub>1</sub>
                                                                                                              RDBREAK
                                                                                                 51
c.ca n12 n8 = 7.5e-10
                                                                                  RSLC2 €
                                                                                                                       72
c.cb n15 n14 = 7.6e-10
                                                                                                                                   RDBODY
                                                                                                   ISCL
c.cin n6 n8 = 4.03e-10
                                                                                                               DBREAK _
d.dbody n7 n71 = model=dbodymod
                                                                                                 RDRAIN
d.dbreak n72 n11 = model=dbreakmod
                                                                              6
8
                                                                        ESG
                                                                                                                        11
d.dplcap n10 n5 = model=dplcapmod
                                                                                     EVTHRES
                                                                                                     16
                                                                                                 21
                                                                                        1<u>9</u>
                                                                                                                 MWEAK
i.it n8 n17 = 1
                                                    LGATE
                                                                      EVTEMP
                                                                                                                                   DBODY
                                                              RGATE
                                           GATE
                                                                                                                  EBREAK
I.ldrain n2 n5 = 1e-9
                                                                                                       MMED
                                                             9
                                                                     20
I.lgate n1 n9 = 3.7e-9
                                                                                             I<del><</del>_MSTR
                                                   RLGATE
I.Isource n3 n7 = 3.4e-9
                                                                                                                                   LSOURCE
                                                                                           CIN
                                                                                                                                              SOURCE
                                                                                                     8
m.mmed n16 n6 n8 n8 = model=mmedmod, l=1u, w=1u
m.mstrong n16 n6 n8 n8 = model=mstrongmod, l=1u, w=1u
                                                                                                                 RSOURCE
m.mweak n16 n21 n8 n8 = model=mweakmod, l=1u, w=1u
                                                                                                                                  RLSOURCE
                                                                                  S2A
res.rbreak n17 n18 = 1, tc1 = 1.05e-3, tc2 = -5e-7
                                                                                                                     RBREAK
res.rdbody n71 n5 = 1.2e-2, tc1 = 1.2e-3, tc2 = 1.03e-6
                                                                                                                 17
res.rdbreak n72 n5 = 9.9e-1, tc1 = 1e-3, tc2 = -2e-5
res.rdrain n50 n16 = 9.4e-2, tc1 = 8.1e-3, tc2 = 2.4e-5
                                                                                                                                 RVTEMP
                                                                                  o S2B
res.rgate n9 n20 = 3.3
                                                                                          CB
                                                                CA
res.rldrain n2 n5 = 10
                                                                                                               ΙT
res.rlgate n1 n9 = 37
                                                                                                                                   VBAT
res.rlsource n3 n7 = 34
                                                                          EGS
                                                                                       EDS
res.rslc1 n5 n51 = 1e-6, tc1 = 3e-3, tc2 = 2e-6
                                                                                                             8
res.rslc2 n5 n50 = 1e3
res.rsource n8 n7 = 1.3e-2, tc1 = 1e-3, tc2 = 1e-6
                                                                                                                     RVTHRES
res.rvtemp n18 n19 = 1, tc1 = -1.6e-3, tc2 = 1.5e-6
res.rvthres n22 n8 = 1, tc1 = -1.5e-3, tc2 = -4.3e-6
spe.ebreak n11 n7 n17 n18 = 116.7
spe.eds n14 n8 n5 n8 = 1
spe.eqs n13 n8 n6 n8 = 1
spe.esg n6 n10 n6 n8 = 1
spe.evtemp n20 n6 n18 n22 = 1
spe.evthres n6 n21 n19 n8 = 1
sw vcsp.s1a n6 n12 n13 n8 = model=s1amod
sw_vcsp.s1b n13 n12 n13 n8 = model=s1bmod
sw_vcsp.s2a n6 n15 n14 n13 = model=s2amod
sw vcsp.s2b n13 n15 n14 n13 = model=s2bmod
v.vbat n22 n19 = dc=1
equations {
i (n51->n50) +=iscl
iscl: v(n51,n50) = ((v(n5,n51)/(1e-9+abs(v(n5,n51))))*((abs(v(n5,n51)*1e6/17.3))** 3.5))
```

SPICE Thermal Model

T76609d3

CTHERM1 th 6 9.50e-4
CTHERM2 6 5 2.40e-3
CTHERM3 5 4 3.90e-3
CTHERM4 4 3 4.10e-3
CTHERM5 3 2 5.60e-3
CTHERM6 2 tl 4.00e-2

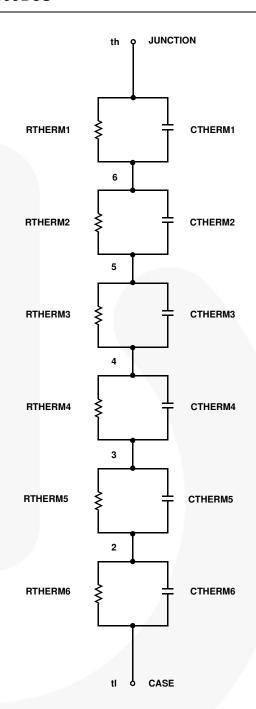
RTHERM1 th 6 2.00e-2
RTHERM2 6 5 1.10e-1
RTHERM3 5 4 2.75e-1
RTHERM4 4 3 5.53e-1
RTHERM5 3 2 7.25e-1
RTHERM5 2 tl 7.56e-1

REV 23 August 1999

SABER Thermal Model

SABER thermal model t76609d3

template thermal_model th tl thermal_c th, tl { ctherm.ctherm1 th 6 = 9.50e-4 ctherm.ctherm2 6 5 = 2.40e-3 ctherm.ctherm3 5 4 = 3.90e-3 ctherm.ctherm4 4 3 = 4.10e-3 ctherm.ctherm5 3 2 = 5.60e-3 ctherm.ctherm6 2 tl = 4.00e-2 rtherm.rtherm1 th 6 = 2.00e-2 rtherm.rtherm2 6 5 = 1.10e-1 rtherm.rtherm3 5 4 = 2.75e-1 rtherm.rtherm4 4 3 = 5.53e-1 rtherm.rtherm5 3 2 = 7.25e-1 rtherm.rtherm6 2 tl = 7.56e-1 }



HUF76609D3S



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