

NTD4959NH

Power MOSFET

30 V, 58 A, Single N-Channel, DPAK/IPAK

Features

- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Optimized Gate Charge to Minimize Switching Losses
- These are Pb-Free Devices

Applications

- CPU Power Delivery
- DC-DC Converters
- Low Side Switching

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit			
Drain-to-Source Voltage	V_{DS}	30	V			
Gate-to-Source Voltage	V_{GS}	± 20	V			
Continuous Drain Current ($R_{\theta JA}$) (Note 1)	$T_A = 25^\circ\text{C}$	I_D	11.5	A		
		I_D	9.0	A		
	$T_A = 25^\circ\text{C}$	P_D	2.0	W		
		P_D	1.3	W		
	Power Dissipation ($R_{\theta JA}$) (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	I_D	9.0	A
			$T_A = 85^\circ\text{C}$	I_D	7.0	A
Continuous Drain Current ($R_{\theta JA}$) (Note 2)	Steady State	$T_A = 25^\circ\text{C}$	P_D	1.3	W	
		$T_A = 85^\circ\text{C}$	P_D	0.8	W	
Power Dissipation ($R_{\theta JA}$) (Note 2)	Steady State	$T_A = 25^\circ\text{C}$	P_D	1.3	W	
		$T_A = 85^\circ\text{C}$	P_D	0.8	W	
Continuous Drain Current ($R_{\theta JC}$) (Note 1)	Steady State	$T_C = 25^\circ\text{C}$	I_D	58	A	
		$T_C = 85^\circ\text{C}$	I_D	45	A	
Power Dissipation ($R_{\theta JC}$) (Note 1)	Steady State	$T_C = 25^\circ\text{C}$	P_D	52	W	
		$T_C = 85^\circ\text{C}$	P_D	35	W	
Pulsed Drain Current	$t_p = 10\mu\text{s}$	$T_A = 25^\circ\text{C}$	I_{DM}	130	A	
Current Limited by Package		$T_A = 25^\circ\text{C}$	$I_{DmaxPkg}$	45	A	
Operating Junction and Storage Temperature	T_J, T_{stg}	-55 to 175		$^\circ\text{C}$		
Source Current (Body Diode)	I_S	43		A		
Drain to Source dV/dt	dV/dt	6.0		V/ns		
Single Pulse Drain-to-Source Avalanche Energy ($V_{DD} = 24\text{ V}, V_{GS} = 10\text{ V}, L = 1.0\text{ mH}, I_{L(pk)} = 15\text{ A}, R_G = 25\ \Omega$)	E_{AS}	112.5		mJ		
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	T_L	260		$^\circ\text{C}$		

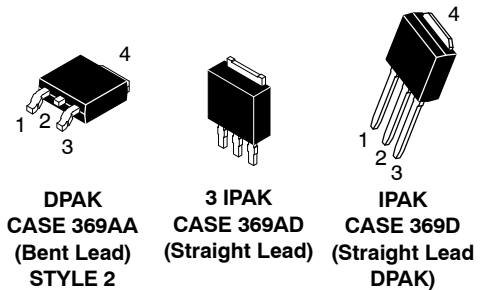
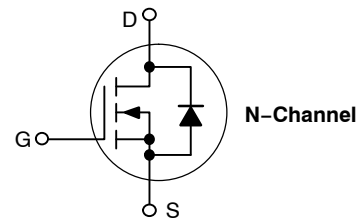
Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.



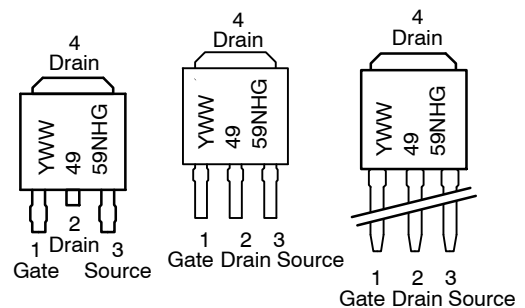
ON Semiconductor®

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$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	I_D MAX
30 V	9.0 m Ω @ 10 V	58 A
	12.5 m Ω @ 4.5 V	



MARKING DIAGRAMS & PIN ASSIGNMENTS



Y = Year
 WW = Work Week
 4959NH = Device Code
 G = Pb-Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

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THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case (Drain)	$R_{\theta JC}$	2.9	°C/W
Junction-to-TAB (Drain)	$R_{\theta JC-TAB}$	3.5	
Junction-to-Ambient - Steady State (Note 1)	$R_{\theta JA}$	74	
Junction-to-Ambient - Steady State (Note 2)	$R_{\theta JA}$	116	

- Surface-mounted on FR4 board using 1 in sq pad size, 1 oz Cu.
- Surface-mounted on FR4 board using the minimum recommended pad size.

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	30			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			25		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = 24\text{ V}$	$T_J = 25^\circ\text{C}$		1.0	μA
			$T_J = 125^\circ\text{C}$		10	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$	1.5	2.1	2.5	V	
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			5.7		mV/°C	
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ to }11.5\text{ V}$	$I_D = 30\text{ A}$		7.0	9.0	m Ω
			$I_D = 15\text{ A}$		7.0		
		$V_{GS} = 4.5\text{ V}$	$I_D = 30\text{ A}$		10.45	12.5	
			$I_D = 15\text{ A}$		9.95		
Forward Transconductance	g_{FS}	$V_{DS} = 15\text{ V}, I_D = 15\text{ A}$		9.0		S	

CHARGES AND CAPACITANCES

Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}, V_{DS} = 12\text{ V}$		1596	2155	pF
Output Capacitance	C_{oss}			331	447	
Reverse Transfer Capacitance	C_{rss}			190	294	
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 15\text{ V}, I_D = 30\text{ A}$		12.5	15	nC
Threshold Gate Charge	$Q_{G(TH)}$			2.4	3.6	
Gate-to-Source Charge	Q_{GS}			5.3	7.9	
Gate-to-Drain Charge	Q_{GD}			5.1	7.7	
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 11.5\text{ V}, V_{DS} = 15\text{ V}, I_D = 30\text{ A}$		29.3	44	nC

SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	$t_{d(on)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 15\text{ V}, I_D = 15\text{ A}, R_G = 3.0\ \Omega$		12.0	18	ns
Rise Time	t_r			20	30	
Turn-Off Delay Time	$t_{d(off)}$			14	21	
Fall Time	t_f			5.0	7.5	
Turn-On Delay Time	$t_{d(on)}$	$V_{GS} = 11.5\text{ V}, V_{DS} = 15\text{ V}, I_D = 15\text{ A}, R_G = 3.0\ \Omega$		7.0	10.4	ns
Rise Time	t_r			18	27	
Turn-Off Delay Time	$t_{d(off)}$			22	33	
Fall Time	t_f			3.0	4.6	

- Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.
- Switching characteristics are independent of operating junction temperatures.

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ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V _{SD}	V _{GS} = 0 V, I _S = 30 A	T _J = 25°C		0.95	1.2	V
			T _J = 125°C		0.83		
Reverse Recovery Time	t _{RR}	V _{GS} = 0 V, dI _S /dt = 100 A/μs, I _S = 30 A		15.6		ns	
Charge Time	t _a			10.6			
Discharge Time	t _b			5.0			
Reverse Recovery Time	Q _{RR}			7.5			nC

PACKAGE PARASITIC VALUES

Source Inductance	L _S	T _A = 25°C		2.49		nH
Drain Inductance, DPAK	L _D			0.0164		
Drain Inductance, IPAK	L _D			1.88		
Gate Inductance	L _G			3.46		
Gate Resistance	R _G			0.75		Ω

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TYPICAL PERFORMANCE CURVES

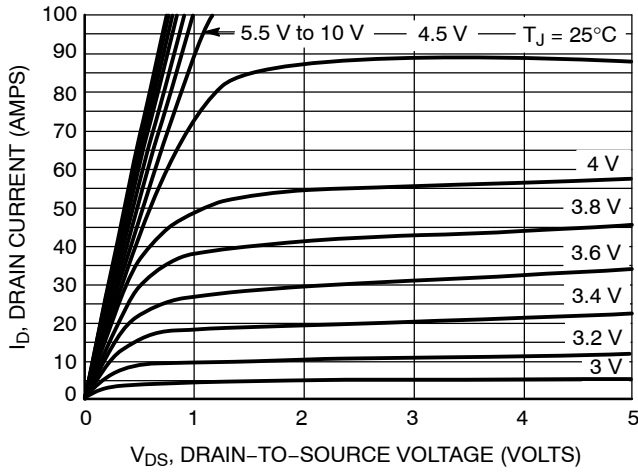


Figure 1. On-Region Characteristics

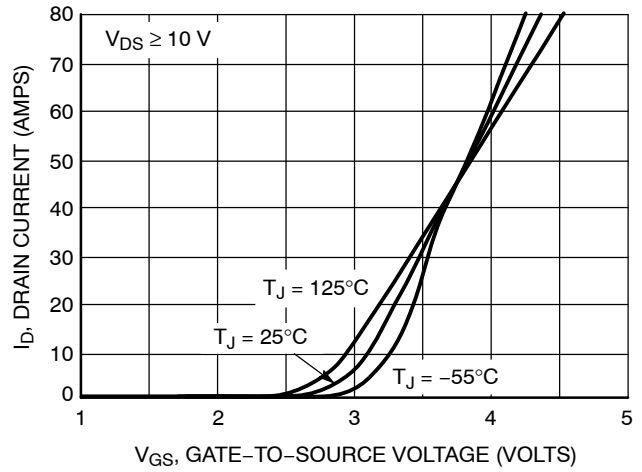


Figure 2. Transfer Characteristics

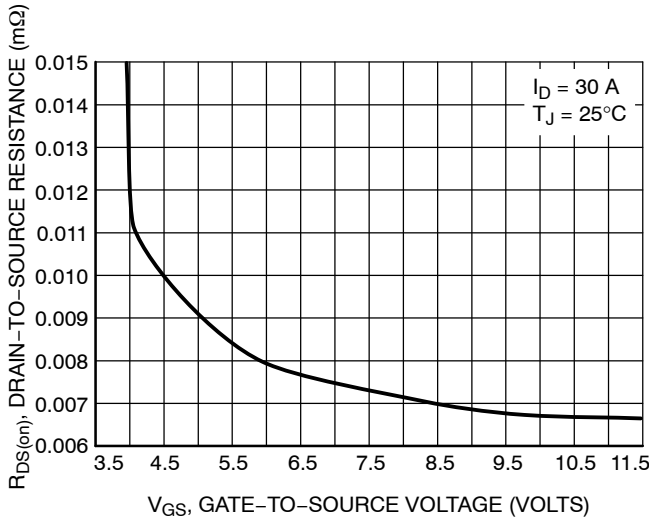


Figure 3. On-Resistance vs. Gate-to-Source Voltage

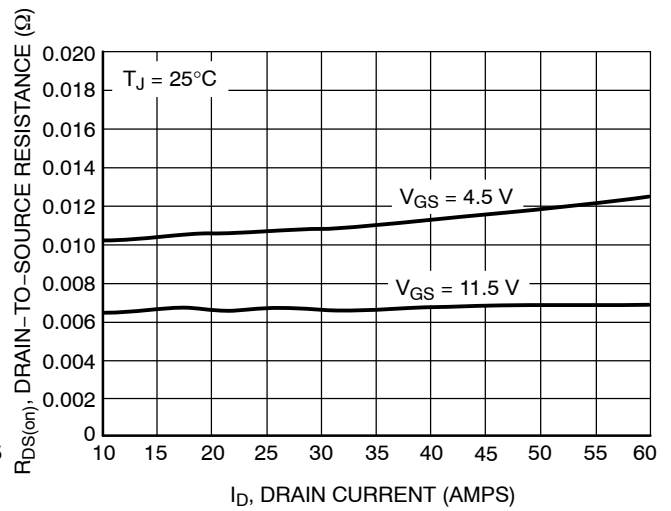


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

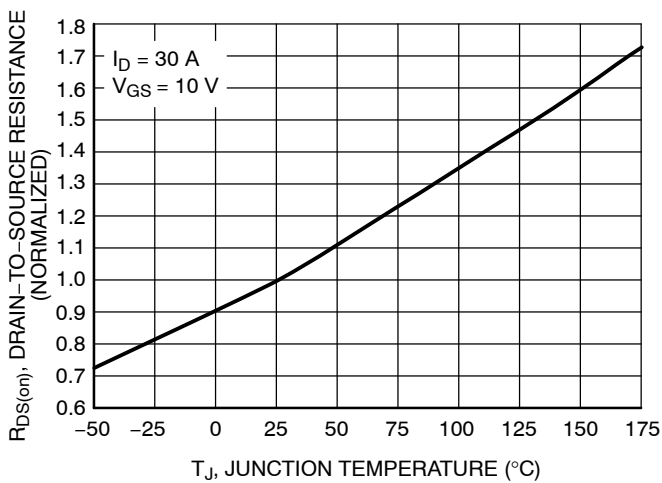


Figure 5. On-Resistance Variation with Temperature

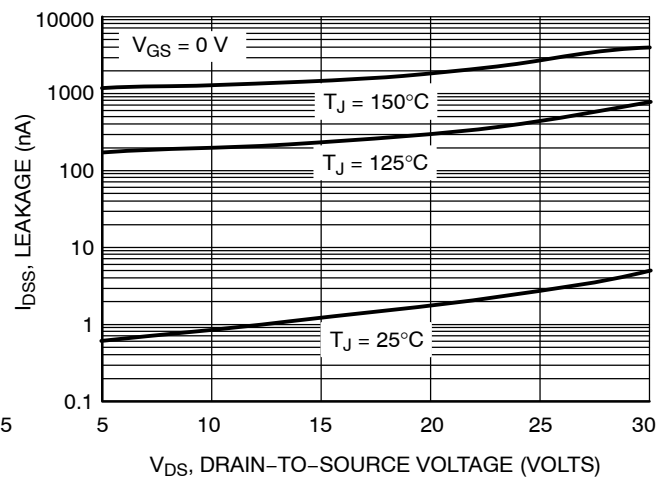


Figure 6. Drain-to-Source Leakage Current vs. Drain Voltage

TYPICAL PERFORMANCE CURVES

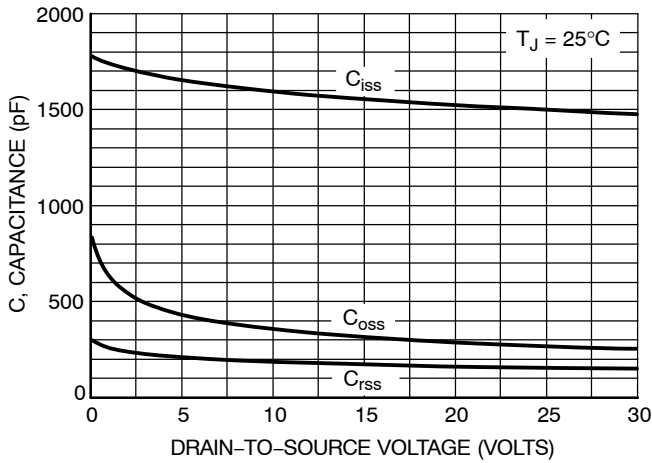


Figure 7. Capacitance Variation

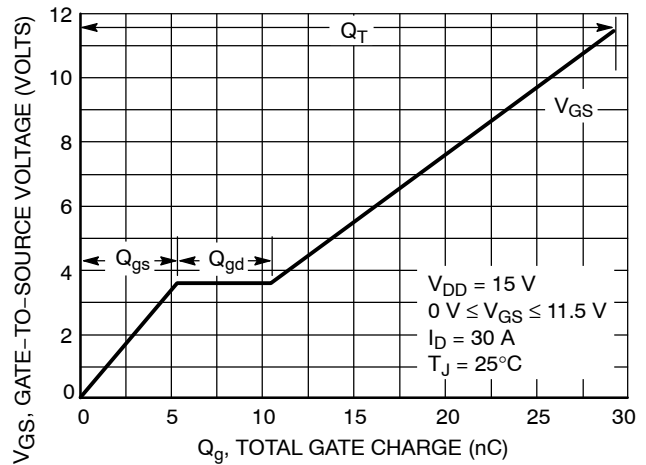


Figure 8. Gate-to-Source Voltage vs. Total Charge

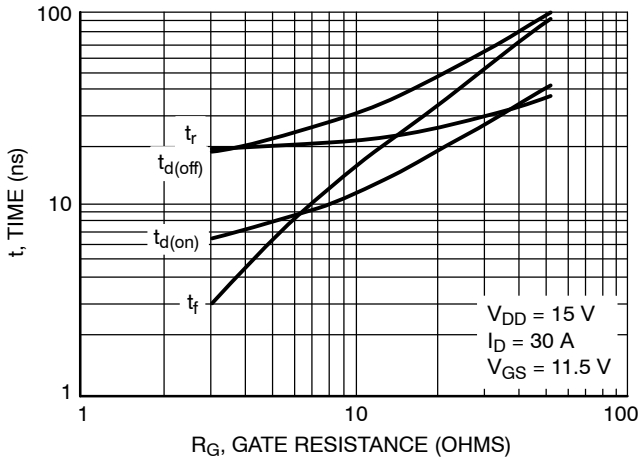


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

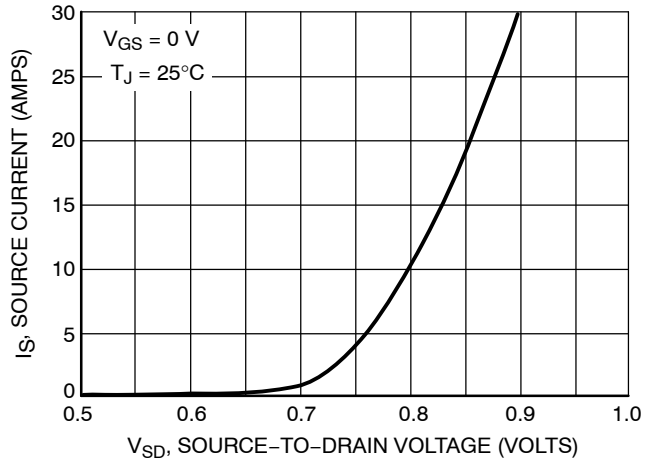


Figure 10. Diode Forward Voltage vs. Current

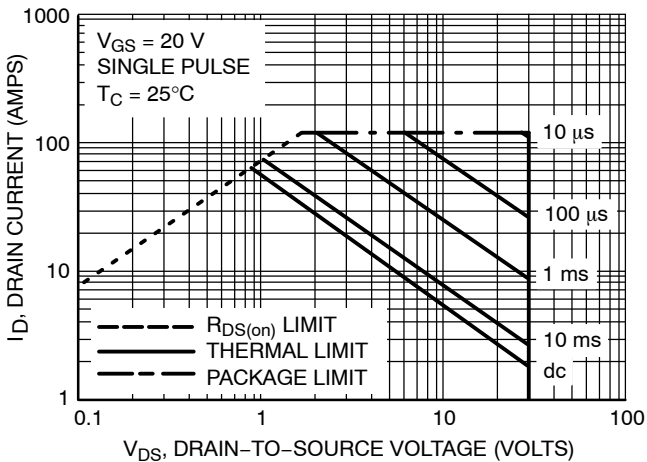


Figure 11. Maximum Rated Forward Biased Safe Operating Area

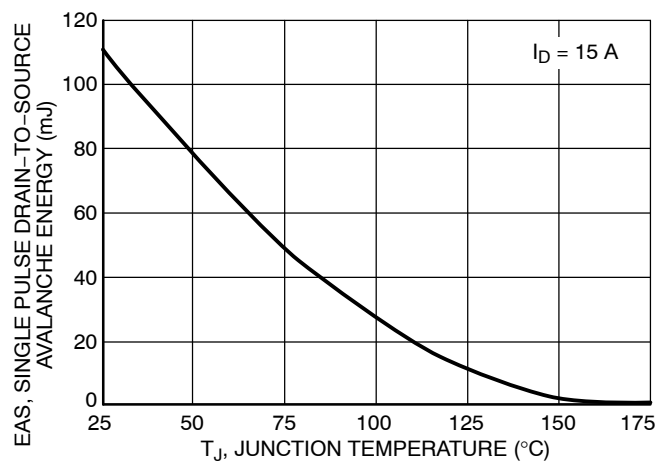


Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature

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TYPICAL PERFORMANCE CURVES

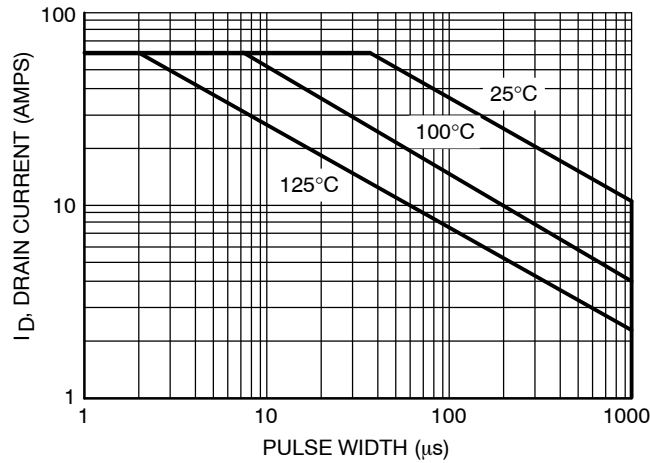


Figure 13. Avalanche Characteristics

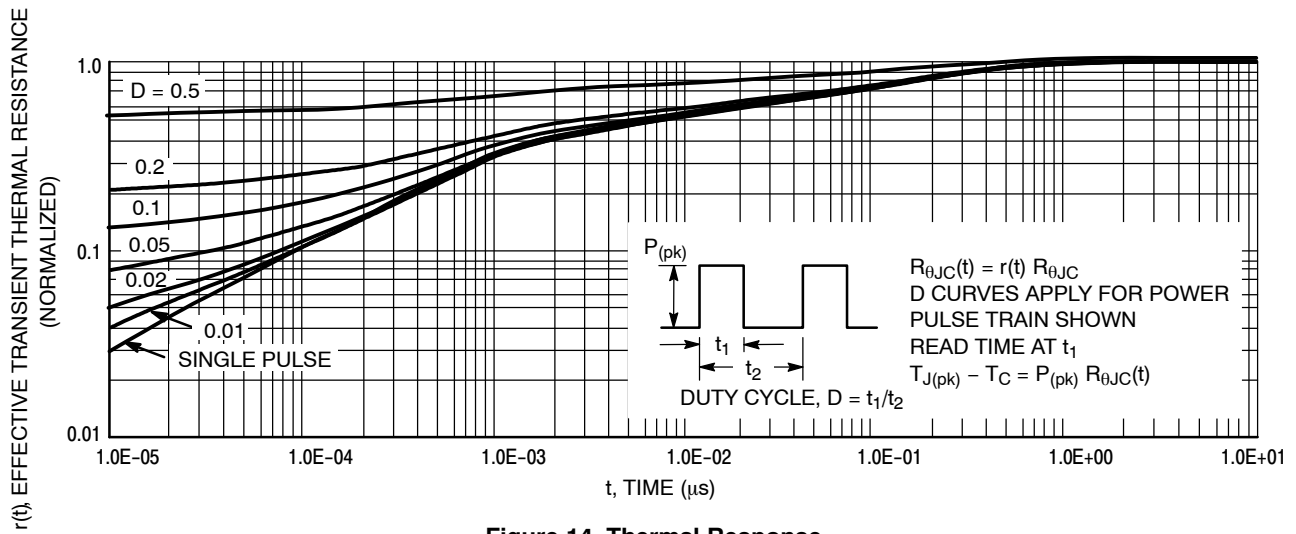


Figure 14. Thermal Response

ORDERING INFORMATION

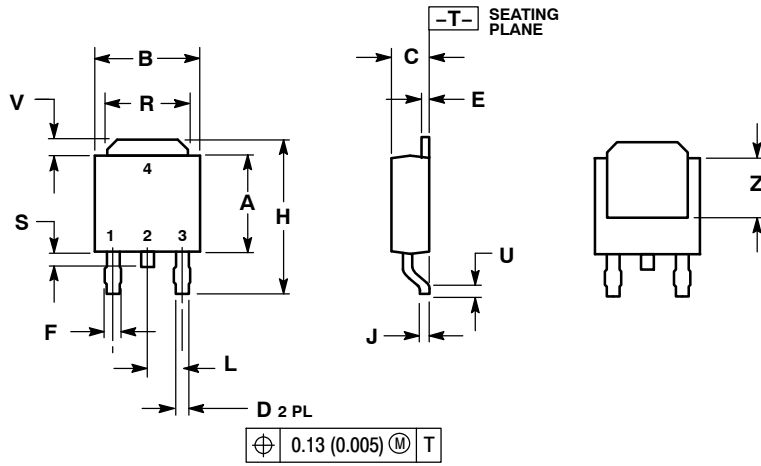
Device	Package	Shipping [†]
NTD4959NHT4G	DPAK (Pb-Free)	2500 / Tape & Reel
NTD4959NH-1G	IPAK (Pb-Free)	75 Units / Rail
NTD4959NH-35G	IPAK Trimmed Lead (3.5 ± 0.15 mm) (Pb-Free)	75 Units / Rail

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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PACKAGE DIMENSIONS

DPAK (SINGLE GAUGE)
CASE 369AA-01
ISSUE A

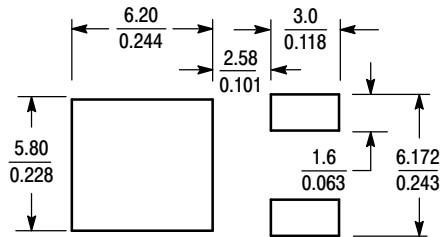


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.22
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.025	0.035	0.63	0.89
E	0.018	0.024	0.46	0.61
F	0.030	0.045	0.77	1.14
H	0.386	0.410	9.80	10.40
J	0.018	0.023	0.46	0.58
L	0.090 BSC		2.29 BSC	
R	0.180	0.215	4.57	5.45
S	0.024	0.040	0.60	1.01
U	0.020	---	0.51	---
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

SOLDERING FOOTPRINT*



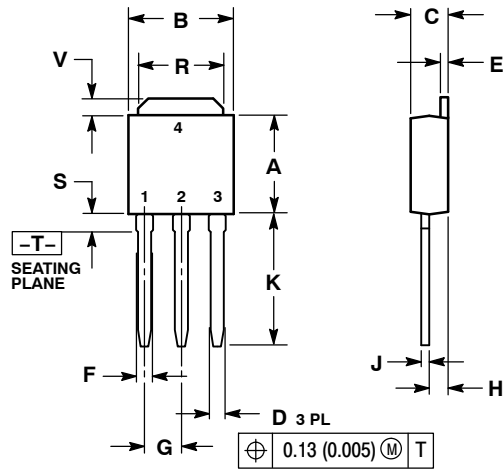
SCALE 3:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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PACKAGE DIMENSIONS

IPAK (STRAIGHT LEAD DPAK) CASE 369D-01 ISSUE B

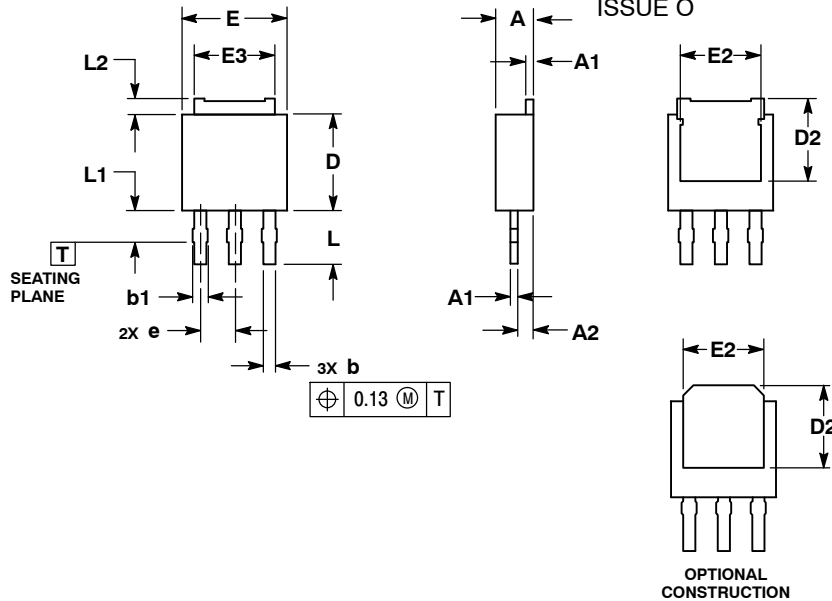


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.090 BSC		2.29 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.180	0.215	4.45	5.45
S	0.025	0.040	0.63	1.01
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

- STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

3.5 MM IPAK, STRAIGHT LEAD CASE 369AD-01 ISSUE O



- NOTES:
1.. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2.. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD GATE OR MOLD FLASH.

DIM	MILLIMETERS	
	MIN	MAX
A	2.19	2.38
A1	0.46	0.60
A2	0.87	1.10
b	0.69	0.89
b1	0.77	1.10
D	5.97	6.22
D2	4.80	---
E	6.35	6.73
E2	4.70	---
E3	4.45	5.46
e	2.28 BSC	
L	3.40	3.60
L1	---	2.10
L2	0.89	1.27

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