Power MOSFET

30 V, 29 A, Single N-Channel, SO-8 Flat Lead

Features

- Low R_{DS(on)}
- Optimized Gate Charge
- Low Inductance SO-8 Package
- These are Pb-Free Devices

Applications

- Notebooks, Graphics Cards
- DC-DC Converters
- Synchronous Rectification

MAXIMUM RATINGS ($T_J = 25^{\circ}C$ unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V_{DSS}	30	V
Gate-to-Source Voltage	Gate-to-Source Voltage			20	V
Continuous Drain Current	Steady	T _A = 25°C	I _D	17	Α
(Note 1)	State	T _A = 85°C		12	
	t ≤10 s	T _A = 25°C		29	
Power Dissipation (Note 1)	Steady State T _A = 25°C		P _D	2.2	W
	t ≤10 s			6.6	
Continuous Drain Current	Olerad	T _A = 25°C	I _D	11	Α
(Note 2)	Steady State	T _A = 85°C		8.0	
Power Dissipation (Note 2)	310113	T _A = 25°C	P_{D}	0.9	W
Pulsed Drain Current	t _p =	10 μs	I _{DM}	88	Α
Operating Junction and Storage Temperature			T _J , T _{stg}	-55 to 150	°C
Source Current (Body Diode)			IS	6.5	Α
Single Pulse Drain-to-Source Avalanche Energy (V_{DD} = 30 V, V_{GS} = 10 V, I_{PK} = 29 A, L = 1 mH, R_G = 25 Ω)			E _{AS}	430	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			TL	260	°C

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case - Steady State	$R_{\theta JC}$	2.2	°C/W
Junction-to-Ambient - Steady State (Note 1)	$R_{\theta JA}$	56.2	°C/W
Junction-to-Ambient - t ≤10 s (Note 1)	$R_{\theta JA}$	19	
Junction-to-Ambient - Steady State (Note 2)	$R_{\theta JA}$	141.1	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

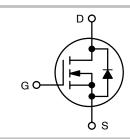
- 1. Surface mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces).
- Surface mounted on FR4 board using the minimum recommended pad size (Cu area = 1.0 in sq).



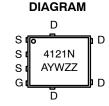
ON Semiconductor®

http://onsemi.com

V _{(BR)DSS}	R _{DS(on)} Typ	I _D Max (Note 1)
30 V	4.0 mΩ @ 10 V	29 A
30 7	5.5 mΩ @ 4.5 V	2011







MARKING

4121N = Specific Device Code A = Assembly Location

Y = Year
W = Work Week
ZZ = Lot Traceability

ORDERING INFORMATION

Device	Package	Shipping [†]
NTMFS4121NT1G	SO-8 FL (Pb-Free)	1500 Tape & Reel
NTMFS4121NT3G	SO-8 FL (Pb-Free)	5000 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

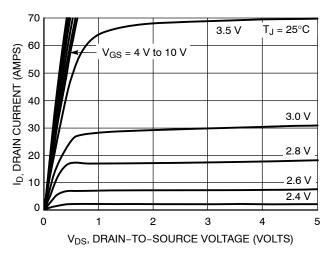
ELECTRICAL CHARACTERISTICS ($T_J = 25^{\circ}C$ unless otherwise noted)

Characteristic	Symbol	Test Condition	Test Condition		Тур	Max	Unit
OFF CHARACTERISTICS	•			•	•		•
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		30			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J				21		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	., .,,,	T _J = 25°C			1.0	μΑ
		$V_{GS} = 0 \text{ V}, V_{DS} = 24 \text{ V}$	T _J = 125°C			10	
Gate-to-Source Leakage Current	I _{GSS}	V _{DS} = 0 V, V _{GS} =	= 20 V			100	nA
ON CHARACTERISTICS (Note 3)							
Gate Threshold Voltage	V _{GS(TH)}	$V_{GS} = V_{DS}$, $I_D = 2$	250 μΑ	1.0		2.5	V
Negative Threshold Temperature Coefficient	V _{GS(TH)} /T _J				7.4		mV/°C
Drain-to-Source On Resistance	R _{DS(on)}	$V_{GS} = 10 \text{ V}, I_D = 24 \text{ A}$ $V_{GS} = 4.5 \text{ V}, I_D = 21 \text{ A}$			4.2	5.25	mΩ
					5.5	7.0	1
Forward Transconductance	9FS	V _{DS} = 15 V, I _D = 24 A			20		S
CHARGES, CAPACITANCES AND GATE R	ESISTANCE						
Input Capacitance	C _{ISS}	V _{GS} = 0 V, f = 1.0 MHz, V _{DS} = 24 V			2700		pF
Output Capacitance	C _{OSS}				480		
Reverse Transfer Capacitance	C _{RSS}				290		
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 4.5 V, V _{DS} = 15 V, I _D = 21 A			24	40	nC
Threshold Gate Charge	Q _{G(TH)}				3.0		- - -
Gate-to-Source Charge	Q_{GS}				7.3		
Gate-to-Drain Charge	Q_{GD}				10.2		
Gate Resistance	R_{G}				1.5		Ω
SWITCHING CHARACTERISTICS, V _{GS} = 4.	5 V (Note 4)				_		_
Turn-On Delay Time	t _{d(ON)}	$V_{GS} = 4.5 \text{ V}, V_{DS} = 15 \text{ V},$ $I_{D} = 1.0 \text{ A}, R_{L} = 15 \Omega, R_{G} = 3.0 \Omega$			16		ns
Rise Time	t _r				29		
Turn-Off Delay Time	t _{d(OFF)}				32		
Fall Time	t _f				31		
DRAIN-SOURCE DIODE CHARACTERISTI	cs						
Forward Diode Voltage	V _{SD}	V _{GS} = 0 V, I _S = 6.0 A	T _J = 25°C		0.8	1.0	V
			T _J = 125°C		0.6		1
Reverse Recovery Time	t _{RR}	$V_{GS} = 0 \text{ V, } dI_{S}/dt = 100 \text{ A/}\mu\text{s,}$ $I_{S} = 6.0 \text{ A}$			34		ns
Charge Time	t _a				18		1
Discharge Time	t _b				16		1
Reverse Recovery Charge	Q _{RR}				25.4		nC

Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
 Switching characteristics are independent of operating junction temperatures.

TYPICAL PERFORMANCE CURVES

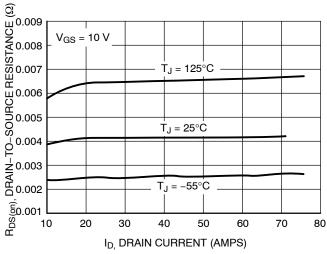
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 $V_{DS} \ge 10 \text{ V}$ 60 ID, DRAIN CURRENT (AMPS) 50 40 30 T_J = 125°C 20 T_J = 25°C 10 $T_J = -55^{\circ}C$ 0 0 5 3 V_{GS}, GATE-TO-SOURCE VOLTAGE (VOLTS)

Figure 1. On-Region Characteristics

Figure 2. Transfer Characteristics



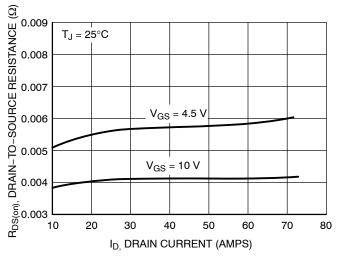
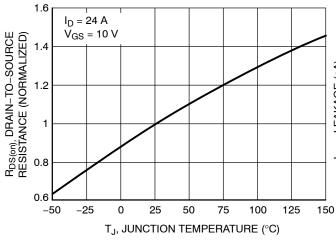


Figure 3. On-Resistance vs. Drain Current and Temperature

Figure 4. On-Resistance vs. Drain Current and Gate Voltage



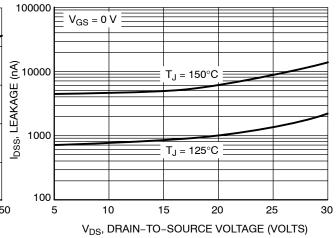


Figure 5. On–Resistance Variation with Temperature

Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL PERFORMANCE CURVES

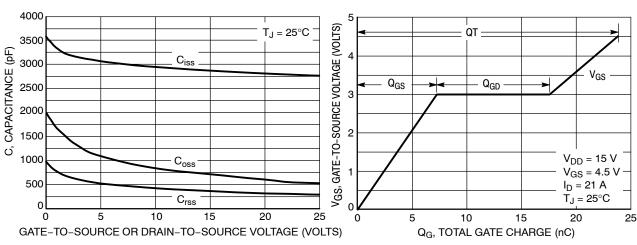


Figure 7. Capacitance Variation

Figure 8. Gate-To-Source and Drain-To-Source Voltage vs. Total Charge

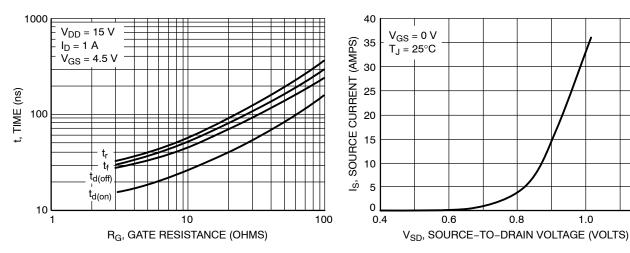


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

Figure 10. Diode Forward Voltage vs. Current

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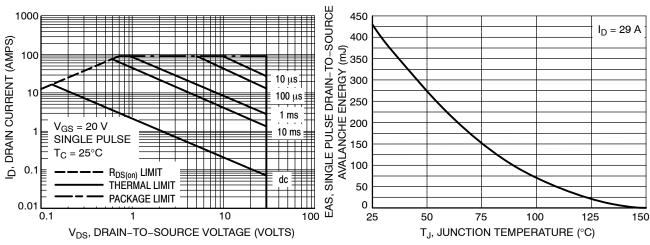


Figure 11. Maximum Rated Forward Biased Safe Operating Area

Figure 12. Maximum Avalanche Energy vs Starting Junction Temperature

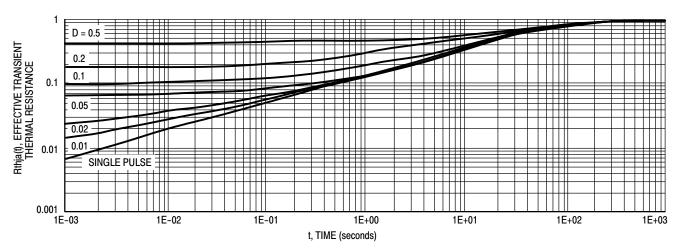
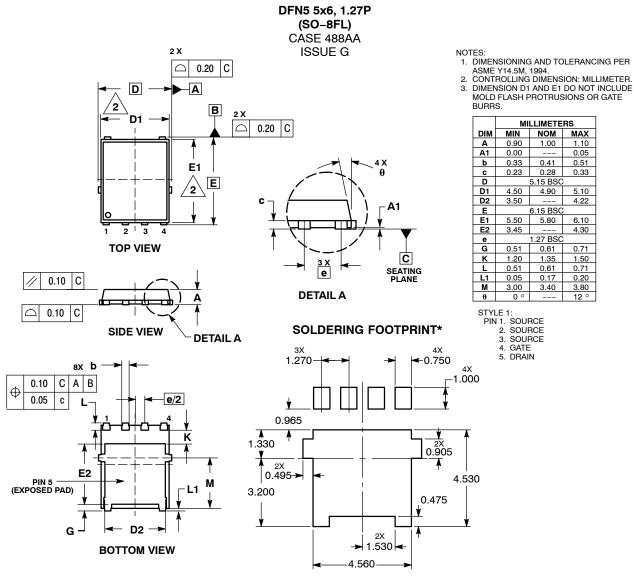


Figure 13. Thermal Response

PACKAGE DIMENSIONS



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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