MOSFET – Power 60 V, 63 A, 12.4 m Ω

Features

- Low R_{DS(on)}
- High Current Capability
- Avalanche Energy Specified
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS (T_J = 25°C unless otherwise stated)

Parameter			Symbol	Value	Units	
Drain-to-Source Voltage		V_{DSS}	60	V		
Gate-to-Source Voltage	e – Contin	uous	V_{GS}	±20	V	
Gate-to-Source Voltage – Non-Repetitive (t _p = 10 μs)		V_{GS}	±30	V		
Continuous Drain	Steady 1.C - 20 0		I _D	63	Α	
Current – R _{θJC} (Note 1)	State	T _C = 100°C		45		
Power Dissipation -	Steady	T _C = 25°C	P_{D}	107	W	
R _{θJC} (Note 1)		T _C = 100°C		54		
Pulsed Drain Current	t _p = 10 μs		I _{DM}	252	Α	
Operating Junction and Storage Temperature		T _J , T _{STG}	–55 to 175	°C		
Source Current (Body Diode) Pulsed			IS	63	Α	
Single Pulse Drain-to Source Avalanche		EAS	80	mJ		
Energy – (L = 0.1 mH)		IAS	40	Α		
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		T_L	260	°C		

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Units
Junction-to-Case (Drain) - Steady State (Note 1)	$R_{\theta JC}$	1.4	°C/W
Junction-to-Ambient - Steady State (Note 1)	$R_{\theta JA}$	33	°C/W

1. Surface mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces).

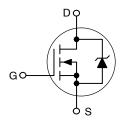


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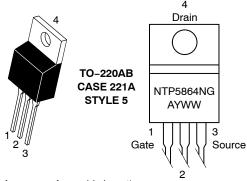
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V _{(BR)DSS}	R _{DS(ON)} MAX	I _D MAX (Note 1)
60 V	12.4 mΩ @ 10 V	63 A

N-Channel



MARKING DIAGRAM & PIN ASSIGNMENT



A = Assembly Location

Y = Year WW = Work Week

G

= Pb-Free Package

ORDERING INFORMATION

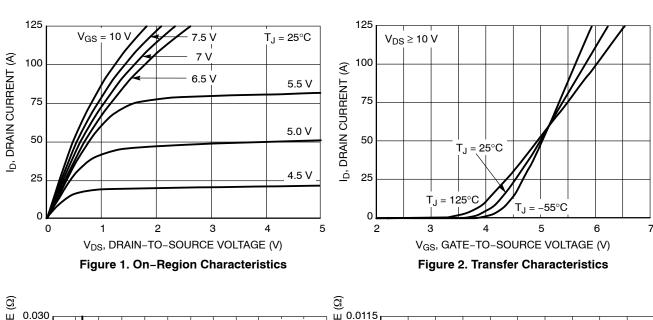
Device	Package	Shipping
NTP5864NG	TO-220 (Pb-Free)	50 Units / Rail

ELECTRICAL CHARACTERISTICS ($T_J = 25^{\circ}C$ unless otherwise stated)

Parameter	Symbol	Test Condition		Min	Тур	Max	Unit
OFF CHARACTERISTICS	•		•		•		•
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		60			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J				58		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V, V _{DS} = 60 V	T _J = 25°C			1.0	μΑ
Gate-to-Source Leakage Current	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V				±100	nA
ON CHARACTERISTICS (Note 2)							
Gate Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _E	ο = 250 μΑ	2.0		4.0	٧
Gate Threshold Temperature Coefficient	V _{GS(TH)} /T _J				-10		mV/°C
Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = 10 V,	I _D = 20 A		10.2	12.4	mΩ
Forward Transconductance	9FS	V _{DS} = 15 V,	I _D = 20 A		10		S
CHARGES AND CAPACITANCES							
Input Capacitance	C _{ISS}				1680		pF
Output Capacitance	C _{OSS}	V _{GS} = 0 V, f = V _{DS} = 2	: 1.0 MHz, 25 V		189		
Reverse Transfer Capacitance	C _{RSS}	- 503			124		
Total Gate Charge	Q _{G(TOT)}				31		nC
Threshold Gate Charge	Q _{G(TH)}	$V_{GS} = 10 \text{ V}, V_{DS} = 48 \text{ V},$ $I_{D} = 20 \text{ A}$			2.0		
Gate-to-Source Charge	Q_{GS}				7.3		
Gate-to-Drain Charge	Q_{GD}				10		
Gate Resistance	R_{g}				0.5		Ω
SWITCHING CHARACTERISTICS, V_0	as = 10 V (Note	3)					
Turn-On Delay Time	t _{d(ON)}				10		ns
Rise Time	t _r	V _{GS} = 10 V, V	_{DD} = 48 V,		6.4		
Turn-Off Delay Time	t _{d(OFF)}	I _D = 20 A, R	$_{\rm G}$ = 2.5 Ω		18		
Fall Time	t _f				4.6		
DRAIN-SOURCE DIODE CHARACTE	RISTICS						
Forward Diode Voltage	V_{SD}	V _{GS} = 0 V,	T _J = 25°C		0.94	1.2	٧
		I _S = 40 A	T _J = 125°C		0.84		
Reverse Recovery Time	t _{RR}	$V_{GS} = 0 \text{ V}, \text{ dI}_{SD}/\text{dt} = 100 \text{ A}/\mu\text{s}, \\ I_{S} = 20 \text{ A}$			24		ns
Charge Time	t _a				16		
Discharge Time	t _b				7.9		
Reverse Recovery Charge	Q _{RR}				20		nC

Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
 Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS



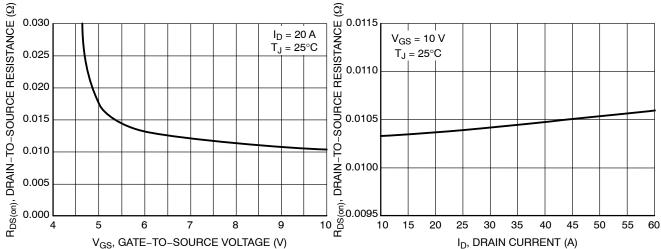
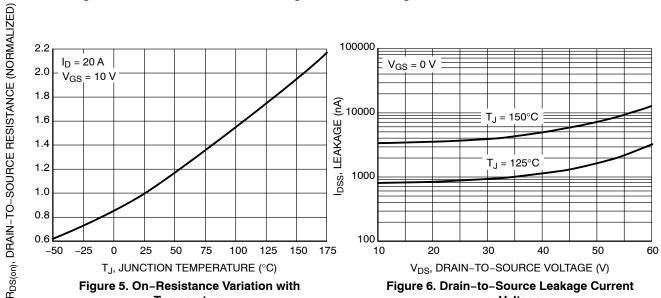


Figure 3. On-Resistance vs. Gate Voltage

Figure 4. On-Resistance vs. Drain Current



Temperature

vs. Voltage

TYPICAL CHARACTERISTICS

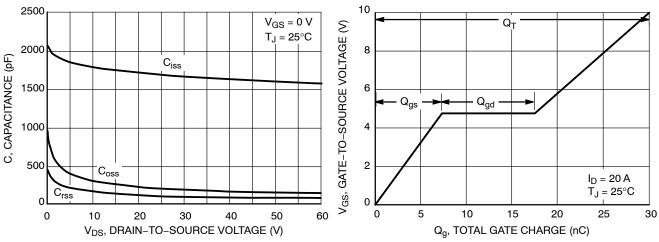


Figure 7. Capacitance Variation

Figure 8. Gate-to-Source vs. Total Charge

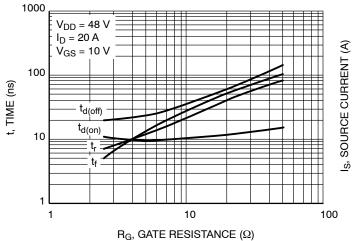


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

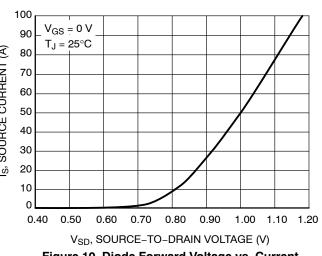


Figure 10. Diode Forward Voltage vs. Current

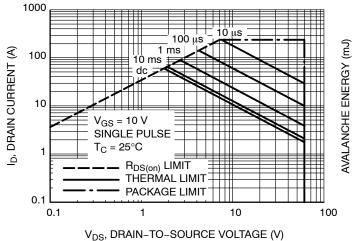
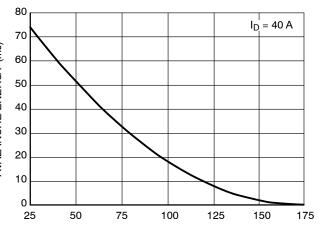


Figure 11. Maximum Rated Forward Biased Safe Operating Area



T_J, STARTING JUNCTION TEMPERATURE Figure 12. Maximum Avalanche Energy versus **Starting Junction Temperature**

TYPICAL CHARACTERISTICS

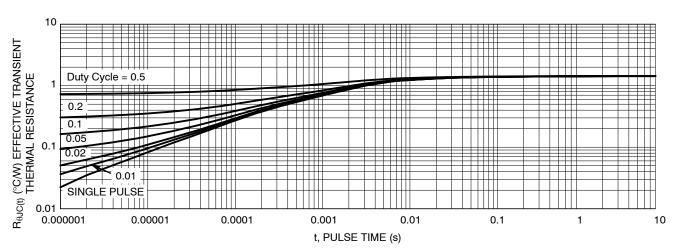
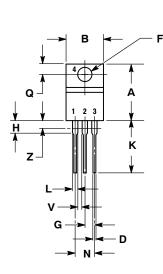
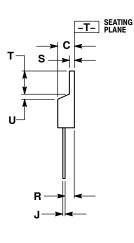


Figure 13. Thermal Response

PACKAGE DIMENSIONS

TO-220 CASE 221A-09 **ISSUE AH**





NOTES

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982. CONTROLLING DIMENSION: INCH.
- DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE

	INCHES		MILLIMETERS		
DIM	MIN	MAX	MIN	MAX	
Α	0.570	0.620	14.48	15.75	
В	0.380	0.415	9.66	10.53	
С	0.160	0.190	4.07	4.83	
D	0.025	0.038	0.64	0.96	
F	0.142	0.161	3.61	4.09	
G	0.095	0.105	2.42	2.66	
Н	0.110	0.161	2.80	4.10	
J	0.014	0.024	0.36	0.61	
K	0.500	0.562	12.70	14.27	
L	0.045	0.060	1.15	1.52	
N	0.190	0.210	4.83	5.33	
Q	0.100	0.120	2.54	3.04	
R	0.080	0.110	2.04	2.79	
S	0.045	0.055	1.15	1.39	
T	0.235	0.255	5.97	6.47	
U	0.000	0.050	0.00	1.27	
٧	0.045		1.15		
Z		0.080		2.04	

STYLE 5:

PIN 1. GATE DRAIN 2.

- SOURCE
- DRAIN

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