# **MOSFET** – Power

# 60 V, 37 A, 11.5 m $\Omega$

#### **Features**

- Low R<sub>DS(on)</sub>
- Low Capacitance
- Optimized Gate Charge
- These Devices are Pb-Free and are RoHS Compliant

## **MAXIMUM RATINGS** ( $T_J = 25^{\circ}C$ unless otherwise stated)

Param	Symbol	Value	Unit		
Drain-to-Source Voltage			V <sub>DSS</sub>	60	V
Gate-to-Source Voltage			V <sub>GS</sub>	±20	V
Continuous Drain		T <sub>A</sub> = 25°C	I <sub>D</sub>	11	Α
Current R <sub>θJA</sub> (Note 1)		T <sub>A</sub> = 100°C		7	
Power Dissipation R <sub>θJA</sub>		T <sub>A</sub> = 25°C	$P_{D}$	2.7	W
(Note 1)	Steady	T <sub>A</sub> = 100°C		1.1	
Continuous Drain	State	T <sub>C</sub> = 25°C	I <sub>D</sub>	37	Α
Current R <sub>θJC</sub> (Note 1)		T <sub>C</sub> = 100°C		24	
Power Dissipation		T <sub>C</sub> = 25°C	P <sub>D</sub>	33	W
R <sub>θJC</sub> (Note 1)		T <sub>C</sub> = 100°C		13	
Pulsed Drain Current	t <sub>p</sub> =	10 μs	I <sub>DM</sub>	149	Α
Operating Junction and Storage Temperature			T <sub>J</sub> , T <sub>stg</sub>	-55 to +150	°C
Source Current (Body Diode)			I <sub>S</sub>	37	Α
Single Pulse Drain-to-Source Avalanche Energy		E <sub>AS</sub>	48	mJ	
			I <sub>AS</sub>	31	Α
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T <sub>L</sub>	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

#### THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case - Steady State (Note 1)	$R_{ hetaJC}$	3.8	°C/W
Junction-to-Ambient - Steady State (Note 1)	$R_{ heta JA}$	46.7	

Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces.

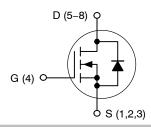


## ON Semiconductor®

#### http://onsemi.com

V <sub>(BR)DSS</sub>	R <sub>DS(on)</sub> MAX	I <sub>D</sub> MAX	
60 V	11.5 mΩ @ 10 V	37 A	
60 V	15 mΩ @ 4.5 V	37 A	

#### **N-Channel MOSFET**





CASE 511AB

#### **MARKING DIAGRAM**



5820 = Specific Device Code A = Assembly Location

Y = Year WW = Work Week

(Note: Microdot may be in either location)

= Pb-Free Package

#### **ORDERING INFORMATION**

Device	Package	Shipping <sup>†</sup>
NTTFS5820NLTAG	WDFN8 (Pb-Free)	1500 / Tape & Reel
NTTFS5820NLTW0	WDFN8 (Pb-Free)	5000 / Tape & Reel

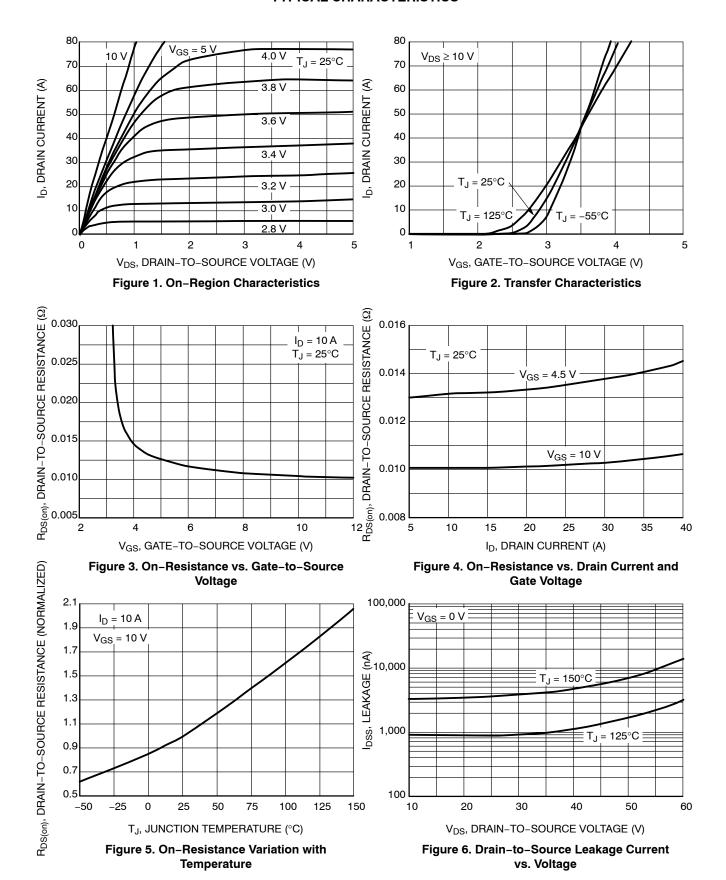
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

# **ELECTRICAL CHARACTERISTICS** (T<sub>J</sub> = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Тур	Max	Unit
OFF CHARACTERISTICS	•				•	1	-1
Drain-to-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		60			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V <sub>(BR)DSS</sub> /T <sub>J</sub>				57		mV/°C
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V,	T <sub>J</sub> = 25°C			1.0	μΑ
		$V_{DS} = 60 \text{ V}$	T <sub>J</sub> = 125°C			10	
Gate-to-Source Leakage Current	I <sub>GSS</sub>	$V_{DS} = 0 V, V_{GS}$	= ±20 V			±100	nA
ON CHARACTERISTICS (Note 2)			•		•	•	
Gate Threshold Voltage	V <sub>GS(TH)</sub>	$V_{GS} = V_{DS}, I_D =$	250 μΑ	1.5		2.3	V
Negative Threshold Temperature Coefficient	V <sub>GS(TH)</sub> /T <sub>J</sub>				6.2		mV/°C
Drain-to-Source On Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 8.7 A		10.1	11.5	mΩ
		V <sub>GS</sub> = 4.5 V	I <sub>D</sub> = 7.3 A		13.0	15	╡ !
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> = 5 V, I <sub>D</sub> :	= 10 A		24.6		S
CHARGES, CAPACITANCES AND GA	ATE RESISTAN	ICE	I				
Input Capacitance	C <sub>iss</sub>				1462		pF
Output Capacitance	C <sub>oss</sub>	V <sub>GS</sub> = 0 V, f = 1.0 MH	z, V <sub>DS</sub> = 25 V		150		
Reverse Transfer Capacitance	C <sub>rss</sub>	, , ,			96		
Total Gate Charge	Q <sub>G(TOT)</sub>	$V_{GS} = 10 \text{ V}, V_{DS} = 48$	3 V, I <sub>D</sub> = 10 A		28		nC
		V <sub>GS</sub> = 4.5 V, V <sub>DS</sub> = 4	8 V, I <sub>D</sub> = 10 A		15		
Threshold Gate Charge	Q <sub>G(TH)</sub>				1		nC
Gate-to-Source Charge	Q <sub>GS</sub>		_ ,,,		4		1
Gate-to-Drain Charge	$Q_{GD}$	$V_{GS} = 4.5 \text{ V}, V_{DS} = 4.5 \text{ V}$	8 V, I <sub>D</sub> = 10 A		8		1
Plateau Voltage	V <sub>GP</sub>				3		V
Gate Resistance	$R_{G}$				0.62		Ω
SWITCHING CHARACTERISTICS (No	ote 3)					•	•
Turn-On Delay Time	t <sub>d(on)</sub>				10		ns
Rise Time	t <sub>r</sub>	V <sub>GS</sub> = 4.5 V, V <sub>DS</sub>	s = 48 V.		28		1
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D = 10 \text{ A}, R_G = 2.5 \Omega$			19		7
Fall Time	t <sub>f</sub>				22		7
DRAIN-SOURCE DIODE CHARACTE	RISTICS				-	-	-
Forward Diode Voltage	oltage V <sub>SD</sub>	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 10 A	T <sub>J</sub> = 25°C		0.79	1.2	V
			T <sub>J</sub> = 125°C		0.65		
Reverse Recovery Time	t <sub>RR</sub>	$V_{GS} = 0 \text{ V, } d_{IS}/d_t = 100 \text{ A/}\mu\text{s,}$ $I_S = 10 \text{ A}$			19		ns
Charge Time	t <sub>a</sub>				13		
Discharge Time	t <sub>b</sub>				6		
Reverse Recovery Charge	Q <sub>RR</sub>				15		nC

<sup>2.</sup> Pulse Test: pulse width  $\leq 300~\mu s$ , duty cycle  $\leq 2\%$ . 3. Switching characteristics are independent of operating junction temperatures.

#### **TYPICAL CHARACTERISTICS**



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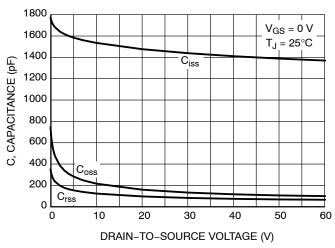


Figure 7. Capacitance Variation

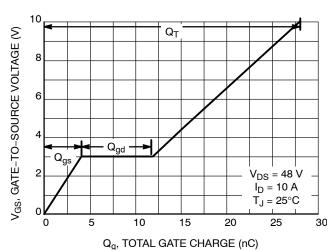


Figure 8. Gate-to-Source Voltage vs. Total Charge

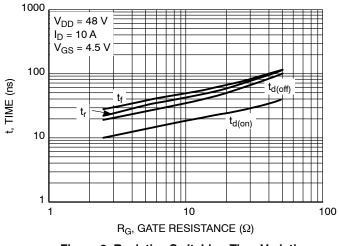


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

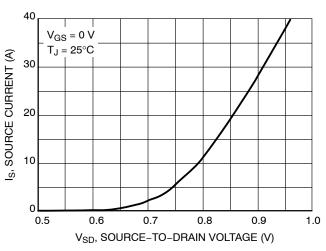


Figure 10. Diode Forward Voltage vs. Current

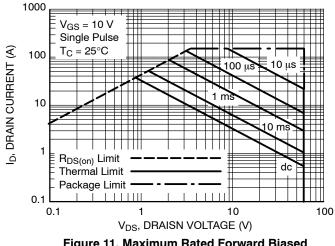


Figure 11. Maximum Rated Forward Biased Safe Operating Area

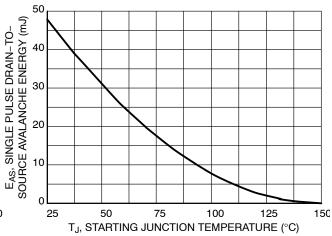


Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature

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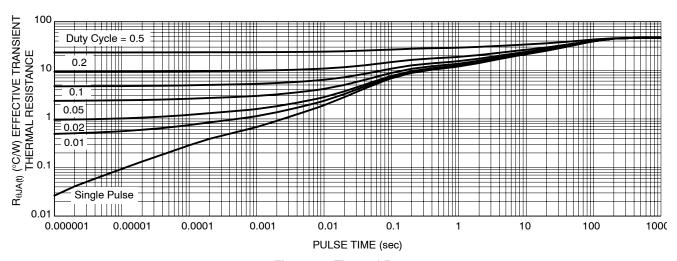
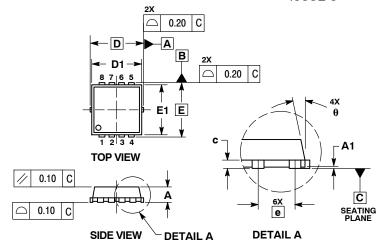


Figure 13. Thermal Response

#### PACKAGE DIMENSIONS

# WDFN8 3.3x3.3, 0.65P

CASE 511AB **ISSUE C** 

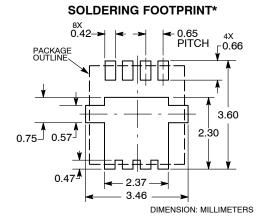


#### NOTES:

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994. CONTROLLING DIMENSION: MILLIMETERS.
- DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

	MILLIMETERS			INCHES			
DIM	MIN	NOM	MAX	MIN	NOM	MAX	
Α	0.70	0.75	0.80	0.028	0.030	0.031	
A1	0.00		0.05	0.000		0.002	
b	0.23	0.30	0.40	0.009	0.012	0.016	
С	0.15	0.20	0.25	0.006	0.008	0.010	
D		3.30 BSC		C	.130 BSC	)	
D1	2.95	3.05	3.15	0.116	0.120	0.124	
D2	1.98	2.11	2.24	0.078	0.083	0.088	
E		3.30 BSC		0.130 BSC			
E1	2.95	3.05	3.15	0.116	0.120	0.124	
E2	1.47	1.60	1.73	0.058	0.063	0.068	
E3	0.23	0.30	0.40	0.009	0.012	0.016	
е		0.65 BSC		0.026 BSC			
G	0.30	0.41	0.51	0.012	0.016	0.020	
K	0.64			0.025			
L	0.30	0.43	0.56	0.012	0.017	0.022	
L1	0.06	0.13	0.20	0.002	0.005	0.008	
М	1.40	1.50	1.60	0.055	0.059	0.063	
θ	0°		12°	0°		12°	

## 0.10 С Α В С 0.05 Å E2 E3\_ D2 G **BOTTOM VIEW**



\*For additional information on our Pb -Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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