NVD5C668NL

Power MOSFET

60 V, 8.9 mΩ, 49 A, Single N−Channel

Features

- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

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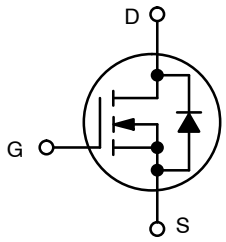
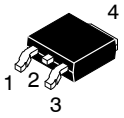
$V_{(BR)DSS}$	$R_{DS(on)}$	I_D
60 V	8.9 mΩ @ 10 V	49 A
	12.8 mΩ @ 4.5 V	



N−CHANNEL MOSFET



DPAK
CASE 369C
STYLE 2

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	60	V
Gate−to−Source Voltage			V_{GS}	±20	V
Continuous Drain Current $R_{\theta JC}$ (Notes 1 & 3)	Steady State	T_C = 25°C	I_D	49	A
		T_C = 100°C		34	
Power Dissipation $R_{\theta JC}$ (Note 1)		T_C = 25°C	P_D	44	W
		T_C = 100°C		22	
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2 & 3)	Steady State	T_A = 25°C	I_D	13	A
		T_A = 100°C		9.0	
Power Dissipation $R_{\theta JA}$ (Notes 1 & 2)		T_A = 25°C	P_D	3.1	W
		T_A = 100°C		1.5	
Pulsed Drain Current	T_A = 25°C, t_p = 10 μs		I_{DM}	250	A
Operating Junction and Storage Temperature			T_J, T_{stg}	−55 to 175	°C
Source Current (Body Diode)			I_S	25	A
Single Pulse Drain−to−Source Avalanche Energy (T_J = 25°C, $I_{L(pk)}$ = 3 A)			E_{AS}	104	mJ
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)			T_L	260	°C

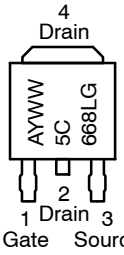
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction−to−Case (Drain) (Note 1)	$R_{\theta JC}$	3.4	°C/W
Junction−to−Ambient − Steady State (Note 2)	$R_{\theta JA}$	48.7	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface−mounted on FR4 board using a 650 mm^2, 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

MARKING DIAGRAM & PIN ASSIGNMENT



A = Assembly Location
Y = Year
WW = Work Week
5C668L = Device Code
G = Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA		60			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$				27		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 60 V	T_J = 25°C			10	μA
			T_J = 125°C			250	
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = 20 V				100	nA
ON CHARACTERISTICS (Note 4)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 50 μA		1.2		2.1	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$				4.8		mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 25 A			7.4	8.9	mΩ
		V_{GS} = 4.5 V, I_D = 25 A			10.2	12.8	
Forward Transconductance	g_{FS}	V_{DS} = 15 V, I_D = 25 A			60		S
CHARGES, CAPACITANCES AND GATE RESISTANCES							
Input Capacitance	C_{iss}	V_{GS} = 0 V, f = 1.0 MHz, V_{DS} = 25 V			1300		pF
Output Capacitance	C_{oss}				580		
Reverse Transfer Capacitance	C_{rss}				18		
Total Gate Charge	$Q_{G(TOT)}$	V_{DS} = 48 V, I_D = 25 A	V_{GS} = 4.5 V		8.7		nC
			V_{GS} = 10 V		18.7		
Threshold Gate Charge	$Q_{G(TH)}$	V_{GS} = 4.5 V, V_{DS} = 48 V, I_D = 25 A			2.4		nC
Gate−to−Source Charge	Q_{GS}				4.1		
Gate−to−Drain Charge	Q_{GD}				2.0		
Plateau Voltage	V_{GP}				3.1		V
SWITCHING CHARACTERISTICS (Note 5)							
Turn−On Delay Time	$t_{d(on)}$	V_{GS} = 4.5 V, V_{DS} = 48 V, I_D = 25 A, R_G = 2.5 Ω			12		ns
Rise Time	t_r				74		
Turn−Off Delay Time	$t_{d(off)}$				26		
Fall Time	t_f				62		
DRAIN−SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 20 A	T_J = 25°C		0.87	1.2	V
			T_J = 125°C		0.76		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dIs/dt = 100 A/μs, I_S = 25 A			32		ns
Charge Time	ta				15		
Discharge Time	tb				16		
Reverse Recovery Charge	Q_{RR}				20		nC

4. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
5. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

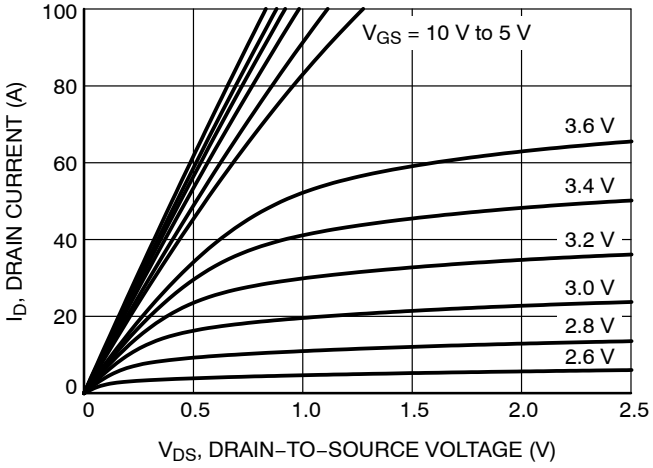


Figure 1. On−Region Characteristics

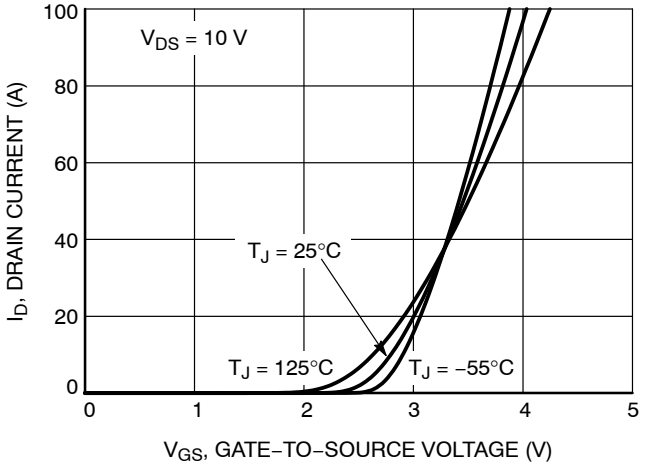


Figure 2. Transfer Characteristics

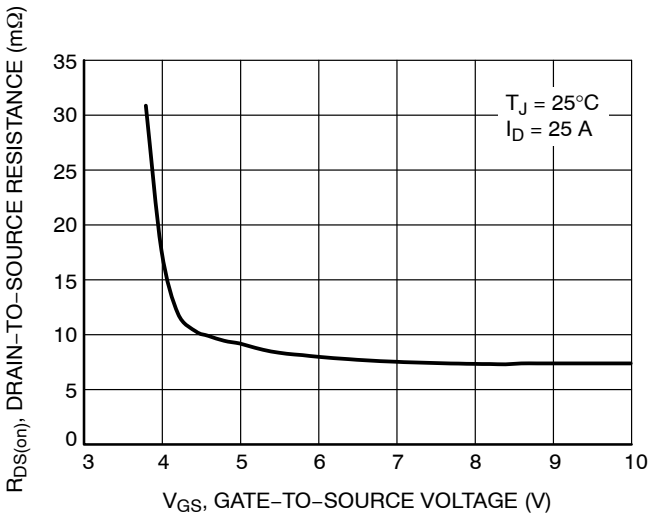


Figure 3. On−Resistance vs. Gate−to−Source Voltage

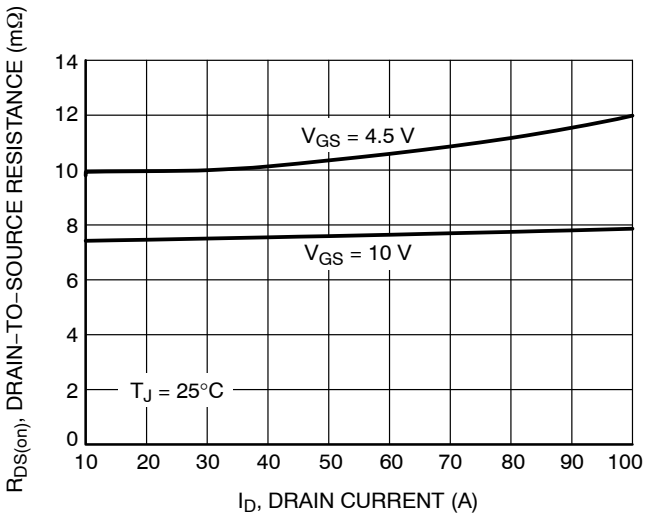


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

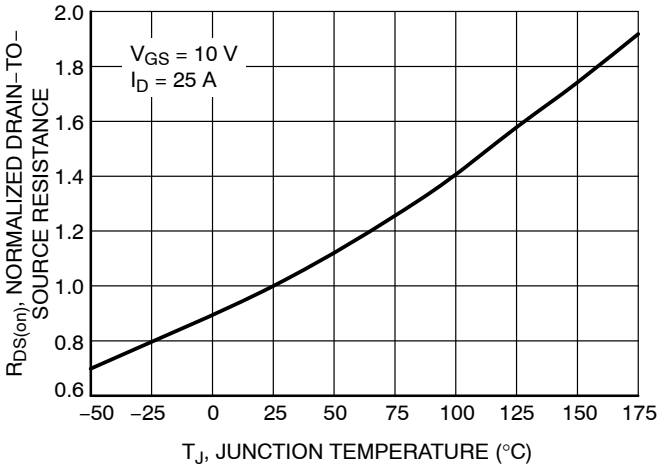


Figure 5. On−Resistance Variation with Temperature

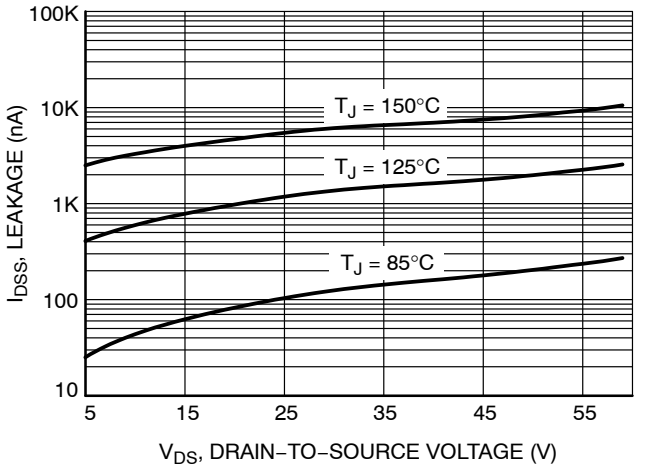


Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

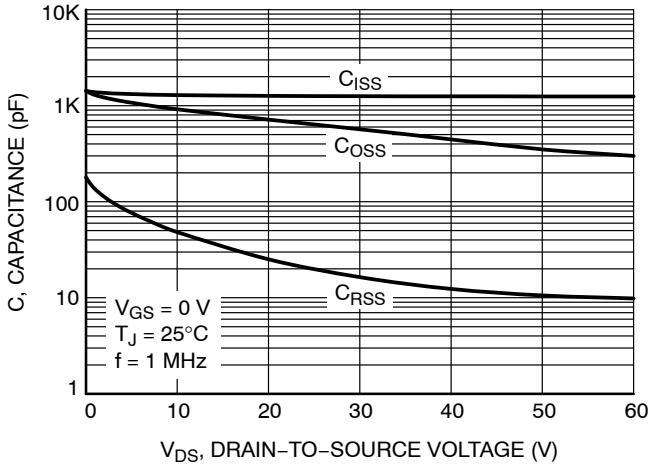


Figure 7. Capacitance Variation

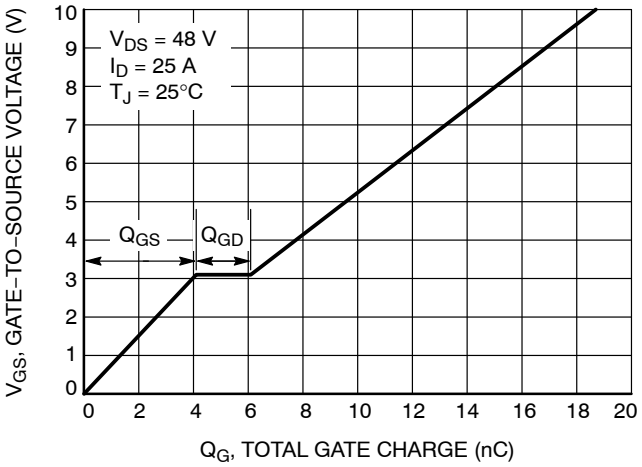


Figure 8. Gate−to−Source vs. Total Charge

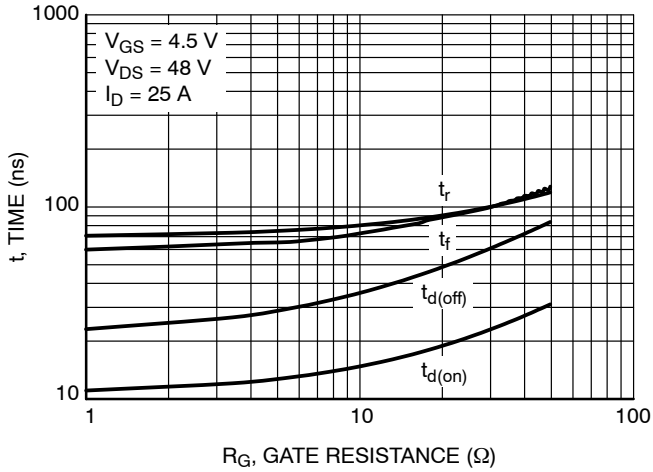


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

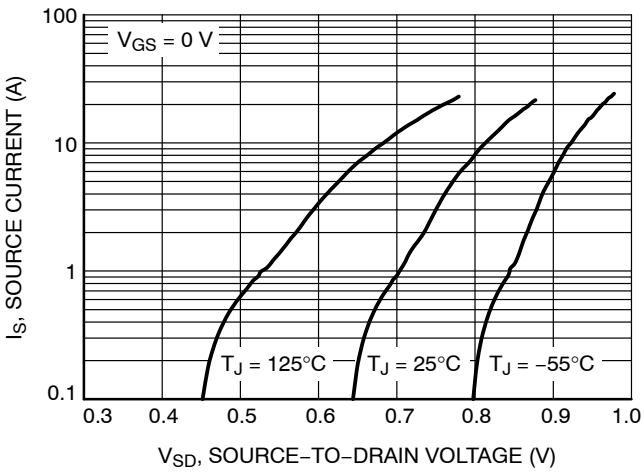


Figure 10. Diode Forward Voltage vs. Current

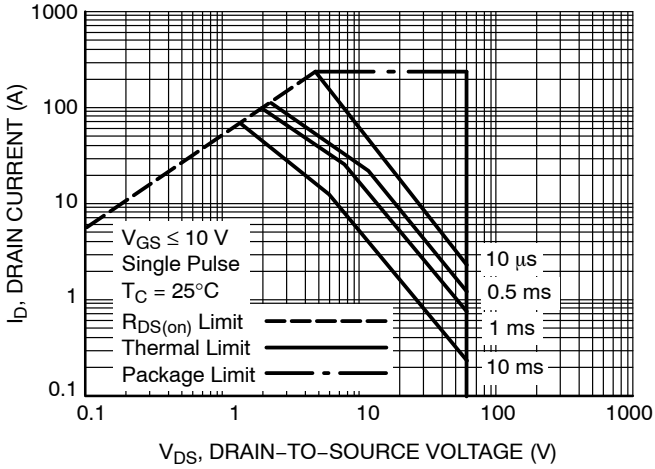


Figure 11. Maximum Rated Forward Biased Safe Operating Area

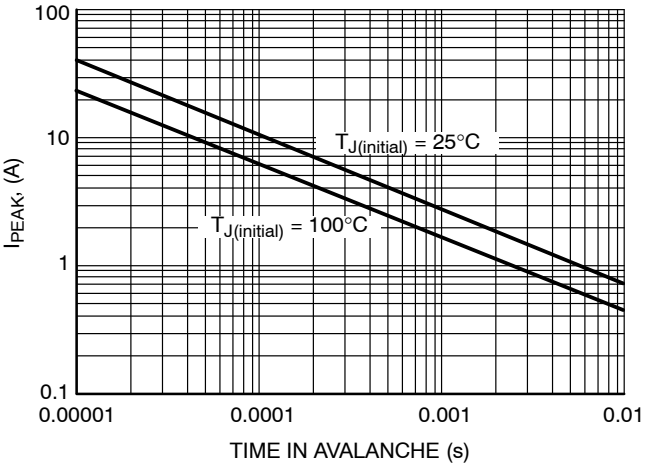


Figure 12. Maximum Drain Current vs. Time in Avalanche

TYPICAL CHARACTERISTICS

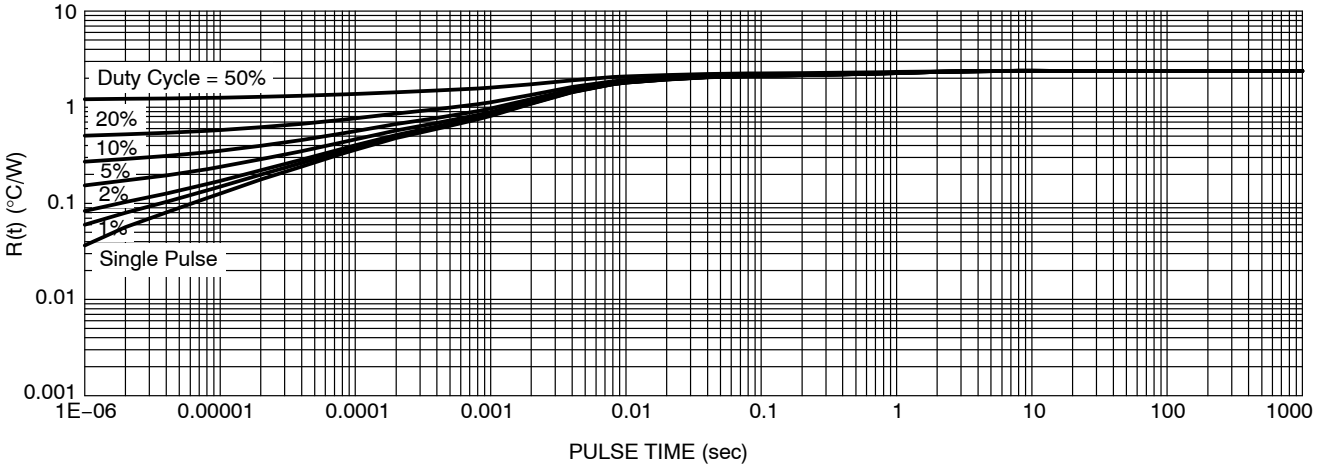
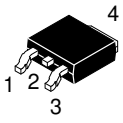


Figure 13. Thermal Response

ORDERING INFORMATION

Order Number	Package	Shipping†
NVD5C668NLT4G	DPAK (Pb−Free)	2500 / Tape & Reel

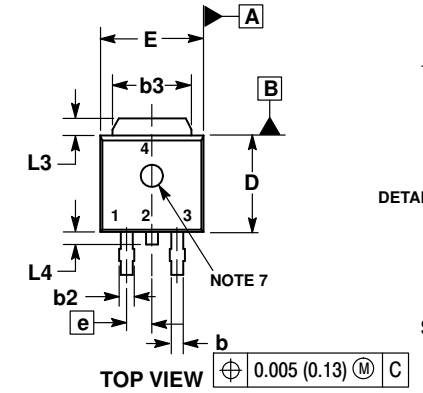
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

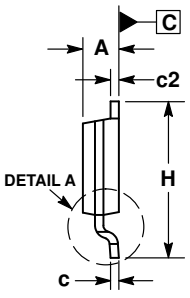


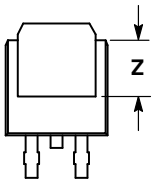
SCALE 1:1

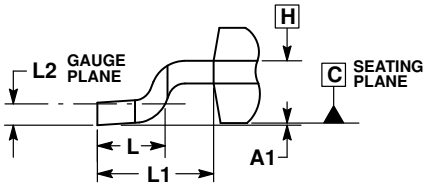
DPAK (SINGLE GAUGE)
CASE 369C
ISSUE F

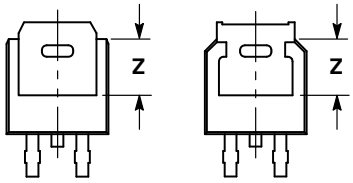
DATE 21 JUL 2015











NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.028	0.045	0.72	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.114 REF		2.90 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4	---	0.040	---	1.01
Z	0.155	---	3.93	---

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

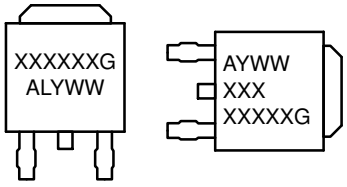
STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 8:
PIN 1. N/C
2. CATHODE
3. ANODE
4. CATHODE

STYLE 9:
PIN 1. ANODE
2. CATHODE
3. RESISTOR ADJUST
4. CATHODE

STYLE 10:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

GENERIC MARKING DIAGRAM*

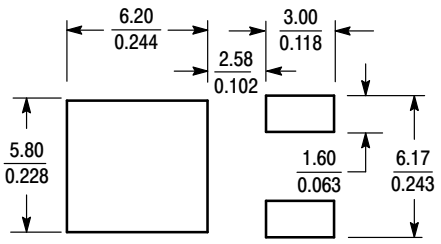


IC **Discrete**

XXXXXX = Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking.

SOLDERING FOOTPRINT*



SCALE 3:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ISSUE	REVISION	DATE
O	RELEASED FOR PRODUCTION. REQ. BY L. GAN	24 SEP 2001
A	ADDED STYLE 8. REQ. BY S. ALLEN.	06 AUG 2008
B	ADDED STYLE 9. REQ. BY D. WARNER.	16 JAN 2009
C	ADDED STYLE 10. REQ. BY S. ALLEN.	09 JUN 2009
D	RELABELED DRAWING TO JEDEC STANDARDS. ADDED SIDE VIEW DETAIL A. CORRECTED MARKING INFORMATION. REQ. BY D. TRUHITTE.	29 JUN 2010
E	ADDED ALTERNATE CONSTRUCTION BOTTOM VIEW. MODIFIED DIMENSIONS b2 AND L1. CORRECTED MARKING DIAGRAM FOR DISCRETE. REQ. BY I. CAMBALIZA.	06 FEB 2014
F	ADDED SECOND ALTERNATE CONSTRUCTION BOTTOM VIEW. REQ. BY K. MUSTAFA.	21 JUL 2015

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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Europe, Middle East and Africa Technical Support:
Phone: 00421 33 790 2910
For additional information, please contact your local Sales Representative

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