NVTFS4C08N

MOSFET – Power, Single N-Channel, µ8FL

30 V, 5.9 mΩ, 55 A

Features

- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Optimized Gate Charge to Minimize Switching Losses
- NVTFS4C08NWF – Wettable Flanks Product
- NVT Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS (T_J = 25°C unless otherwise stated)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	30	V
Gate−to−Source Voltage			V_{GS}	±20	V
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2, 4)	Steady State	T_A = 25°C	I_D	17	A
		T_A = 100°C		12	
Power Dissipation $R_{\theta JA}$ (Note 1, 2, 4)		T_A = 25°C	P_D	3.1	W
		T_A = 100°C		1.6	
Continuous Drain Current $R_{\theta JC}$ (Note 1, 3, 4)		T_A = 25°C	I_D	55	
		T_A = 100°C		39	A
Power Dissipation $R_{\theta JC}$ (Note 1, 3, 4)		T_A = 25°C	P_D	31	W
		T_A = 100°C		15	
Pulsed Drain Current	T_A = 25°C, t_p = 10 µs		I_{DM}	253	A
Operating Junction and Storage Temperature			T_J, T_{stg}	−55 to +175	°C
Source Current (Body Diode)			I_S	28	A
Single Pulse Drain−to−Source Avalanche Energy (T_J = 25°C, I_L = 20 A_{pk}, L = 0.1 mH)			E_{AS}	20	mJ
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)			T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction−to−Case − Steady State (Drain) (Notes 1 and 4)	$R_{\theta JC}$	4.9	°C/W
Junction−to−Ambient − Steady State (Notes 1 and 2)	$R_{\theta JA}$	48	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface−mounted on FR4 board using a 650 mm^2 2 oz. Cu pad.
3. Assumes heat−sink sufficiently large to maintain constant case temperature independent of device power.
4. Continuous DC current rating. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

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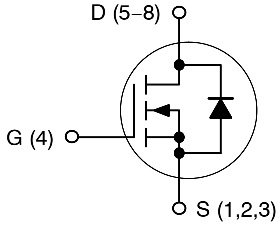
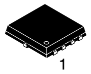
$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	I_D MAX
30 V	5.9 mΩ @ 10 V	55 A
	9.0 mΩ @ 4.5 V	

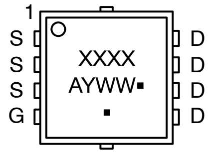
N−Channel MOSFET





WDFN8
(µ8FL)
CASE 511AB

MARKING DIAGRAM



4C08	= Specific Device Code for NVMTS4C08N
08WF	= Specific Device Code of NVTFS4C08NWF
A	= Assembly Location
Y	= Year
WW	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

August, 2019 − Rev. 1

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

OFF CHARACTERISTICS

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA		30			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$				13.8		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 24 V	T_J = 25°C			1.0	μA
			T_J = 125°C			10	
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V				±100	nA

ON CHARACTERISTICS (Note 5)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, I_D = 250 μA		1.3		2.2	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$				5.0		mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V	I_D = 30 A		4.7	5.9	mΩ
		V_{GS} = 4.5 V	I_D = 18 A		7.2	9.0	
Forward Transconductance	g_{FS}	V_{DS} = 1.5 V, I_D = 15 A			42		S
Gate Resistance	R_G	T_A = 25°C			1.0		Ω

CHARGES AND CAPACITANCES

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1 MHz, V_{DS} = 15 V		1113		pF
Output Capacitance	C_{OSS}			702		
Reverse Transfer Capacitance	C_{RSS}			39		
Capacitance Ratio	C_{RSS}/C_{ISS}	V_{GS} = 0 V, V_{DS} = 15 V, f = 1 MHz		0.035		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 4.5 V, V_{DS} = 15 V; I_D = 30 A		8.4		nC
Threshold Gate Charge	$Q_{G(TH)}$			1.8		
Gate−to−Source Charge	Q_{GS}			3.5		
Gate−to−Drain Charge	Q_{GD}			3.3		
Gate Plateau Voltage	V_{GP}			3.4		V
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DS} = 15 V; I_D = 30 A		18.2		nC

SWITCHING CHARACTERISTICS (Note 6)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = 4.5 V, V_{DS} = 15 V, I_D = 15 A, R_G = 3.0 Ω		9.0		ns
Rise Time	t_r			33		
Turn−Off Delay Time	$t_{d(OFF)}$			15		
Fall Time	t_f			4.0		
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = 10 V, V_{DS} = 15 V, I_D = 15 A, R_G = 3.0 Ω		7.0		ns
Rise Time	t_r			26		
Turn−Off Delay Time	$t_{d(OFF)}$			19		
Fall Time	t_f			3.0		

DRAIN−SOURCE DIODE CHARACTERISTICS

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 10 A	T_J = 25°C		0.79	1.1	V
			T_J = 125°C		0.66		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dIS/dt = 100 A/μs, I_S = 30 A			28.3		ns
Charge Time	t_a				14.5		
Discharge Time	t_b				13.8		
Reverse Recovery Charge	Q_{RR}				15.3		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
6. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

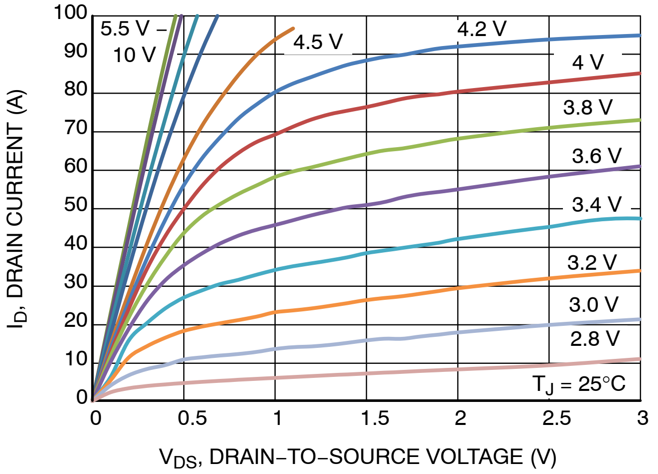


Figure 1. On−Region Characteristics

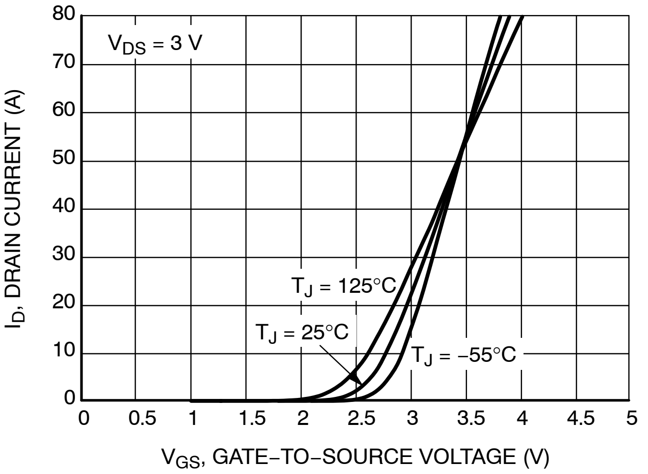


Figure 2. Transfer Characteristics

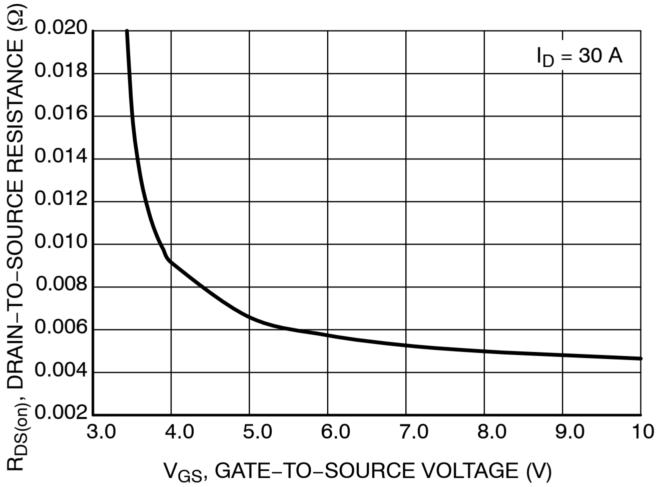


Figure 3. On−Resistance vs. V_{GS}

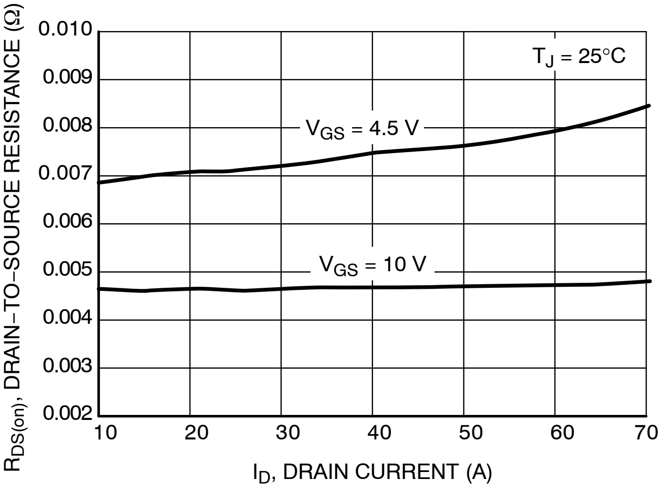


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

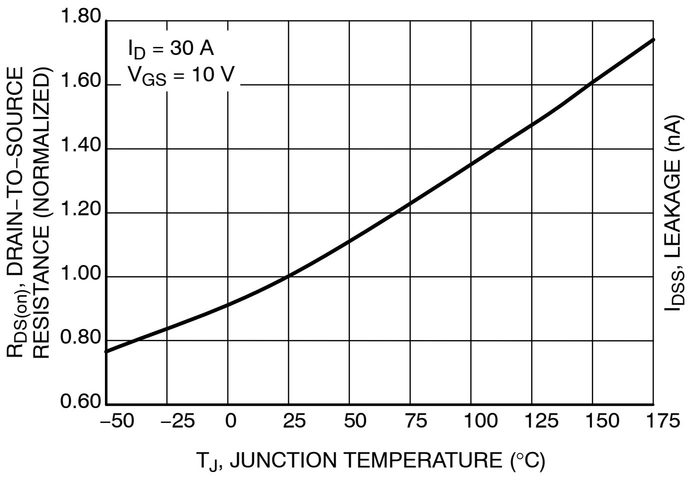


Figure 5. On−Resistance Variation with Temperature

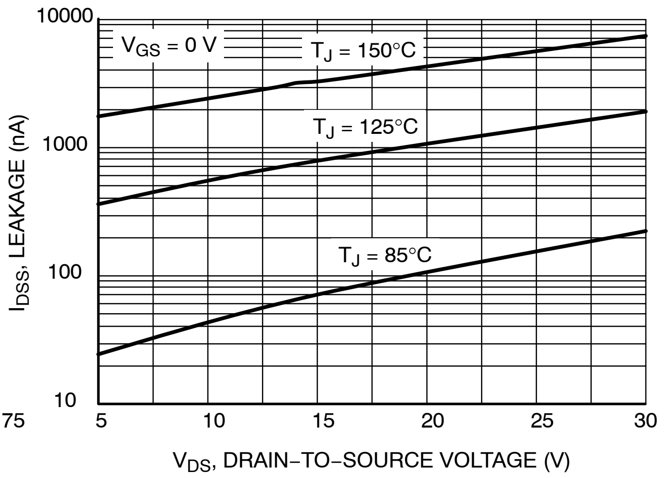


Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

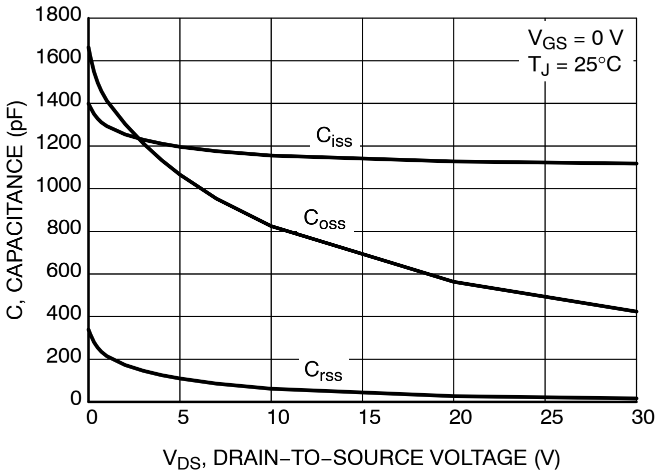


Figure 7. Capacitance Variation

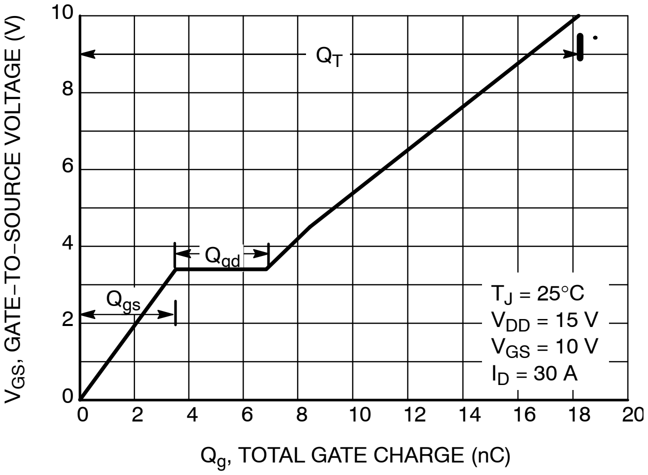


Figure 8. Gate−to−Source and Drain−to−Source Voltage vs. Total Charge

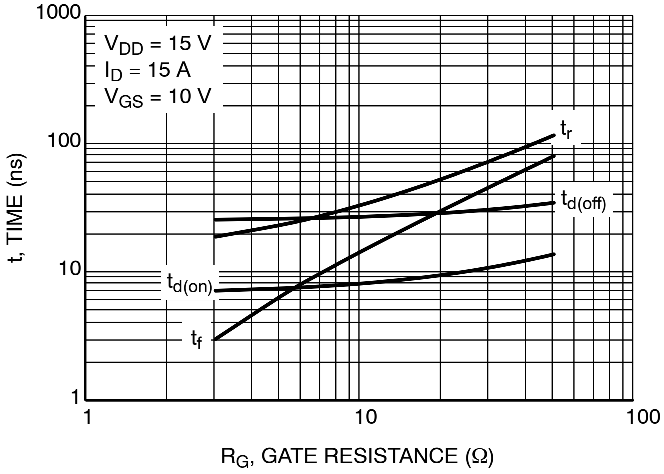


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

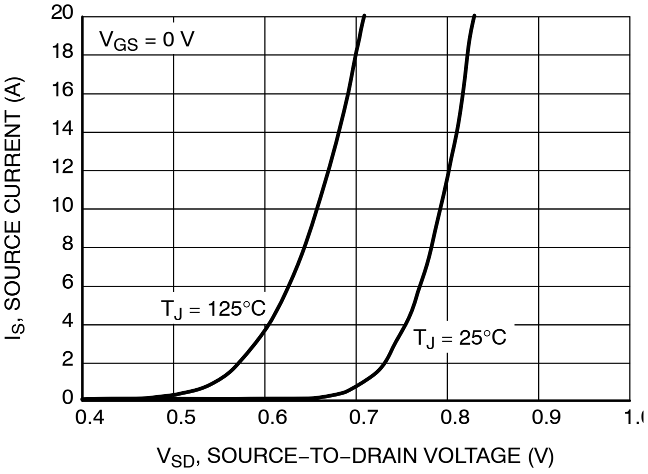


Figure 10. Diode Forward Voltage vs. Current

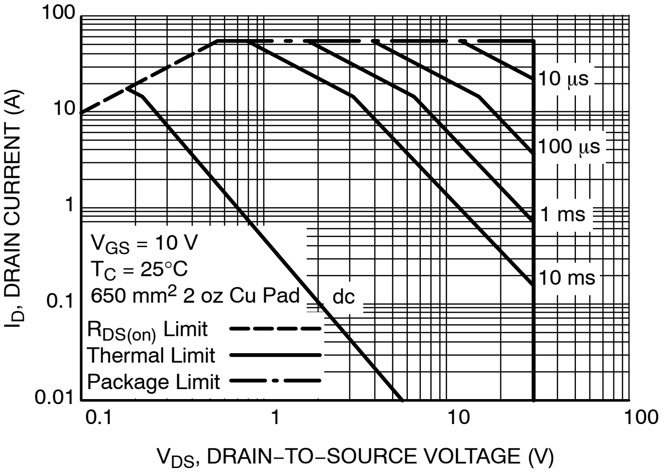


Figure 11. Maximum Rated Forward Biased Safe Operating Area

TYPICAL CHARACTERISTICS

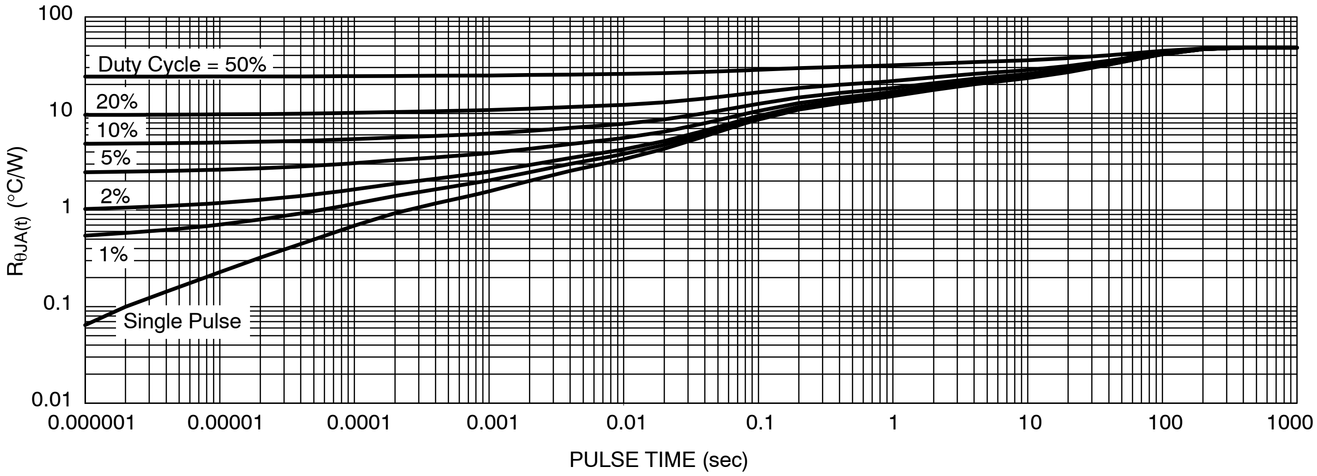


Figure 12. Thermal Response

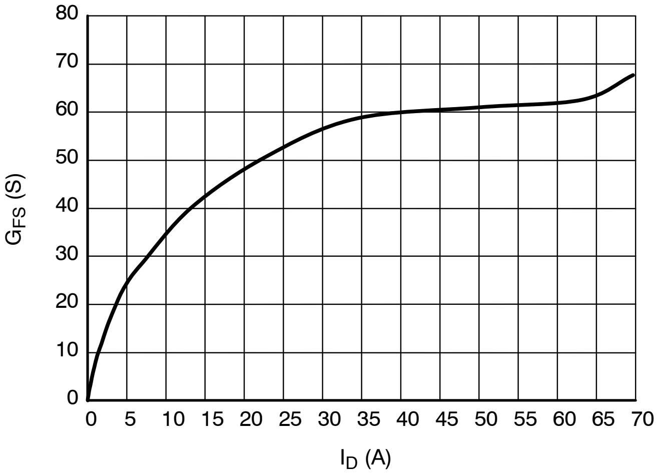


Figure 13. G_{FS} vs. I_D

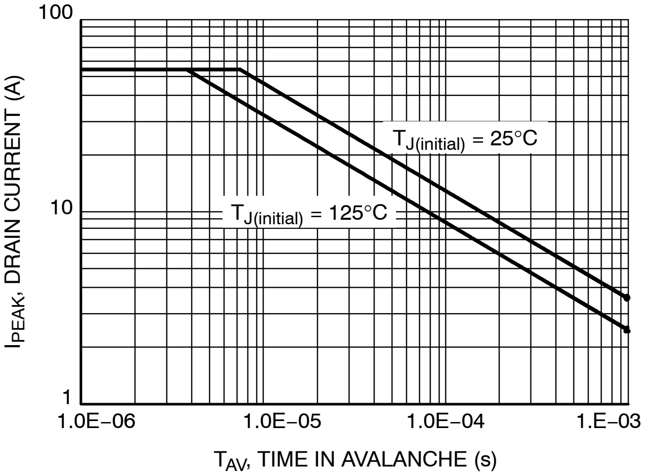


Figure 14. Avalanche Characteristics

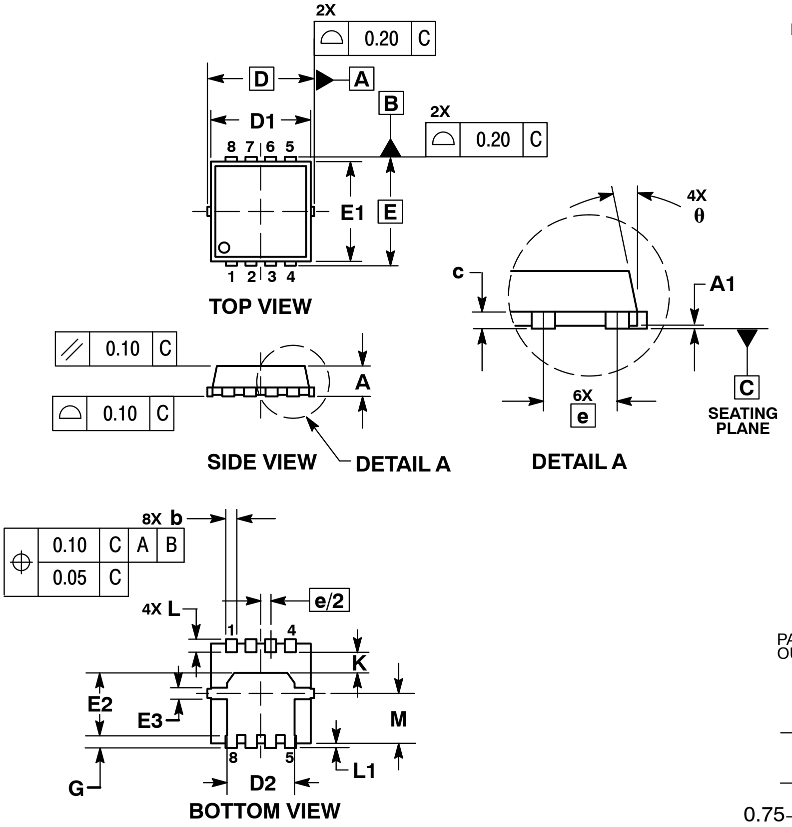
ORDERING INFORMATION

Device	Package	Shipping†
NVTFS4C08NTAG	WDFN8 (Pb−Free)	1500 / Tape & Reel
NVTFS4C08NWFTAG	WDFN8 (Pb−Free)	1500 / Tape & Reel
NVTFS4C08NTWG	WDFN8 (Pb−Free)	5000 / Tape & Reel
NVTFS4C08NWFTWG	WDFN8 (Pb−Free)	5000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

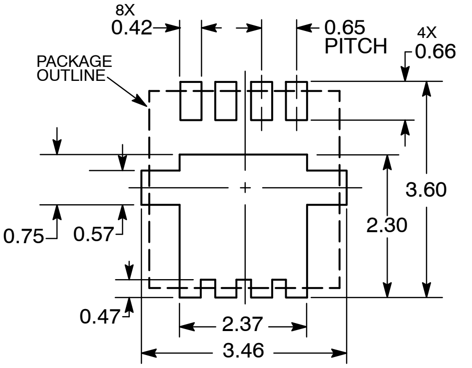
WDFN8 3.3x3.3, 0.65P
CASE 511AB
ISSUE D



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

	MILLIMETERS			INCHES		
DIM	**MIN**	**NOM**	**MAX**	**MIN**	**NOM**	**MAX**
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	---	0.05	0.000	---	0.002
b	0.23	0.30	0.40	0.009	0.012	0.016
c	0.15	0.20	0.25	0.006	0.008	0.010
D	3.30 BSC			0.130 BSC		
D1	2.95	3.05	3.15	0.116	0.120	0.124
D2	1.98	2.11	2.24	0.078	0.083	0.088
E	3.30 BSC			0.130 BSC		
E1	2.95	3.05	3.15	0.116	0.120	0.124
E2	1.47	1.60	1.73	0.058	0.063	0.068
E3	0.23	0.30	0.40	0.009	0.012	0.016
e	0.65 BSC			0.026 BSC		
G	0.30	0.41	0.51	0.012	0.016	0.020
K	0.65	0.80	0.95	0.026	0.032	0.037
L	0.30	0.43	0.56	0.012	0.017	0.022
L1	0.06	0.13	0.20	0.002	0.005	0.008
M	1.40	1.50	1.60	0.055	0.059	0.063
θ	0 °	---	12 °	0 °	---	12 °

SOLDERING FOOTPRINT*



DIMENSION: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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