



SFT1350

P-Channel Power MOSFET -40V, -19A, 59mΩ, Single TP/TP-FA

ON Semiconductor®

<http://onsemi.com>

Features

- ON-resistance $R_{DS(on)1}=45m\Omega$ (typ.)
- Input Capacitance $C_{iss}=590pF$ (typ.)
- 4.5V drive
- Halogen free compliance
- Protection diode in

Specifications

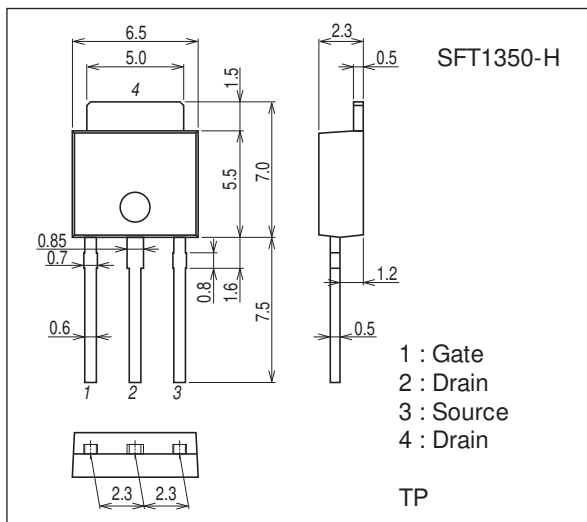
Absolute Maximum Ratings at $T_a=25^\circ C$

Parameter	Symbol	Conditions	Ratings	Unit
Drain-to-Source Voltage	V_{DSS}		-40	V
Gate-to-Source Voltage	V_{GSS}		± 20	V
Drain Current (DC)	I_D		-19	A
Drain Current (PW $\leq 10\mu s$)	I_{DP}	PW $\leq 10\mu s$, duty cycle $\leq 1\%$	-76	A
Allowable Power Dissipation	P_D		1.0	W
		$T_c=25^\circ C$	23	W
Channel Temperature	T_{ch}		150	$^\circ C$
Storage Temperature	T_{stg}		-55 to +150	$^\circ C$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

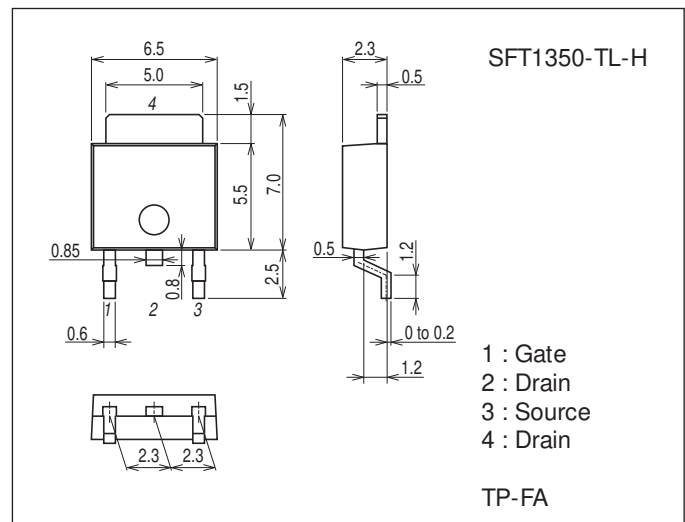
Package Dimensions unit : mm (typ)

7518-004



Package Dimensions unit : mm (typ)

7003-004

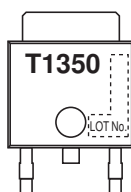


Product & Package Information

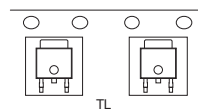
- Package : TP
- JEITA, JEDEC : SC-64, TO-251
- Minimum Packing Quantity : 500 pcs./bag

- Package : TP-FA
- JEITA, JEDEC : SC-63, TO-252
- Minimum Packing Quantity : 700 pcs./reel

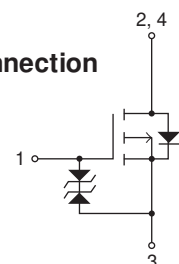
Marking (TP, TP-FA)



Packing Type (TP-FA) : TL



Electrical Connection

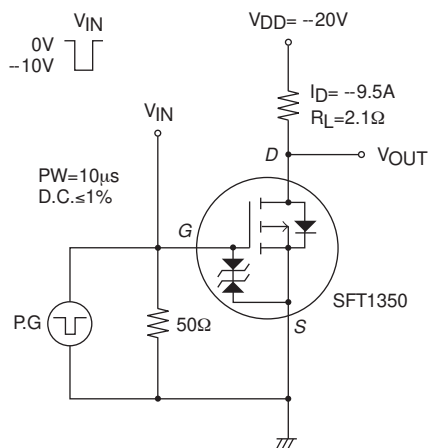


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Electrical Characteristics at Ta=25°C

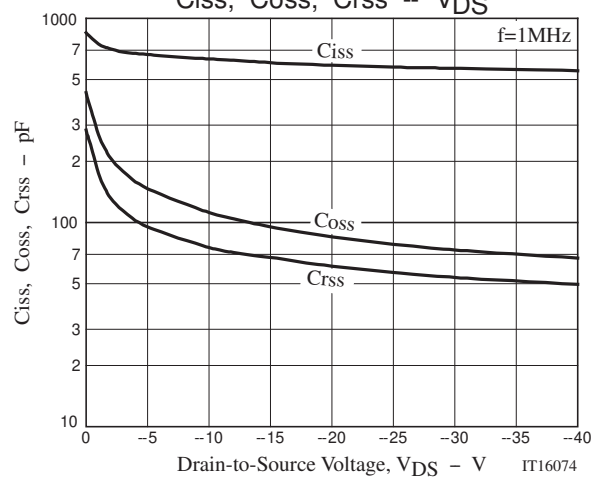
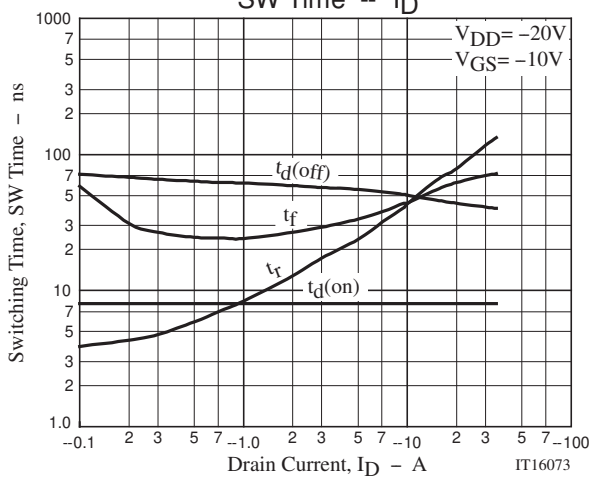
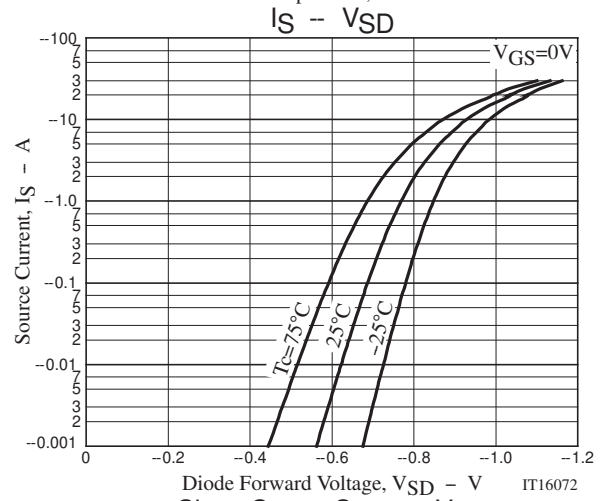
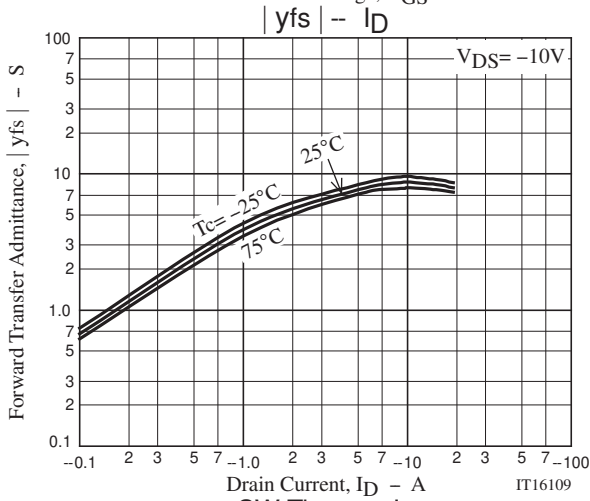
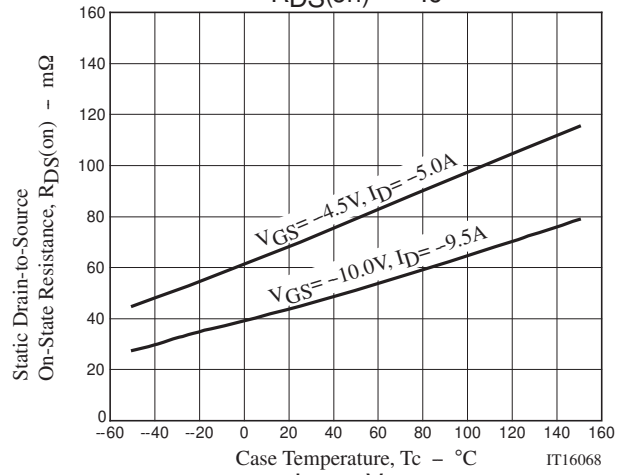
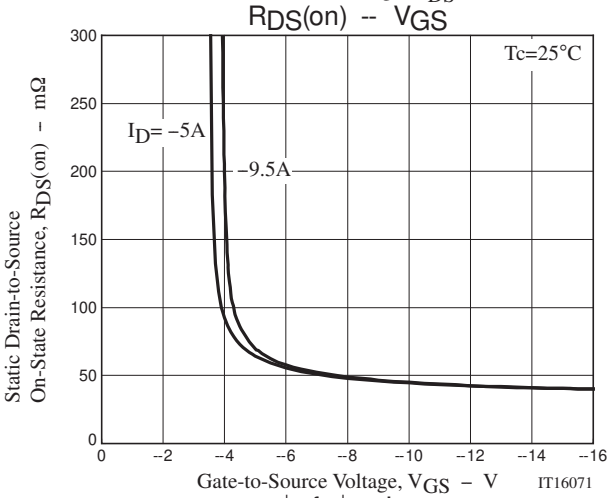
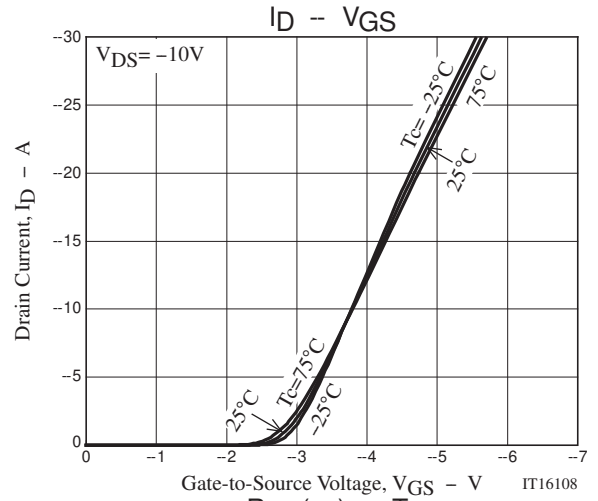
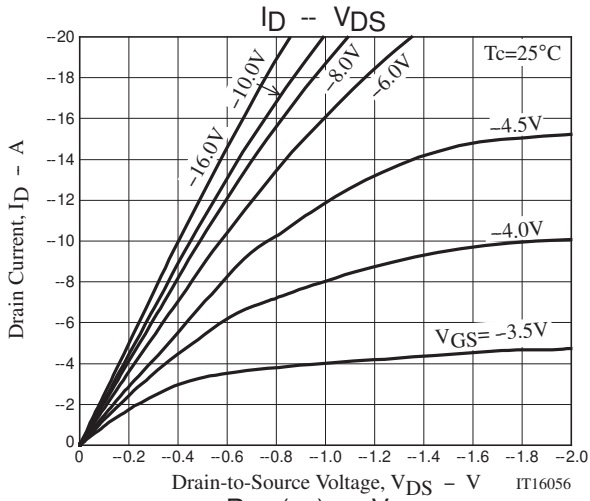
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$I_D = -1\text{mA}$, $V_{GS} = 0\text{V}$	-40			V
Zero-Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -40\text{V}$, $V_{GS} = 0\text{V}$			-1	μA
Gate-to-Source Leakage Current	I_{GSS}	$V_{GS} = \pm 16\text{V}$, $V_{DS} = 0\text{V}$			± 10	μA
Cutoff Voltage	$V_{GS(off)}$	$V_{DS} = -10\text{V}$, $I_D = -1\text{mA}$	-1.7		-2.6	V
Forward Transfer Admittance	$ y_{fs} $	$V_{DS} = -10\text{V}$, $I_D = -9.5\text{A}$		8.7		S
Static Drain-to-Source On-State Resistance	$R_{DS(on)1}$	$I_D = -9.5\text{A}$, $V_{GS} = -10\text{V}$		45	59	$\text{m}\Omega$
	$R_{DS(on)2}$	$I_D = -5\text{A}$, $V_{GS} = -4.5\text{V}$		73	105	$\text{m}\Omega$
Input Capacitance	C_{iss}	$V_{DS} = -20\text{V}$, $f = 1\text{MHz}$		590		pF
Output Capacitance	C_{oss}			85		pF
Reverse Transfer Capacitance	C_{rss}			61		pF
Turn-ON Delay Time	$t_{d(on)}$	See specified Test Circuit.		8		ns
Rise Time	t_r			40		ns
Turn-OFF Delay Time	$t_{d(off)}$			52		ns
Fall Time	t_f			44		ns
Total Gate Charge	Q_g	$V_{DS} = -20\text{V}$, $V_{GS} = -10\text{V}$, $I_D = -19\text{A}$		12		nC
Gate-to-Source Charge	Q_{gs}			3.6		nC
Gate-to-Drain "Miller" Charge	Q_{gd}			2.0		nC
Diode Forward Voltage	V_{SD}	$I_S = -19\text{A}$, $V_{GS} = 0\text{V}$		-1.03	-1.2	V

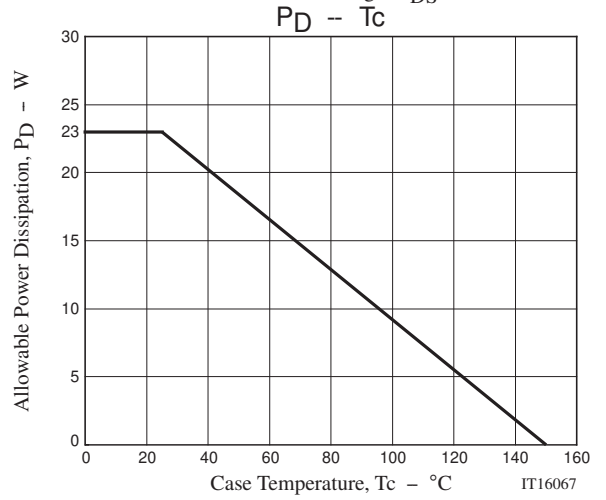
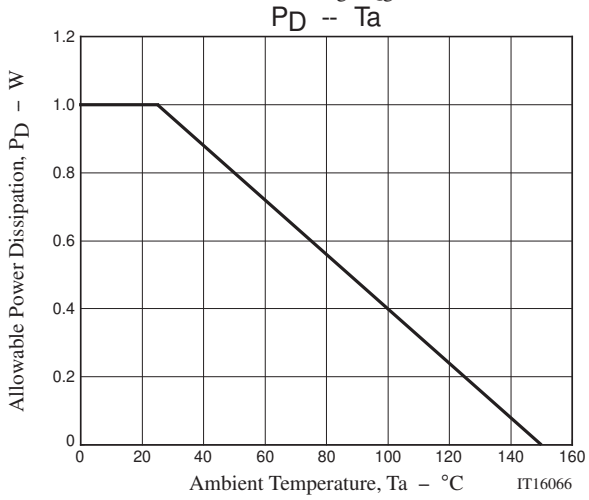
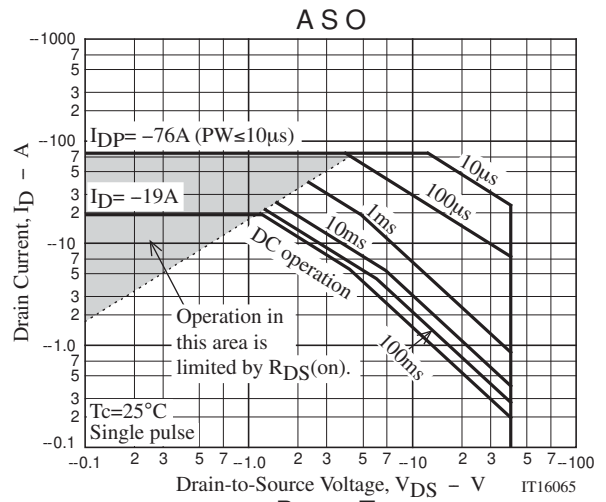
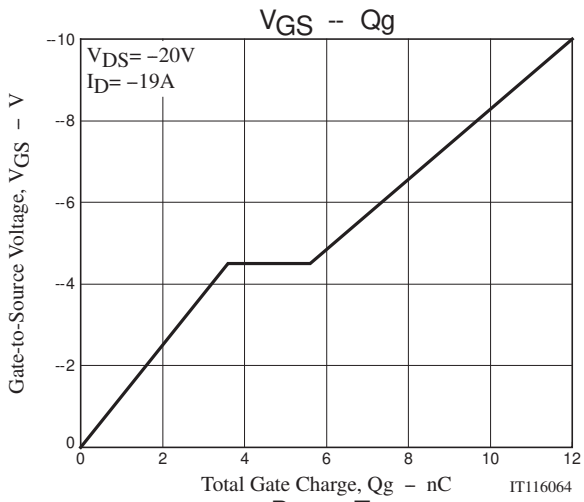
Switching Time Test Circuit



Ordering Information

Device	Package	Shipping	memo
SFT1350-H	TP	500pcs./bag	Pb Free and Halogen Free
SFT1350-TL-H	TP-FA	700pcs./reel	





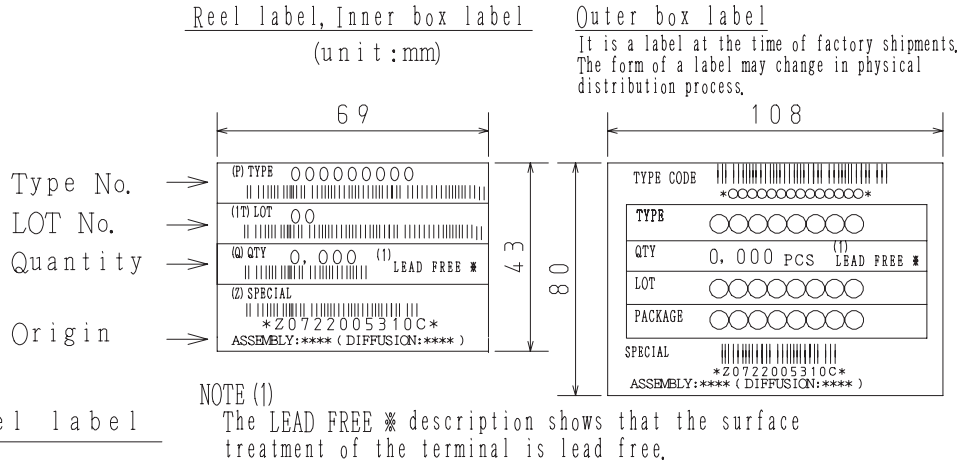
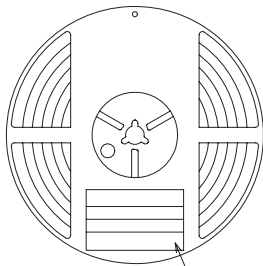
Taping Specification

SFT1350-TL-H

Packing Format

Package Name	Carrier Tape Type	Maximum Number of devices contained (pcs)			Packing format	
		Reel	Inner box	Outer box	Inner BOX (C-1)	Outer BOX (A-7)
TP-FA	TP	700	2,100	12,600	3 reels contained Dimensions:mm (external) 183×72×185	6 inner boxes contained Dimensions:mm (external) 440×195×210

Packing method

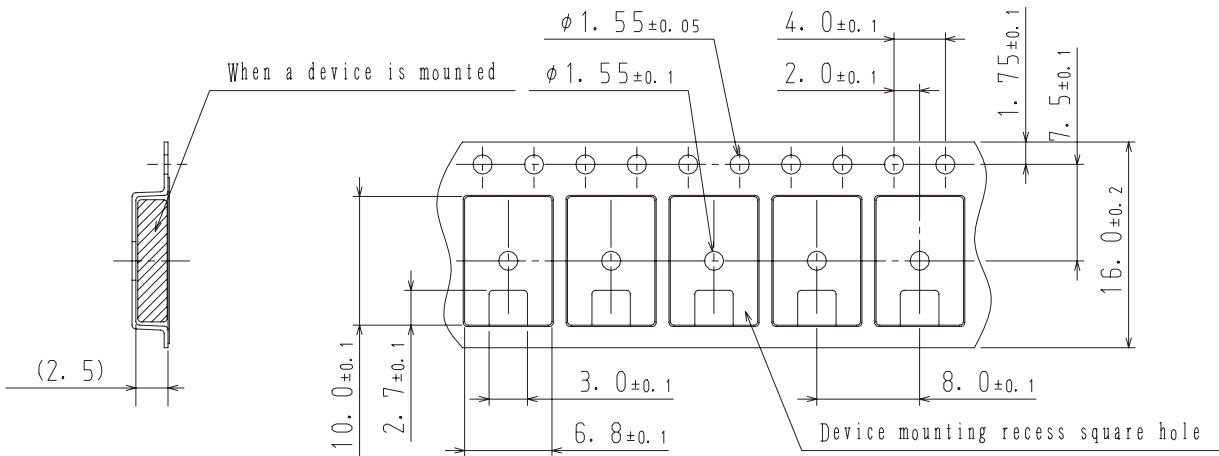


NOTE (1)
The LEAD FREE * description shows that the surface treatment of the terminal is lead free.

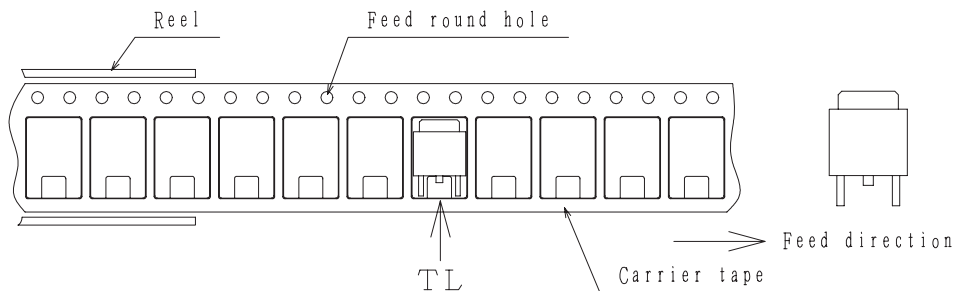
Label	JEITA Phase
LEAD FREE 3	JEITA Phase 3A
LEAD FREE 4	JEITA Phase 3

Taping configuration

1. Carrier tape size (unit:mm)



2. Device placement direction

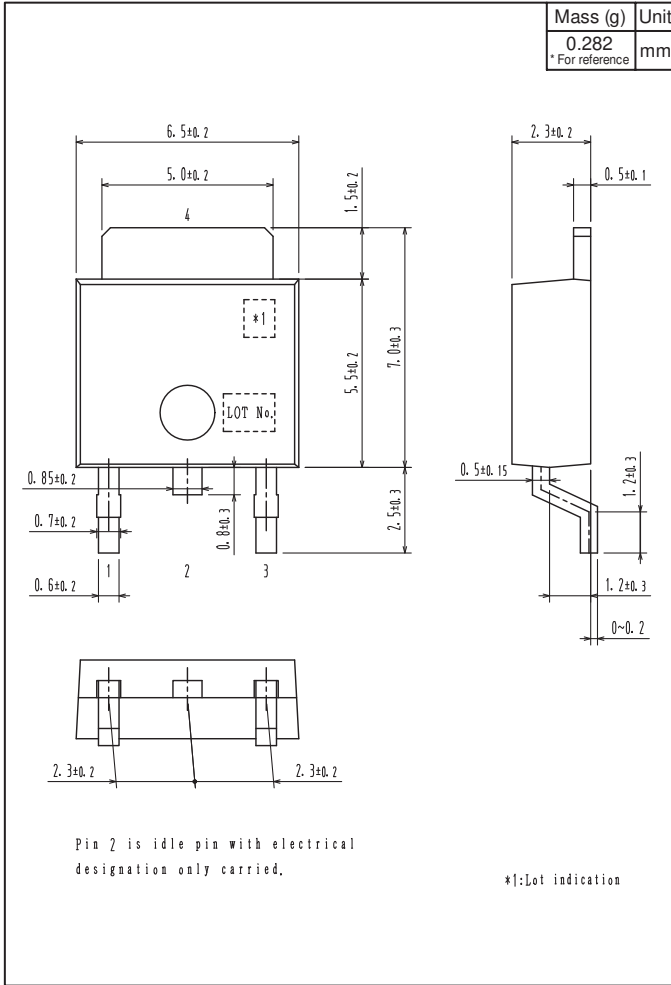


Those with one electrode terminal on the feed hole side.....TL

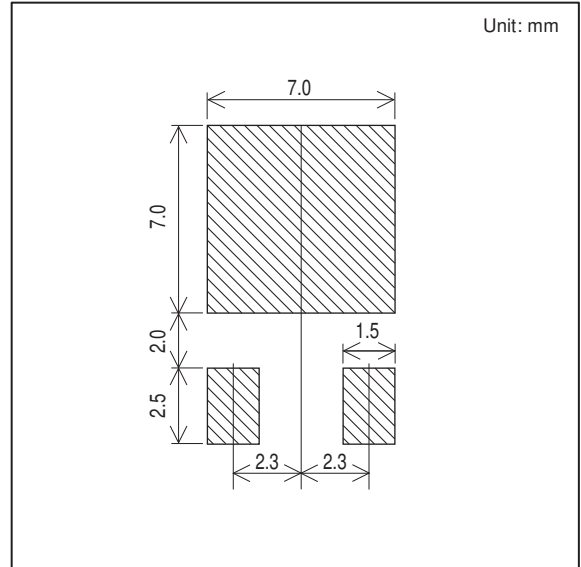
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Outline Drawing

SFT1350-TL-H



Land Pattern Example



SFT1350

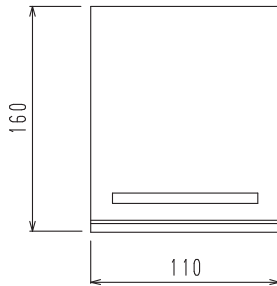
Bag Packing Specification

SFT1350-H

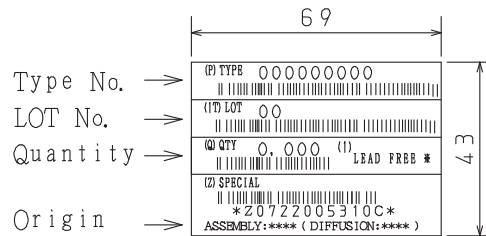
1. Packing Format

Package Name	Maximum Number of devices contained (pcs)			
	Bag	Inner box	Outer box	
TP	500	B-1	A-1	A-2
		10,000	50,000	30,000
Packing format (Dimensions:mm (external))				
		Inner box	Outer box	
		B-1	A-1	A-2
		445×225×55	470×250×300	470×250×190

2. Bag dimensions (unit:mm)



3. Bag label, Inner box label (unit:mm)



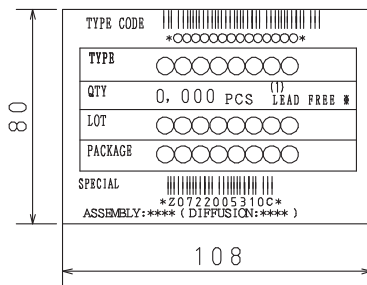
4. Outer box label (unit:mm)

It is a label at the time of factory shipments.
The form of a label may change in physical
distribution process.

NOTE (1)

The LEAD FREE * description shows that the
surface treatment of the terminal is lead free.

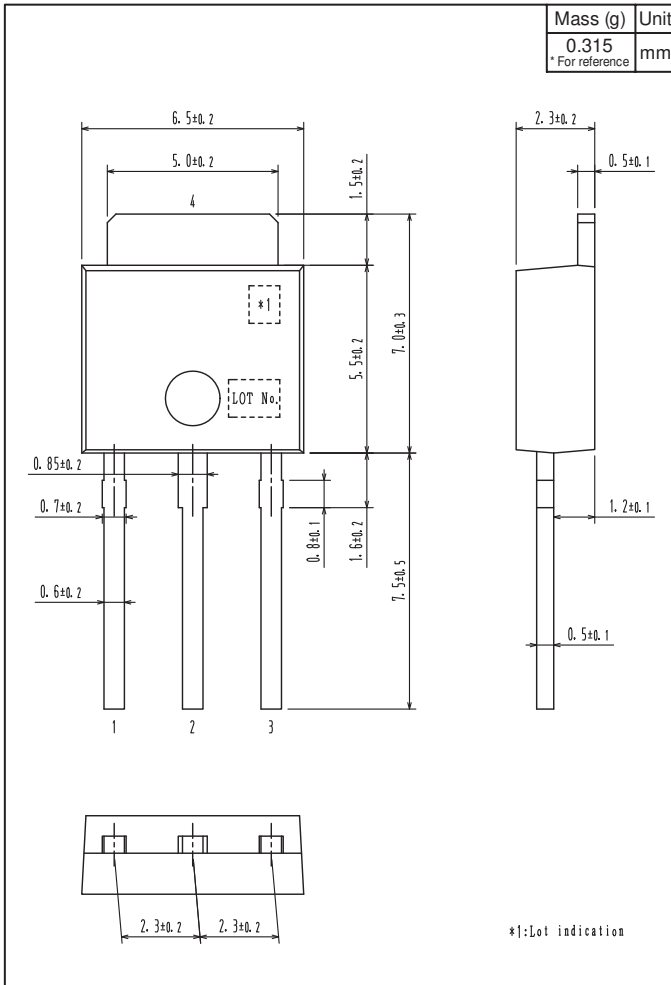
Label	JEITA Phase
LEAD FREE 3	JEITA Phase 3A
LEAD FREE 4	JEITA Phase 3



SFT1350

Outline Drawing

SFT1350-H



Note on usage : Since the SFT1350 is a MOSFET product, please avoid using this device in the vicinity of highly charged objects.

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