RJK0452DPB

40V, 45A, 3.5mΩ max.
Silicon N Channel Power MOS FET
Power Switching
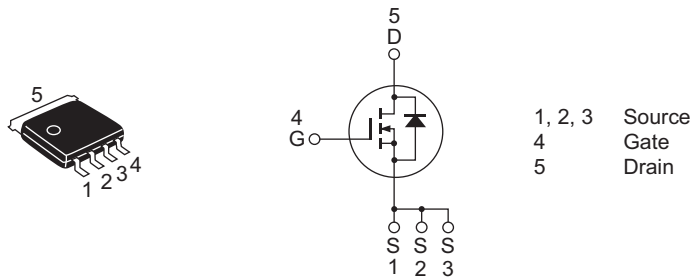
Features

- High speed switching
- Capable of 4.5 V gate drive
- Low drive current
- High density mounting

- Low on-resistance
  $R_{DS(on)} = 2.8$ mΩ typ. (at $V_{GS} = 10$ V)
- Pb-free
- Halogen-free

Outline

RENESAS Package code: PTZZ0005DA-A
(Package name: LFPAK)

1, 2, 3	Source
4	Gate
5	Drain

Application

- Switching Mode Power Supply

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	40	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	45	A
Drain peak current	$I_{D(pulse)}$ [Note1]	180	A
Body-drain diode reverse drain current	I_{DR}	45	A
Avalanche current	I_{AP} [Note 2]	22.5	A
Avalanche energy	E_{AS} [Note 2]	40.5	mJ
Channel dissipation	Pch [Note3]	55	W
Channel to Case Thermal Resistance	θch-C	2.27	°C/W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	−55 to +150	°C

Notes: 1. PW ≤ 10 μs, duty cycle ≤ 1%

2. Value at Tch = 25°C, Rg ≥ 50 Ω

3. Tc = 25°C

This product is for the low voltage drive (≤ 10V).

If the driving voltage is over 10 V under normal conditions, please use the product for high gate to source cutoff voltage ($V_{GS(off)}$) which characteristics has been improved.
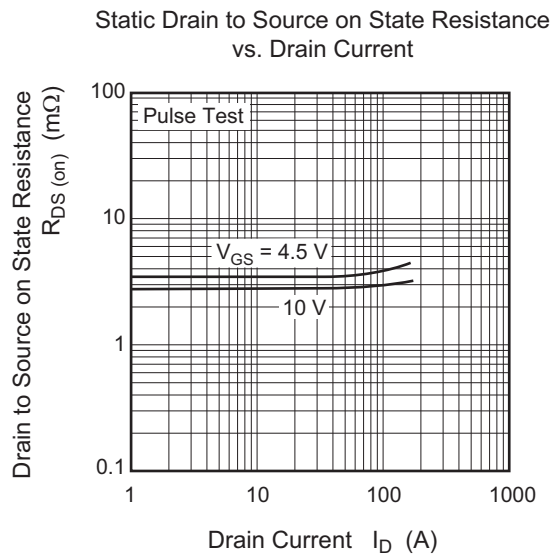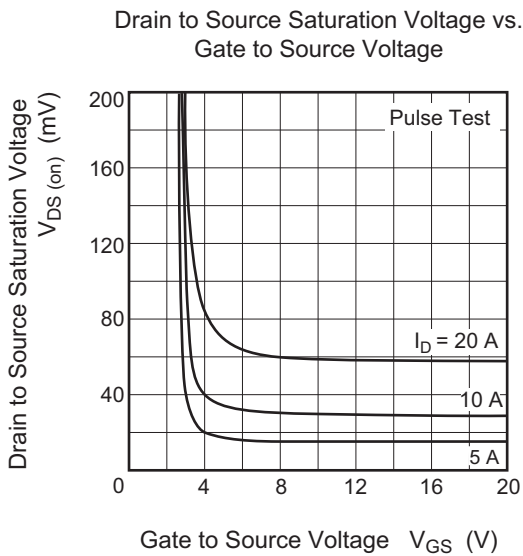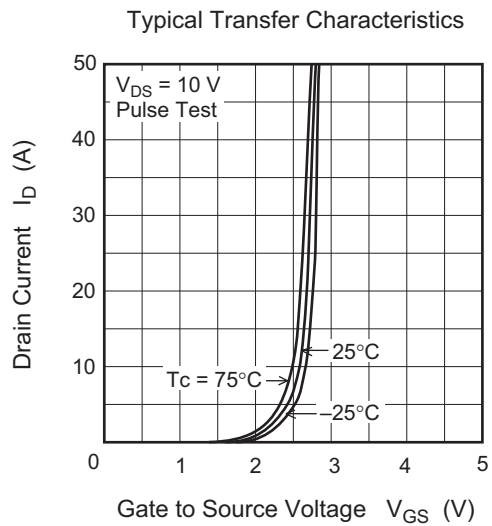
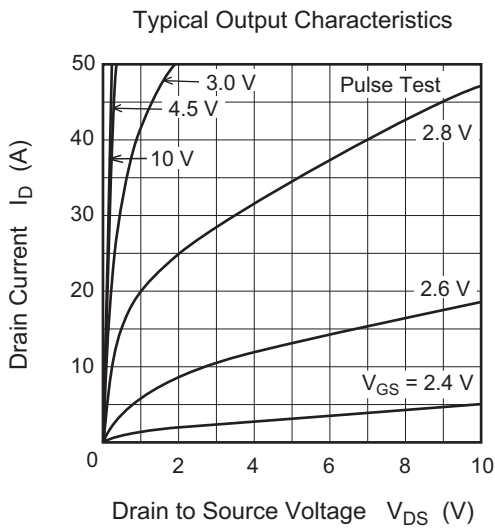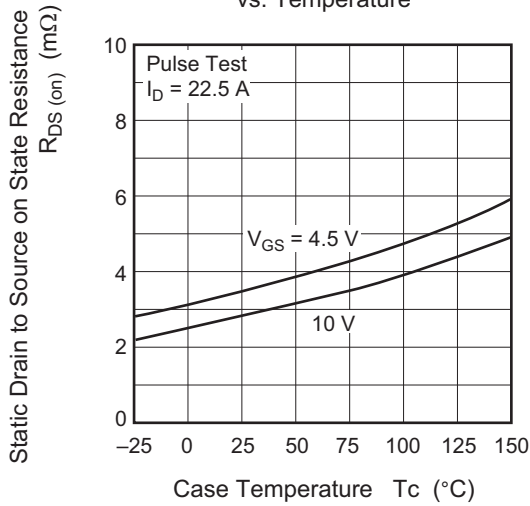## Electrical Characteristics

(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	40	—	—	V	I_D = 10 mA, V_{GS} = 0 V
Gate to source leak current	I_{GSS}	—	—	±0.1	μA	V_{GS} = ±20 V, V_{DS} = 0 V
Zero gate voltage drain current	I_{DSS}	—	—	1	μA	V_{DS} = 40 V, V_{GS} = 0 V
Gate to source cutoff voltage	$V_{GS(off)}$	1.2	—	2.5	V	V_{DS} = 10 V, I_D = 1 mA
Static drain to source on state resistance	$R_{DS(on)}$	—	2.8	3.5	mΩ	I_D = 22.5 A, V_{GS} = 10 V [Note4]
	$R_{DS(on)}$	—	3.5	4.7	mΩ	I_D = 22.5 A, V_{GS} = 4.5 V [Note4]
Forward transfer admittance	$|y_{fs}|$	—	108	—	S	I_D = 22.5 A, V_{DS} = 10 V [Note4]
Input capacitance	Ciss	—	4030	—	pF	V_{DS} = 10 V, V_{GS} = 0 V,
Output capacitance	Coss	—	650	—	pF	f = 1 MHz
Reverse transfer capacitance	Crss	—	270	—	pF	
Gate Resistance	Rg	—	0.4	—	Ω	
Total gate charge	Qg	—	26	—	nC	V_{DD} = 10 V, V_{GS} = 4.5 V,
Gate to source charge	Qgs	—	12	—	nC	I_D = 45 A
Gate to drain charge	Qgd	—	6.6	—	nC	
Turn-on delay time	$t_{d(on)}$	—	18	—	ns	V_{GS} = 10 V, I_D = 22.5 A,
Rise time	t_r	—	6.0	—	ns	V_{DD} ≅ 10 V, R_L = 0.44 Ω,
Turn-off delay time	$t_{d(off)}$	—	65	—	ns	Rg = 4.7 Ω
Fall time	t_f	—	8.5	—	ns	
Body–drain diode forward voltage	V_{DF}	—	0.83	1.1	V	I_F = 45 A, V_{GS} = 0 V [Note4]
Body–drain diode reverse recovery time	t_{rr}	—	35	—	ns	I_F = 45 A, V_{GS} = 0 V di_F/ dt = 100 A/ μs

Notes: 4. Pulse test

Main Characteristics

Power vs. Temperature Derating

Maximum Safe Operation Area

Typical Output Characteristics

Typical Transfer Characteristics

Drain to Source Saturation Voltage vs. Gate to Source Voltage

Static Drain to Source on State Resistance vs. Drain Current

RENESAS
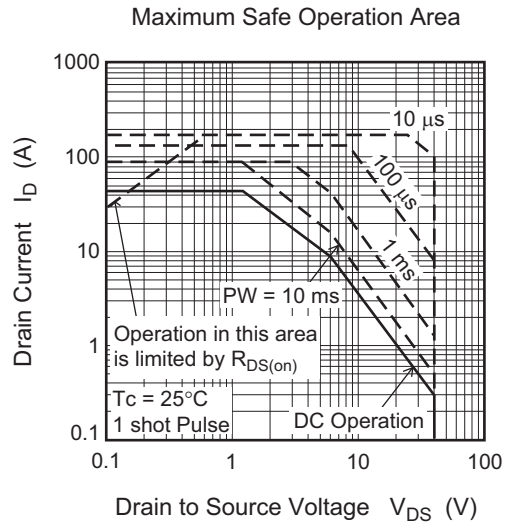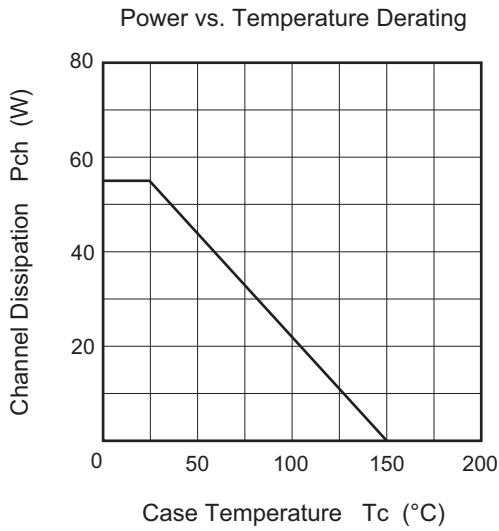
Static Drain to Source on State Resistance vs. Temperature

Pulse Test
I_D = 22.5 A

V_{GS} = 4.5 V

10 V

Static Drain to Source on State Resistance $R_{DS\,(on)}$ (mΩ)

Case Temperature Tc (°C)

Typical Capacitance vs. Drain to Source Voltage

Ciss

Coss

Crss

V_{GS} = 0 V
f = 1 MHz

Capacitance C (pF)

Drain to Source Voltage V_{DS} (V)
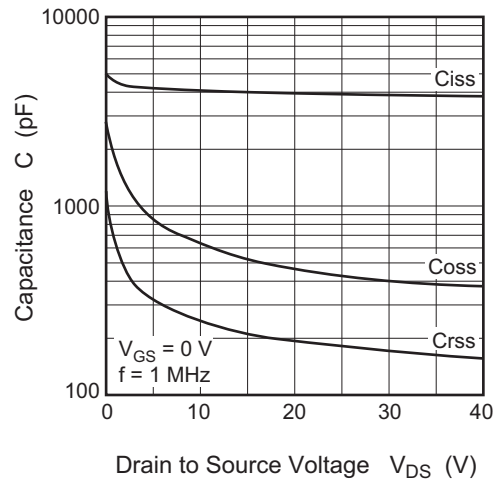
Dynamic Input Characteristics

I_D = 45 A

V_{GS}

V_{DD} = 25 V
10 V

V_{DS}

V_{DD} = 25 V
10 V

Drain to Source Voltage V_{DS} (V)

Gate to Source Voltage V_{GS} (V)

Gate Charge Qg (nC)
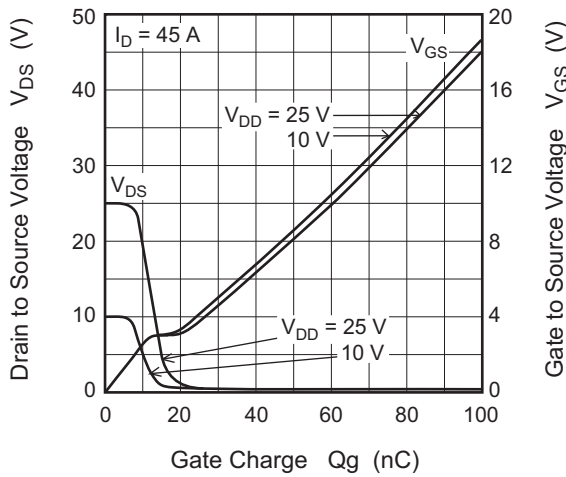
Reverse Drain Current vs. Source to Drain Voltage

Pulse Test

10 V

5 V

V_{GS} = 0

Reverse Drain Current I_{DR} (A)

Source to Drain Voltage V_{SD} (V)
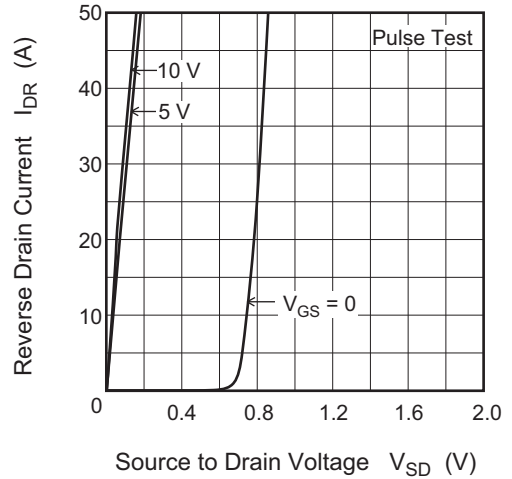
Maximum Avalanche Energy vs. Channel Temperature Derating

I_{AP} = 22.5 A
V_{DD} = 15 V
duty < 0.1 %
Rg ≥ 50 Ω

Avalanche Energy E_{AS} (mJ)

Channel Temperature Tch (°C)
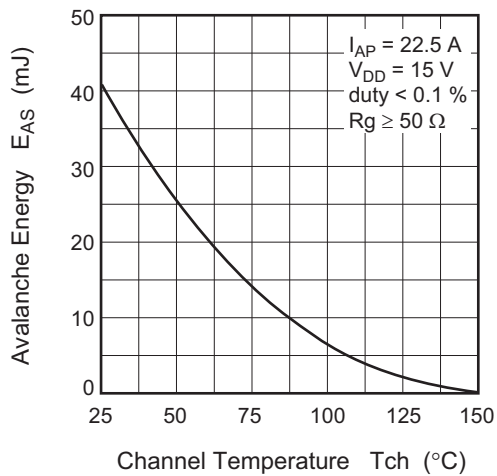
Normalized Transient Thermal Impedance vs. Pulse Width

Normalized Transient Thermal Impedance γs (t)

Tc = 25°C

D = 1
0.5
0.2
0.1
0.05
0.02
0.01
1shot pulse

θch $-$ c (t) = γ s (t) $\bullet$ θch $-$ c
θch $-$ c = 2.27°C/W, Tc = 25°C

P_{DM}

$D = \dfrac{PW}{T}$

PW
T

Pulse Width PW (s)

Avalanche Test Circuit

V_{DS} Monitor

L

I_{AP} Monitor

Rg

D. U. T

V_{DD}

Vin 15 V

50 Ω

Avalanche Waveform

$$E_{AS} = \frac{1}{2} \; L \bullet I_{AP}{}^2 \bullet \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$

I_{AP}

$V_{(BR)DSS}$

V_{DS}

I_D

V_{DD}

0
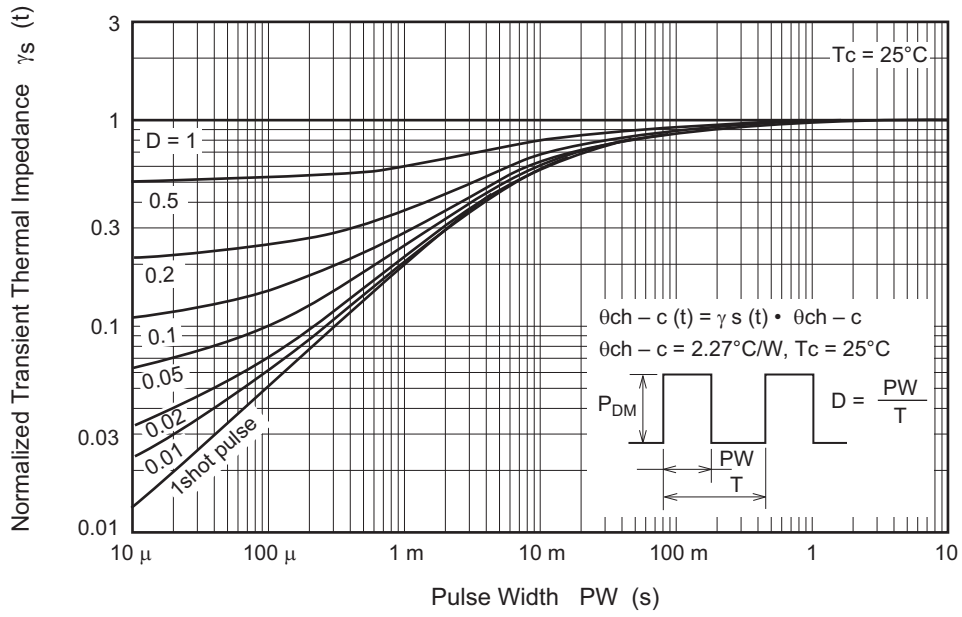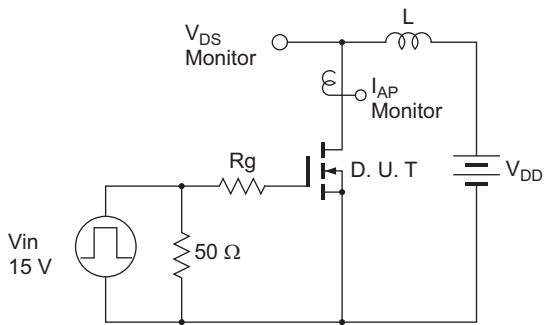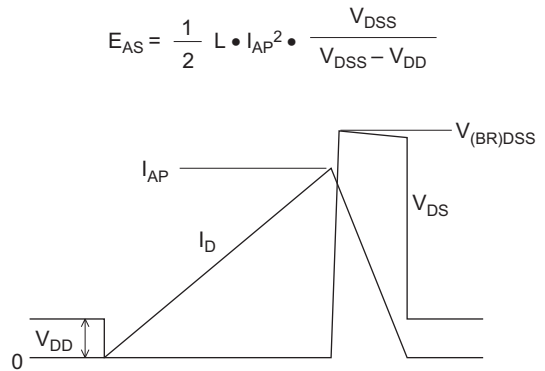
Switching Time Test Circuit

Vin Monitor

Vout Monitor

Rg

D.U.T.

R_L

Vin 10 V

V_{DS} 10 V
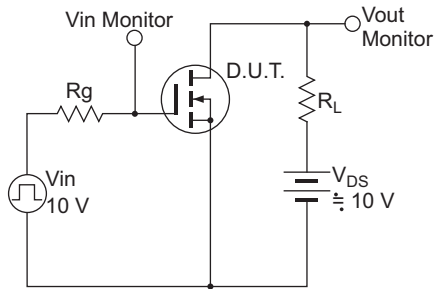
Switching Time Waveform

90%

Vin
10%

Vout
10%
10%

90%
90%

$t_{d(on)}$ t_r $t_{d(off)}$ t_f

Package Dimensions

Package Name	JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]	
LFPAK	SC-100	PTZZ0005DA-A	LFPAKV	0.080g	Unit: mm

(Ni/Pd/Au plating)
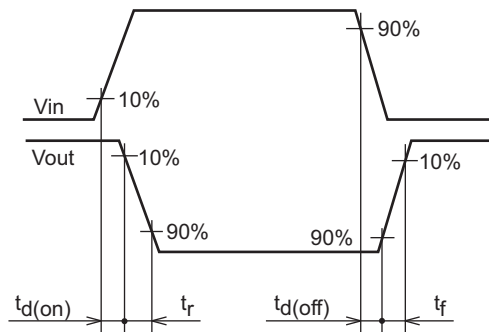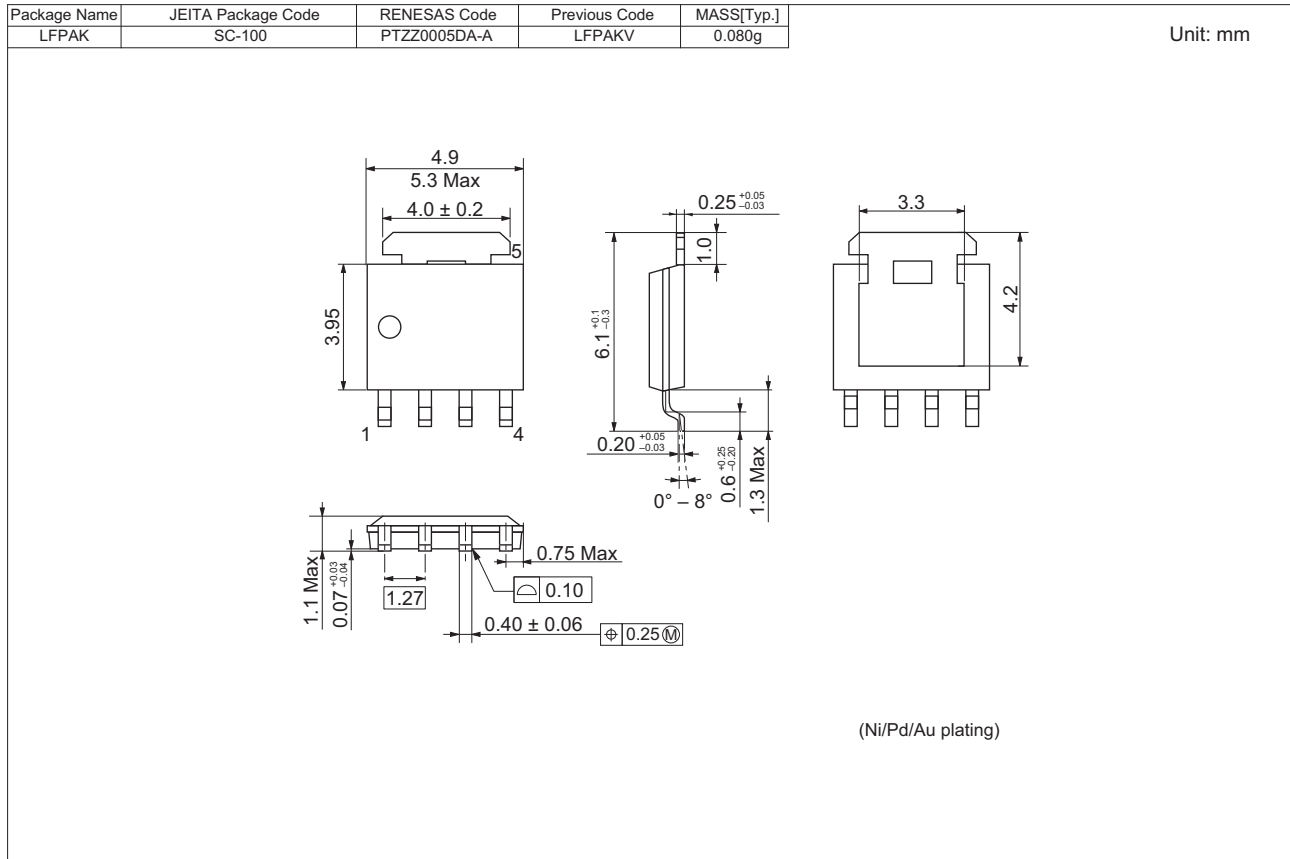
Ordering Information

Part No.	Quantity	Shipping Container
RJK0452DPB-00-J5	2500 pcs	Taping

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