

N-channel 600 V, 0.092 Ω , 31.5 A MDmesh™ II Power MOSFETs in D²PAK and TO-220 packages

Datasheet - production data

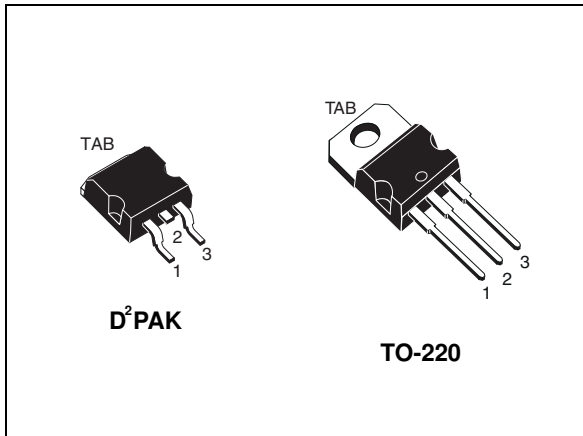
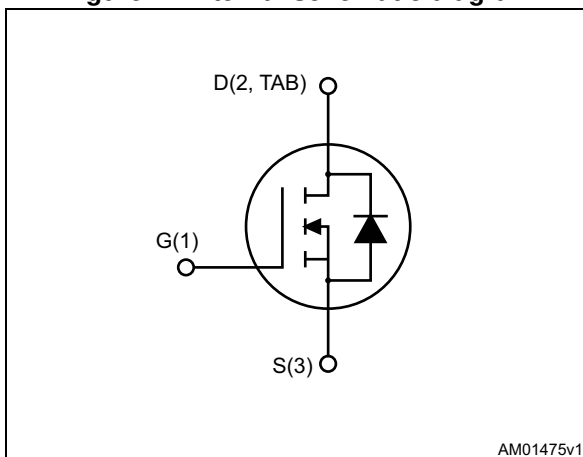


Figure 1. Internal schematic diagram



Features

| Order codes | V _{DSS} | R _{DS(on)} | I _D | P _{TOT} |
|-------------|------------------|---------------------|----------------|------------------|
| STB34NM60N | 600 V | 0.105 Ω | 31.5 A | 250 W |
| STP34NM60N | | | | |

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

Applications

- Switching applications

Description

These devices are N-channel Power MOSFETs developed using the second generation of MDmesh™ technology. This revolutionary Power MOSFET associates a vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters.

Table 1. Device summary

| Order codes | Marking | Packages | Packaging |
|-------------|---------|--------------------|---------------|
| STB34NM60N | 34NM60N | D ² PAK | Tape and reel |
| STP34NM60N | | TO-220 | Tube |

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1 Electrical ratings

Table 2. Absolute maximum ratings

| Symbol | Parameter | Value | Unit |
|----------------|--|------------|------------------|
| V_{DS} | Drain-source voltage | 600 | V |
| V_{GS} | Gate-source voltage | ± 25 | V |
| I_D | Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$ | 31.5 | A |
| I_D | Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$ | 20 | A |
| $I_{DM}^{(1)}$ | Drain current (pulsed) | 126 | A |
| P_{TOT} | Total dissipation at $T_C = 25\text{ }^\circ\text{C}$ | 250 | W |
| I_{AR} | Max current during repetitive or single pulse avalanche (pulse width limited by T_{jmax}) | 7 | A |
| E_{AS} | Single pulse avalanche energy (starting $T_J = 25\text{ }^\circ\text{C}$, $I_D = I_{AS}$, $V_{DD} = 50\text{ V}$) | 345 | mJ |
| $dv/dt^{(2)}$ | Peak diode recovery voltage slope | 15 | V/ns |
| $dv/dt^{(3)}$ | MOSFET dv/dt ruggedness | 50 | V/ns |
| T_{stg} | Storage temperature | -55 to 150 | $^\circ\text{C}$ |
| T_j | Max. operating junction temperature | 150 | $^\circ\text{C}$ |

1. Pulse width limited by safe operating area.
2. $I_{SD} \leq 31.5\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$, $V_{DS\text{ peak}} \leq V_{(BR)DSS}$, $V_{DD} = 80\% V_{(BR)DSS}$
3. $V_{DS} \leq 480\text{ V}$

Table 3. Thermal data

| Symbol | Parameter | Value | | Unit |
|---------------------|--------------------------------------|--------------------|--------|---------------------------|
| | | D ² PAK | TO-220 | |
| $R_{thj-case}$ | Thermal resistance junction-case max | 0.5 | | $^\circ\text{C}/\text{W}$ |
| $R_{thj-amb}$ | Thermal resistance junction-amb max | | 62.5 | |
| $R_{thj-pcb}^{(1)}$ | Thermal resistance junction-pcb max | 30 | | |

1. When mounted on 1 inch² FR-4, 2 Oz copper board.

2 Electrical characteristics

($T_{CASE} = 25\text{ °C}$ unless otherwise specified).

Table 4. On/off states

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---------------|--|---|------|-------|-----------|--------------------------------|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage ($V_{GS} = 0$) | $I_D = 1\text{ mA}$ | 600 | | | V |
| I_{DSS} | Zero gate voltage drain current ($V_{GS} = 0$) | $V_{DS} = 600\text{ V}$ $V_{DS} = 600\text{ V}, T_c = 125\text{ °C}$ | | | 1 100 | μA μA |
| I_{GSS} | Gate body leakage current ($V_{DS} = 0$) | $V_{GS} = \pm 25\text{ V}$ | | | ± 100 | nA |
| $V_{GS(th)}$ | Gate threshold voltage | $V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$ | 2 | 3 | 4 | V |
| $R_{DS(on)}$ | Static drain-source on-resistance | $V_{GS} = 10\text{ V}, I_D = 14.5\text{ A}$ | | 0.092 | 0.105 | Ω |

Table 5. Dynamic

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|----------------------------|-------------------------------------|--|------|------|------|----------|
| C_{iss} | Input capacitance | $V_{DS} = 100\text{ V}, f = 1\text{ MHz}, V_{GS} = 0$ | - | 2722 | - | pF |
| C_{oss} | Output capacitance | | - | 173 | - | pF |
| C_{rss} | Reverse transfer capacitance | | - | 1.75 | - | pF |
| $C_{oss\text{ eq.}}^{(1)}$ | Equivalent capacitance time related | $V_{GS} = 0, V_{DS} = 0\text{ to }480\text{ V}$ | - | 458 | - | pF |
| $t_{d(on)}$ | Turn-on delay time | $V_{DD} = 300\text{ V}, I_D = 15.75\text{ A},$ $R_G = 4.7\text{ }\Omega, V_{GS} = 10\text{ V}$ (see Figure 19 and 14) | - | 18 | - | ns |
| t_r | Rise time | | - | 36 | - | ns |
| $t_{d(off)}$ | Turn-off delay time | | - | 104 | - | ns |
| t_f | Fall time | | - | 73 | - | ns |
| Q_g | Total gate charge | $V_{DD} = 480\text{ V}, I_D = 31.5\text{ A}$ $V_{GS} = 10\text{ V}$ (see Figure 15) | - | 84 | - | nC |
| Q_{gs} | Gate-source charge | | - | 14 | - | nC |
| Q_{gd} | Gate-drain charge | | - | 45 | - | nC |
| R_G | Intrinsic gate resistance | $f = 1\text{ MHz},$ gate DC Bias=0 test signal level=20 mV open drain | - | 2.9 | - | Ω |

1. $C_{oss\text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Source drain diode

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-----------------|-------------------------------|---|------|------|------|---------------|
| I_{SD} | Source-drain current | | - | | 31.5 | A |
| $I_{SDM}^{(1)}$ | Source-drain current (pulsed) | | - | | 126 | A |
| $V_{SD}^{(2)}$ | Forward on voltage | $I_{SD}= 31.5 \text{ A}, V_{GS}=0$ | - | | 1.6 | V |
| t_{rr} | Reverse recovery time | $I_{SD}= 31.5 \text{ A}, V_{DD}= 60 \text{ V}$ $di/dt = 100 \text{ A}/\mu\text{s}$, (see Figure 16) | - | 412 | | ns |
| Q_{rr} | Reverse recovery charge | | - | 8 | | μC |
| I_{RRM} | Reverse recovery current | | - | 39 | | A |
| t_{rr} | Reverse recovery time | $I_{SD}= 31.5 \text{ A}, V_{DD}= 60 \text{ V}$ $di/dt=100 \text{ A}/\mu\text{s}$, $T_j=150 \text{ }^\circ\text{C}$ (see Figure 16) | - | 490 | | ns |
| Q_{rr} | Reverse recovery charge | | - | 10 | | μC |
| I_{RRM} | Reverse recovery current | | - | 43 | | A |

1. Pulse width limited by safe operating area
2. Pulsed: Pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

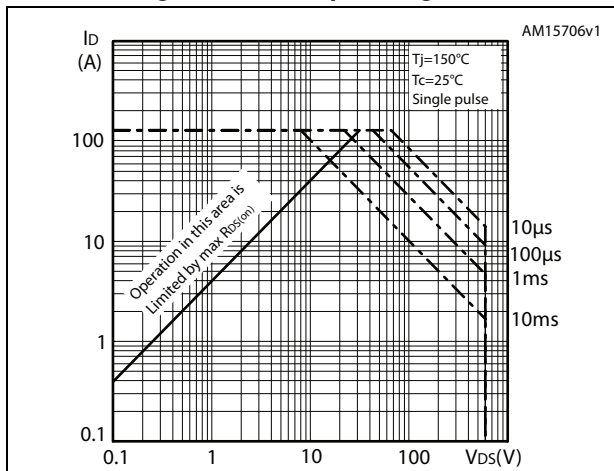


Figure 3. Thermal impedance

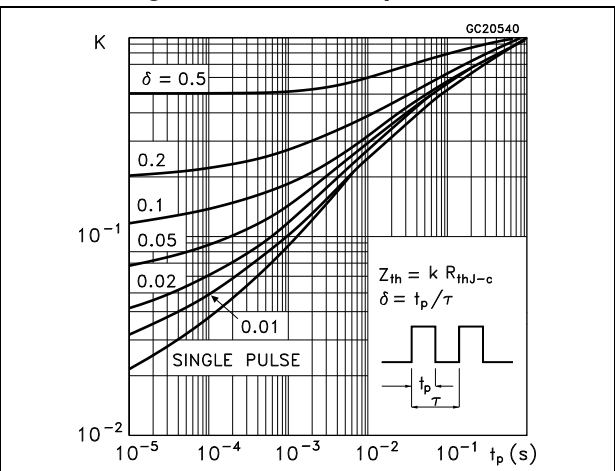


Figure 4. Output characteristics

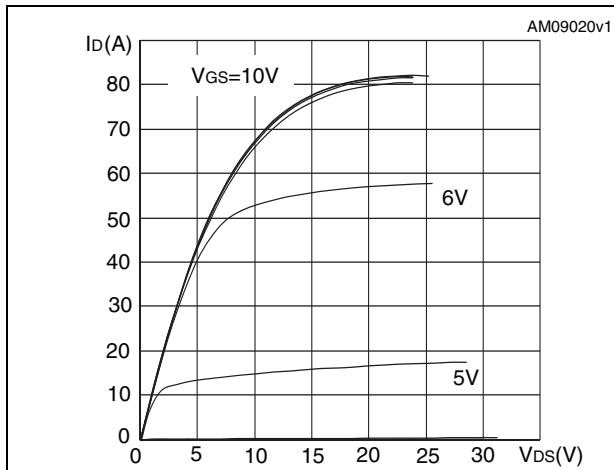


Figure 5. Transfer characteristics

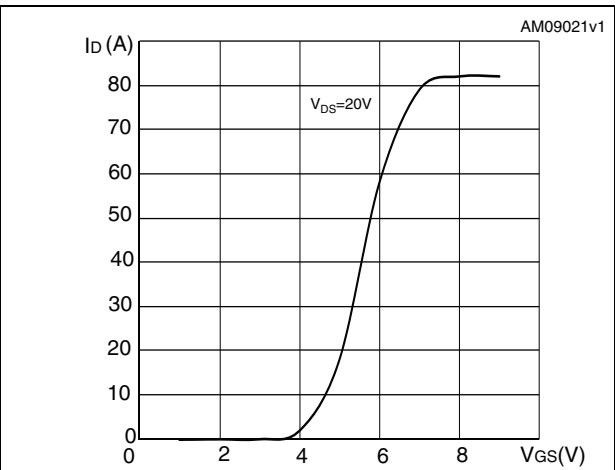


Figure 6. Gate charge vs gate-source voltage

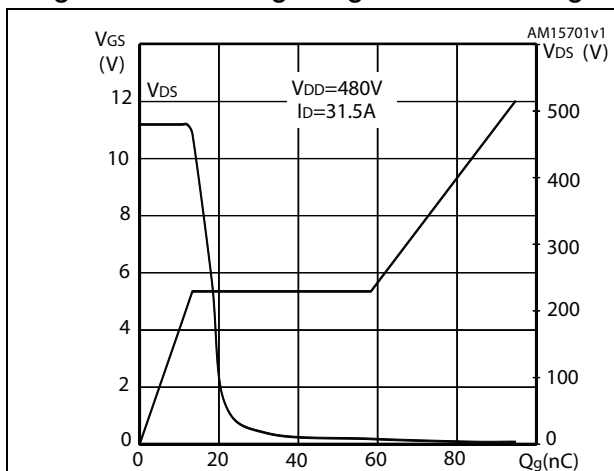


Figure 7. Static drain-source on-resistance

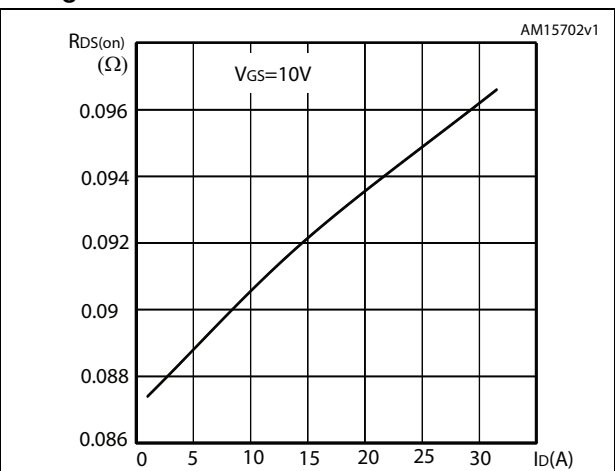


Figure 8. Capacitance variations

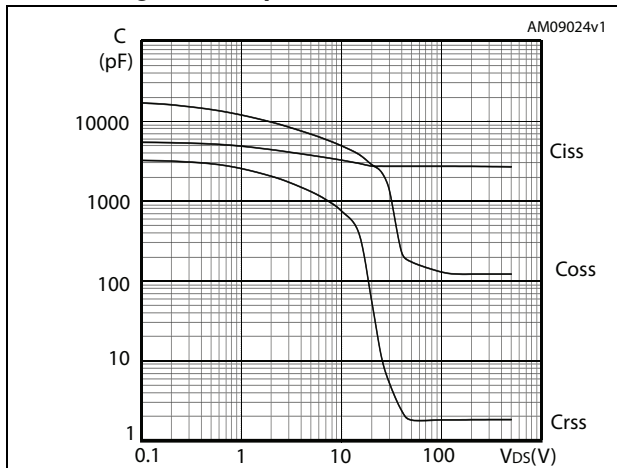


Figure 9. Output capacitance stored energy

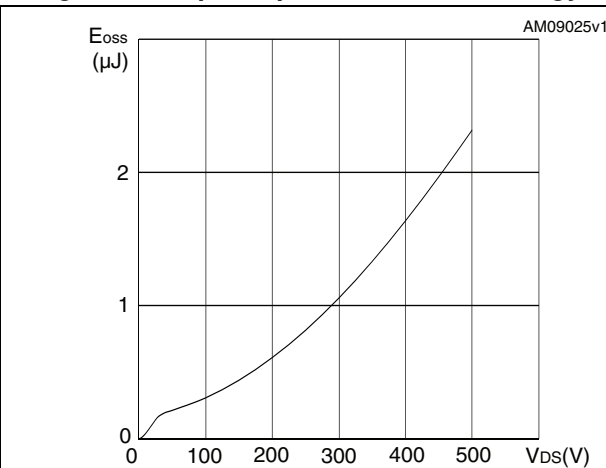


Figure 10. Normalized gate threshold voltage vs temperature

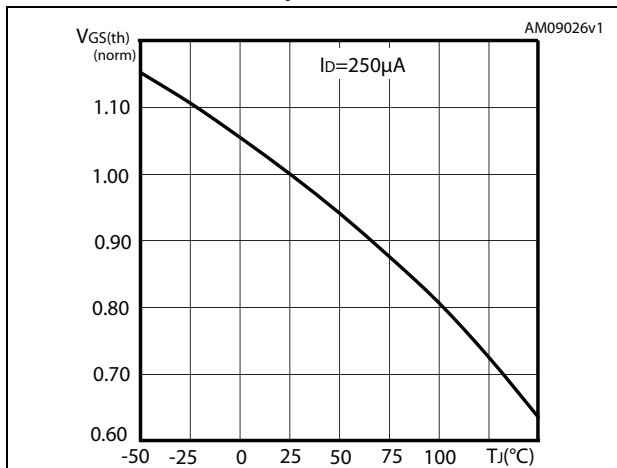


Figure 11. Normalized on-resistance vs temperature

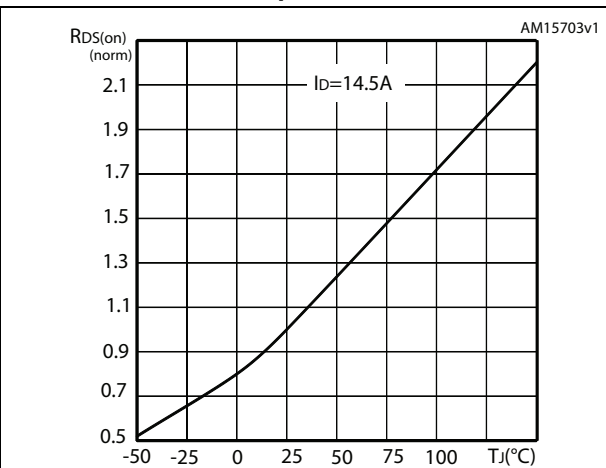


Figure 12. Normalized B_{VDS} vs temperature

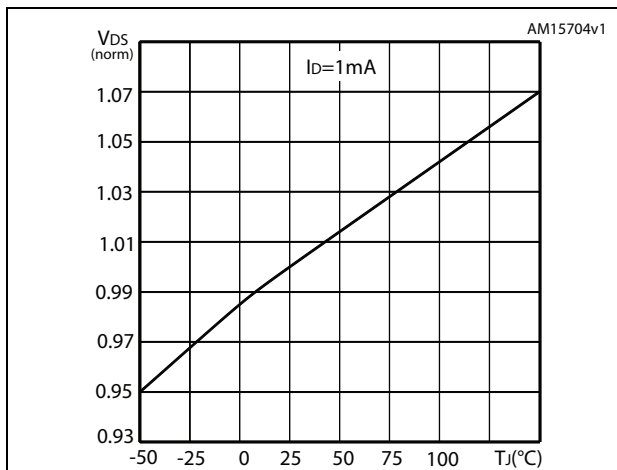
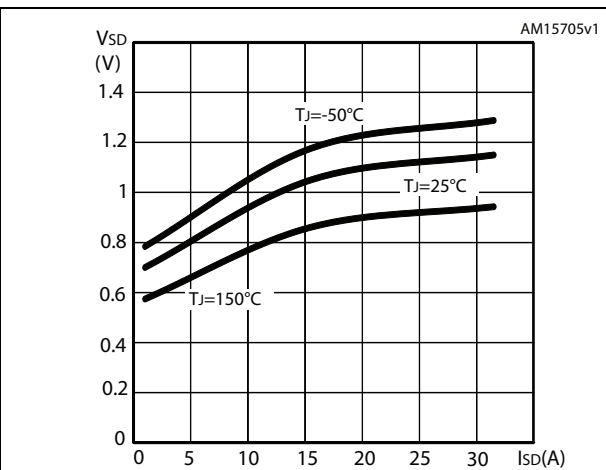


Figure 13. Source-drain diode forward characteristics



3 Test circuits

Figure 14. Switching times test circuit for resistive load

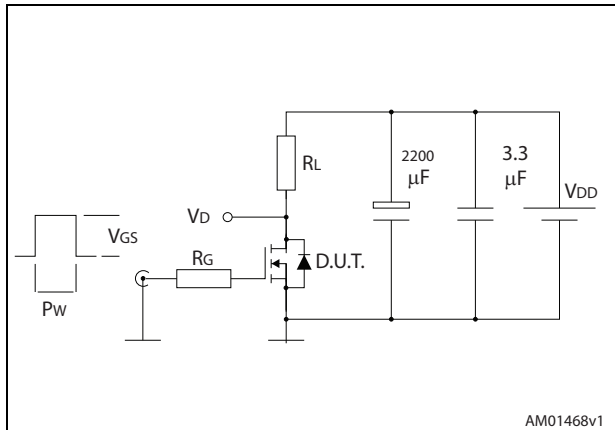


Figure 15. Gate charge test circuit

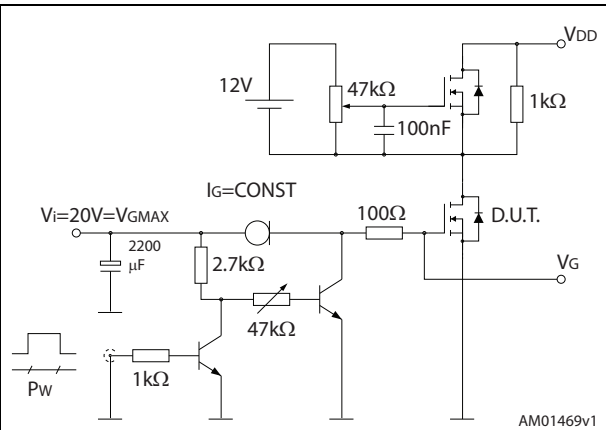


Figure 16. Test circuit for inductive load switching and diode recovery times

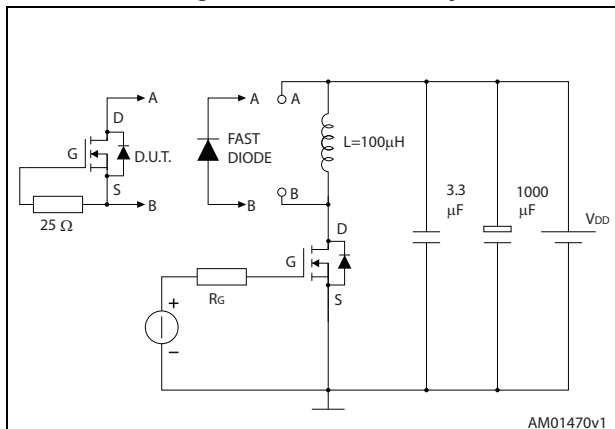


Figure 17. Unclamped inductive load test circuit

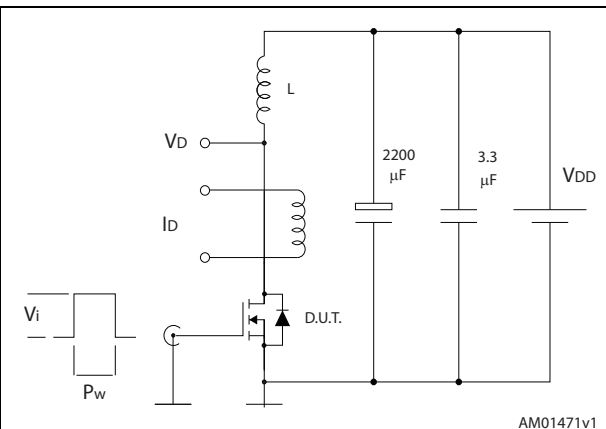


Figure 18. Unclamped inductive waveform

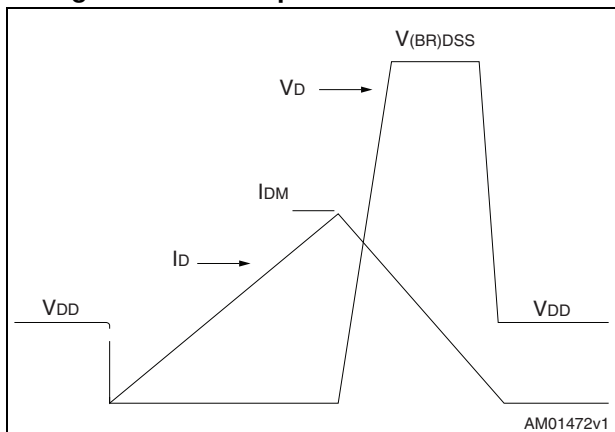
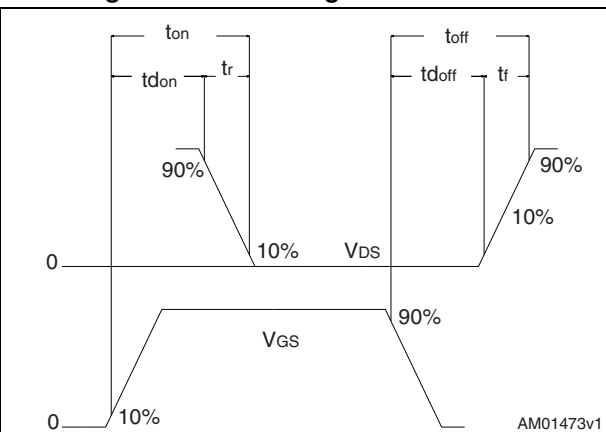


Figure 19. Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

4.1 D²PAK package information

Figure 20. D²PAK (TO-263) outline

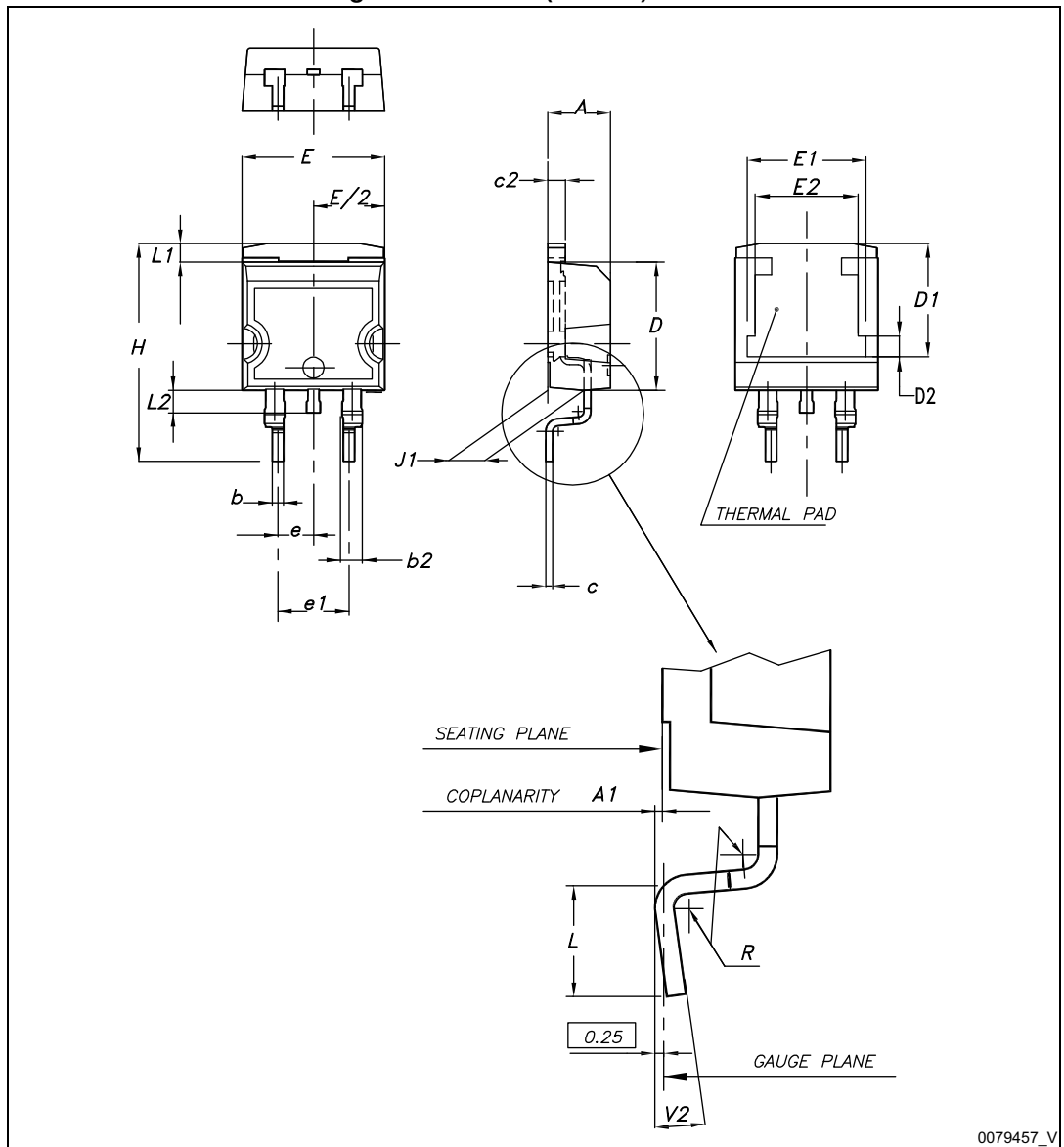
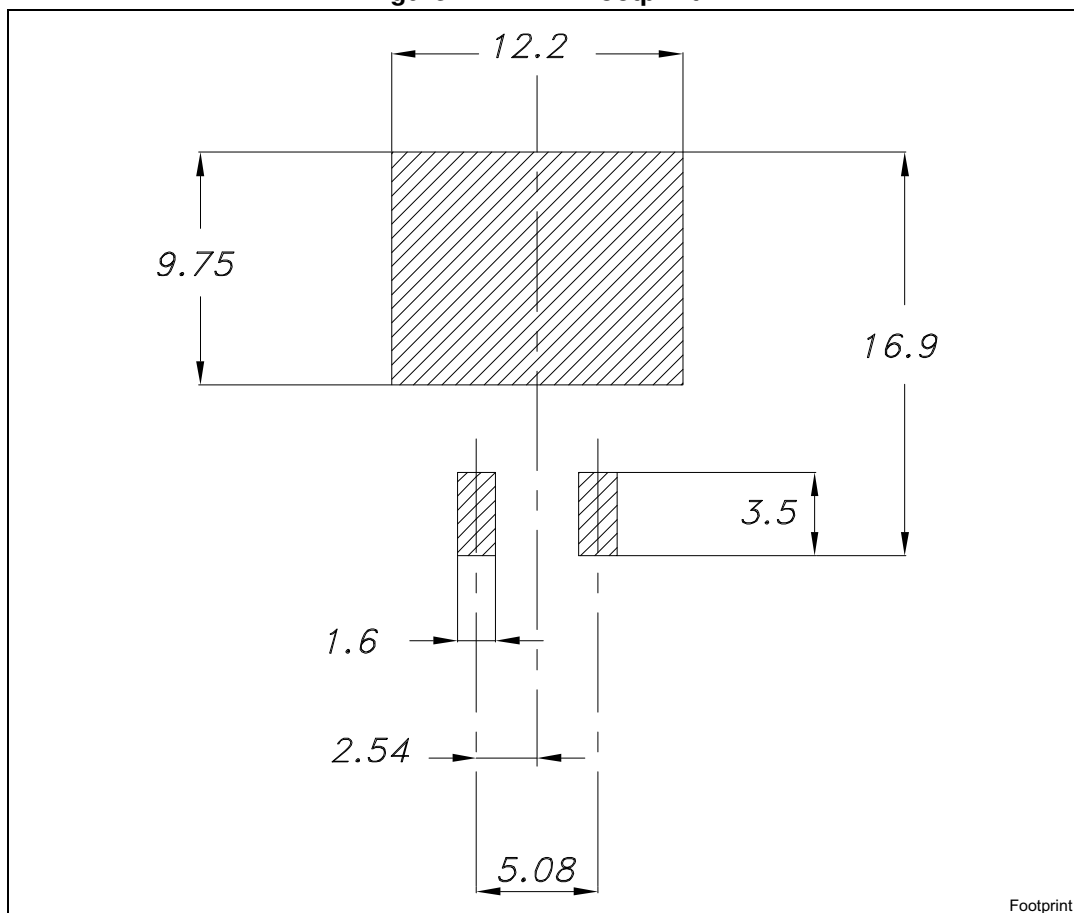


Table 7. D²PAK (TO-263) mechanical data

| Dim. | mm | | |
|------|------|------|-------|
| | Min. | Typ. | Max. |
| A | 4.40 | | 4.60 |
| A1 | 0.03 | | 0.23 |
| b | 0.70 | | 0.93 |
| b2 | 1.14 | | 1.70 |
| c | 0.45 | | 0.60 |
| c2 | 1.23 | | 1.36 |
| D | 8.95 | | 9.35 |
| D1 | 7.50 | 7.75 | 8.00 |
| D2 | 1.10 | 1.30 | 1.50 |
| E | 10 | | 10.40 |
| E1 | 8.50 | 8.70 | 8.90 |
| E2 | 6.85 | 7.05 | 7.25 |
| e | | 2.54 | |
| e1 | 4.88 | | 5.28 |
| H | 15 | | 15.85 |
| J1 | 2.49 | | 2.69 |
| L | 2.29 | | 2.79 |
| L1 | 1.27 | | 1.40 |
| L2 | 1.30 | | 1.75 |
| R | | 0.4 | |
| V2 | 0° | | 8° |

Figure 21. D²PAK footprint^(a)

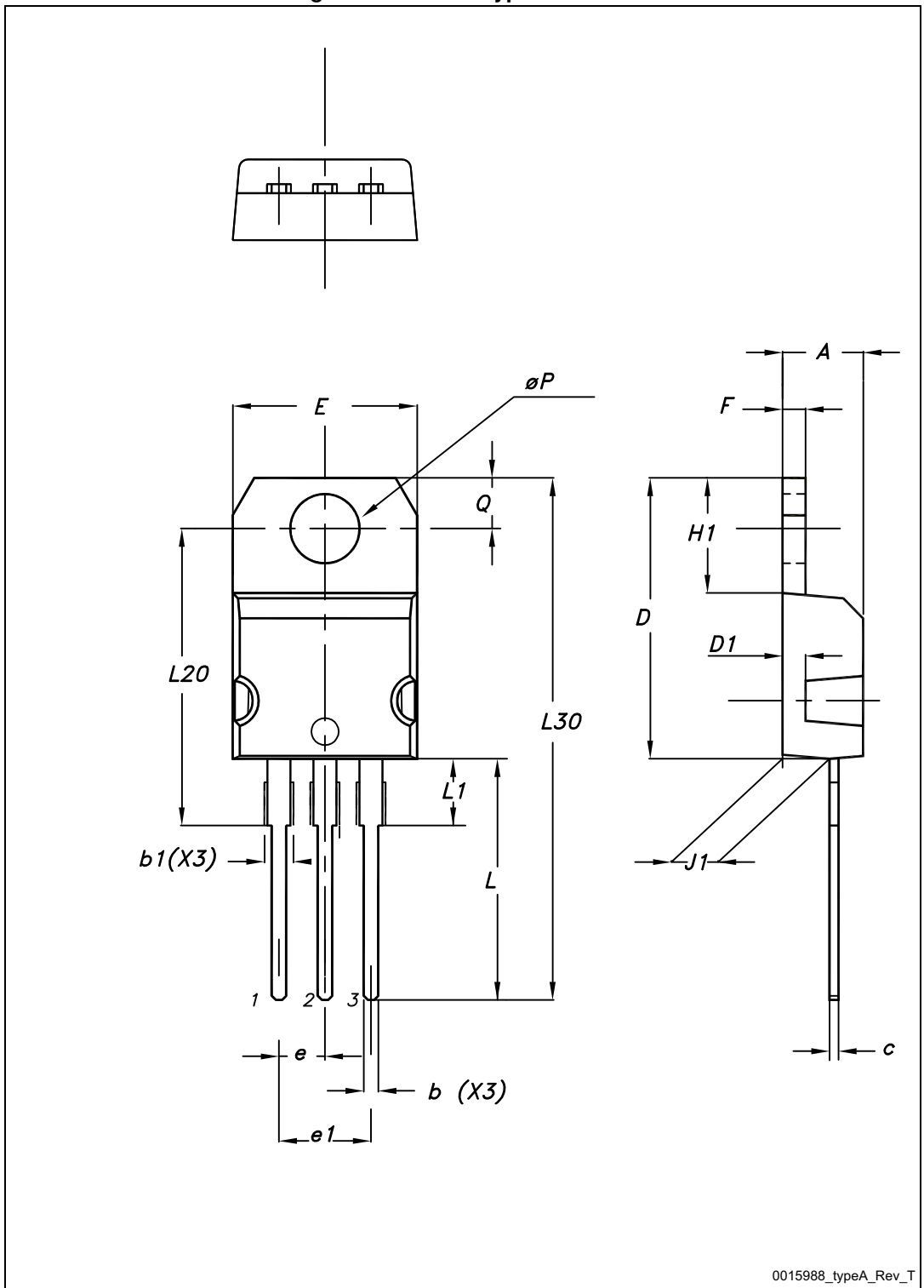


Footprint

a. All dimension are in millimeters

4.2 TO-220 package information

Figure 22. TO-220 type A outline



0015988_typeA_Rev_T

Table 8. TO-220 type A mechanical data

| Dim. | mm | | |
|------|-------|-------|-------|
| | Min. | Typ. | Max. |
| A | 4.40 | | 4.60 |
| b | 0.61 | | 0.88 |
| b1 | 1.14 | | 1.70 |
| c | 0.48 | | 0.70 |
| D | 15.25 | | 15.75 |
| D1 | | 1.27 | |
| E | 10 | | 10.40 |
| e | 2.40 | | 2.70 |
| e1 | 4.95 | | 5.15 |
| F | 1.23 | | 1.32 |
| H1 | 6.20 | | 6.60 |
| J1 | 2.40 | | 2.72 |
| L | 13 | | 14 |
| L1 | 3.50 | | 3.93 |
| L20 | | 16.40 | |
| L30 | | 28.90 | |
| øP | 3.75 | | 3.85 |
| Q | 2.65 | | 2.95 |

5 Packing information

Table 9. D²PAK (TO-263) tape and reel mechanical data

| Tape | | | Reel | | |
|------|------|------|----------|------|------|
| Dim. | mm | | Dim. | mm | |
| | Min. | Max. | | Min. | Max. |
| A0 | 10.5 | 10.7 | A | | 330 |
| B0 | 15.7 | 15.9 | B | 1.5 | |
| D | 1.5 | 1.6 | C | 12.8 | 13.2 |
| D1 | 1.59 | 1.61 | D | 20.2 | |
| E | 1.65 | 1.85 | G | 24.4 | 26.4 |
| F | 11.4 | 11.6 | N | 100 | |
| K0 | 4.8 | 5.0 | T | | 30.4 |
| P0 | 3.9 | 4.1 | | | |
| P1 | 11.9 | 12.1 | Base qty | | 1000 |
| P2 | 1.9 | 2.1 | Bulk qty | | 1000 |
| R | 50 | | | | |
| T | 0.25 | 0.35 | | | |
| W | 23.7 | 24.3 | | | |

Figure 23. Tape

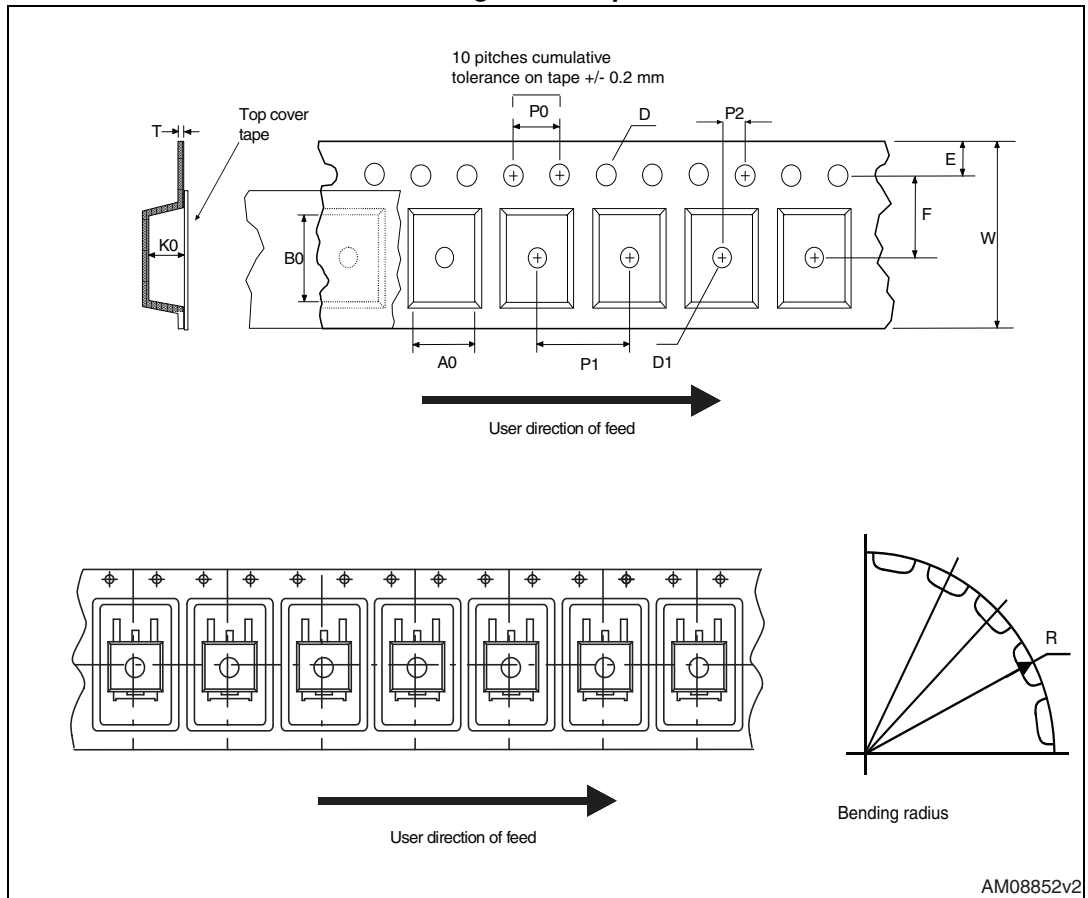
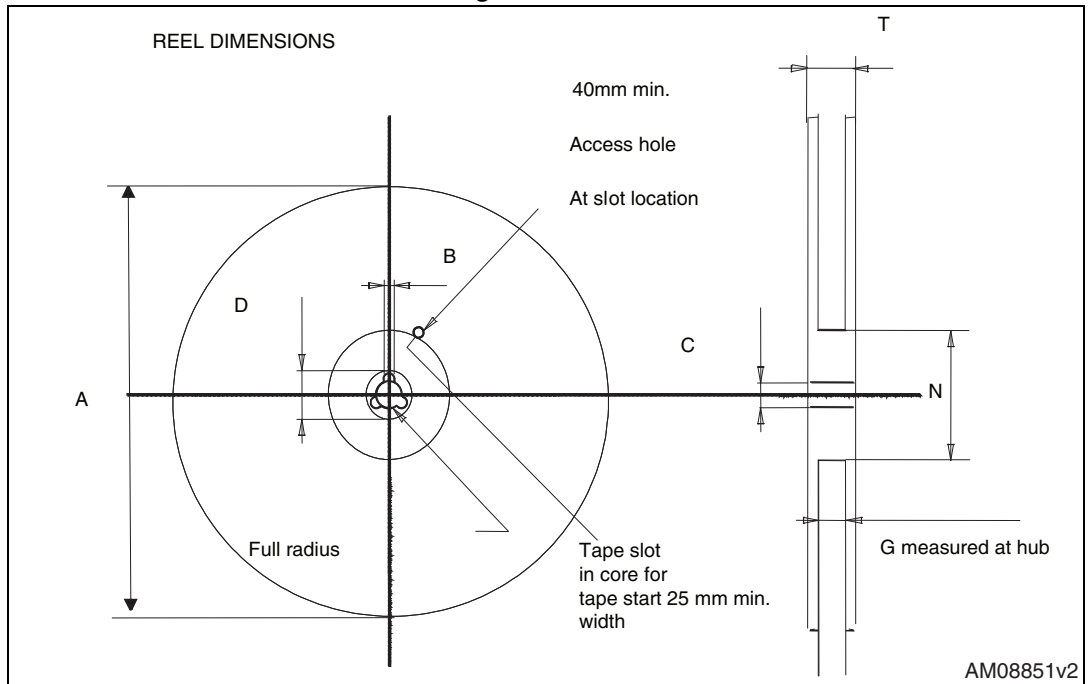


Figure 24. Reel



6 Revision history

Table 10. Document revision history

| Date | Revision | Changes |
|-------------|----------|---|
| 05-Aug-2010 | 1 | Initial release. |
| 02-Sep-2010 | 2 | Updated title on cover page and Table 4: On/off states . |
| 07-Apr-2011 | 3 | Document status promoted from preliminary data to datasheet. |
| 10-Oct-2011 | 4 | Inserted new device in D ² PAK: Updated: Table 2: Absolute maximum ratings , Table 3: Thermal data and Section 4: Package information with the new device. Inserted Section 5: Packing information . Minor text changes. |
| 12-Dec-2011 | 5 | <ul style="list-style-type: none"> – Figure 9: Output capacitance stored energy has been updated. – Figure 10: Normalized gate threshold voltage vs temperature has been updated. – Figure 11: Normalized on-resistance vs temperature has been updated. – Figure 12: Normalized B_{VDSS} vs temperature has been updated. |
| 21-Dec-2011 | 6 | Updated: Table 2: Absolute maximum ratings (V_{ISO} value for TO-220FP) |
| 10-May-2012 | 7 | Figure 6: Gate charge vs gate-source voltage has been updated. |
| 01-Jul-2013 | 8 | <ul style="list-style-type: none"> – The part number STB34NM60N has been moved to a separate datasheet. – Added: MOSFET ruggedness parameter and 3 on Table 2 – Modified: I_D value on Table 5 and typical values for $t_{d(on)}$, t_r, $t_{d(off)}$ and t_f, max values for I_{SD} and I_{SDM}, I_{SD} for V_{SD}, typical value and I_{SD} for t_{rr} – Modified: Figure 6, 7, 12 and 13 – Minor text changes |
| 20-Mar-2015 | 9 | <ul style="list-style-type: none"> – The part number STW34NM60N has been moved to a separate datasheet. – Updated Section 4: Package information. – Minor text changes. |

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