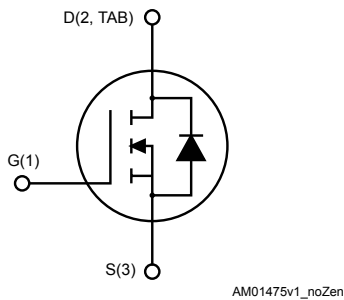
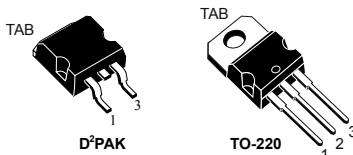


## N-channel 200 V, 15 mΩ, 65 A, MDmesh™ M5 Power MOSFETs in D<sup>2</sup>PAK and TO-220 packages



### Features

Order codes	V <sub>DS</sub>	R <sub>DS(on)</sub> max.	I <sub>D</sub>
STB80N20M5	200 V	20 mΩ	65 A
STP80N20M5			

- Extremely low R<sub>DS(on)</sub>
- Low gate charge and input capacitance
- Excellent switching performance
- 100% avalanche tested

### Applications

- Switching applications

### Description

These devices are N-channel Power MOSFETs based on the MDmesh™ M5 innovative vertical process technology combined with the well-known PowerMESH™ horizontal layout. The resulting products offer extremely low on-resistance, making them particularly suitable for applications requiring high power and superior efficiency.



#### Product status links

[STB80N20M5](#)

[STP80N20M5](#)

#### Product summary

##### Order code: STB80N20M5

<b>Marking</b>	80N20M5
<b>Package</b>	D <sup>2</sup> PAK
<b>Packing</b>	Tape and reel

##### Order code: STP80N20M5

<b>Marking</b>	80N20M5
<b>Package</b>	TO-220
<b>Packing</b>	Tube

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{GS}$	Gate-source voltage	±25	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ °C}$	65	A
	Drain current (continuous) at $T_C = 100\text{ °C}$	41	A
$I_{DM}^{(1)}$	Drain current (pulsed)	232	A
$P_{TOT}$	Total power dissipation at $T_C = 25\text{ °C}$	190	W
$I_{AR}$	Avalanche current, repetitive or non-repetitive (pulse width limited by $T_{Jmax}$ )	20	A
$E_{AS}$	Single pulse avalanche energy (starting $T_j = 25\text{ °C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ )	500	mJ
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
$T_j$	Operating junction temperature range	-55 to 150	°C
$T_{stg}$	Storage temperature range		

1. Pulse width limited by safe operating area
2.  $I_{SD} \leq 65\text{ A}$ ,  $di/dt \leq 400\text{ A}/\mu\text{s}$ ,  $V_{DS(peak)} < V_{(BR)DSS}$

**Table 2. Thermal data**

Symbol	Parameter	Value		Unit
		D <sup>2</sup> PAK	TO-220	
$R_{thj-case}$	Thermal resistance junction-case	0.66		°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient		62.5	°C/W
$R_{thj-pcb}$	Thermal resistance junction-pcb	30		°C/W

## 2 Electrical characteristics

( $T_{CASE} = 25\text{ }^{\circ}\text{C}$  unless otherwise specified)

**Table 3. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$ , $V_{GS} = 0\text{ V}$	200			V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$ , $V_{DS} = 200\text{ V}$			1	$\mu\text{A}$
		$V_{GS} = 0\text{ V}$ , $V_{DS} = 200\text{ V}$ , $T_C = 125\text{ }^{\circ}\text{C}^{(1)}$			100	$\mu\text{A}$
$I_{GSS}$	Gate-body leakage current	$V_{DS} = 0\text{ V}$ , $V_{GS} = \pm 25\text{ V}$			100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}$ , $I_D = 32.5\text{ A}$		15	20	m $\Omega$

1. Defined by design, not subject to production test.

**Table 4. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 50\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0\text{ V}$	-	4080	-	$\mu\text{F}$
$C_{oss}$	Output capacitance			290		
$C_{rss}$	Reverse transfer capacitance			50		
$C_{o(tr)}^{(1)}$	Time-related equivalent capacitance	$V_{DS} = 0\text{ to }160\text{ V}$ , $V_{GS} = 0\text{ V}$	-	740	-	$\mu\text{F}$
$C_{o(er)}^{(2)}$	Energy-related equivalent capacitance			295		
$R_g$	Gate input resistance	$f = 1\text{ MHz}$ open drain	-	2	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 160\text{ V}$ , $I_D = 32.5\text{ A}$ , $V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 14. Test circuit for gate charge behavior)	-	108	-	nC
$Q_{gs}$	Gate-source charge			23		
$Q_{gd}$	Gate-drain charge			62		

1.  $C_{o(tr)}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$ .

2.  $C_{o(er)}$  is defined as a constant equivalent capacitance giving the same stored energy as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$ .

**Table 5. Switching times**

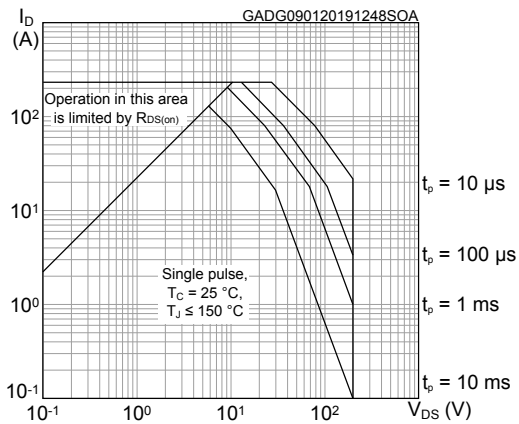
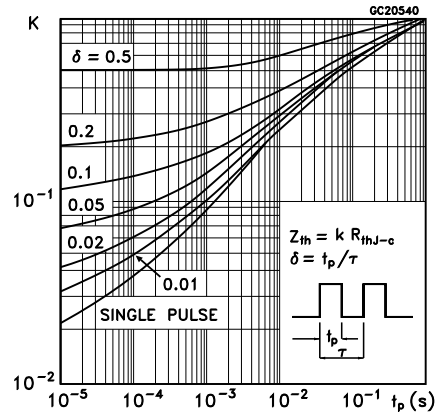
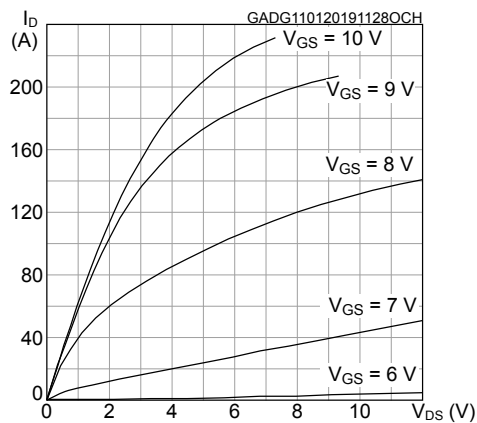
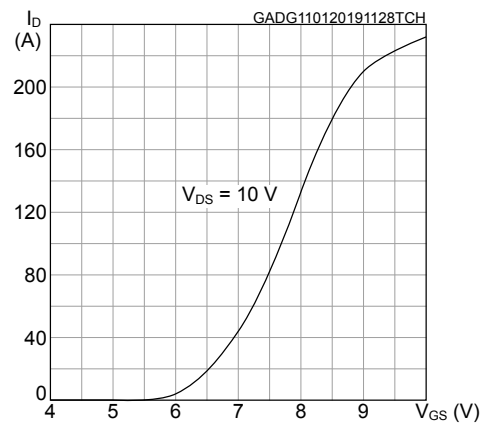
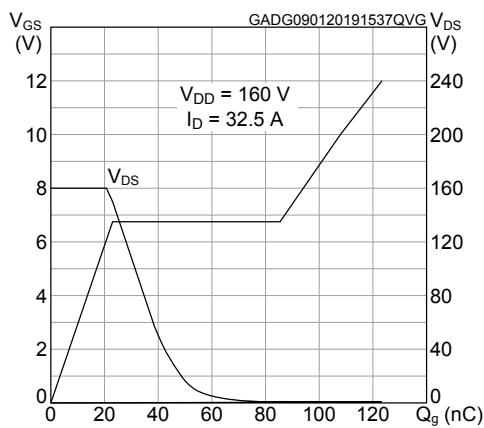
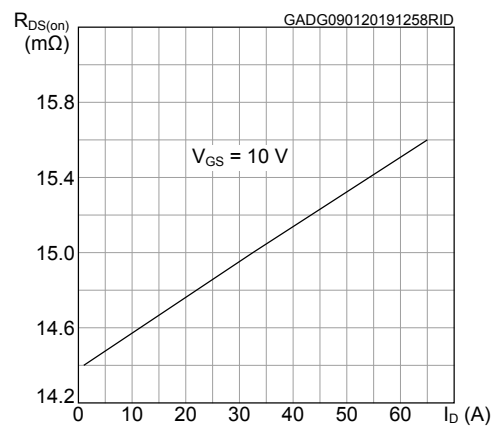
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(v)}$	Voltage delay time	$V_{DD} = 160\text{ V}$ , $I_D = 65\text{ A}$ , $R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$ (see Figure 15. Test circuit for inductive load switching and diode recovery times and Figure 18. Switching time waveform)	-	83	-	ns
$t_{r(v)}$	Voltage rise time			26		
$t_{f(i)}$	Current fall time			46		
$t_{c(off)}$	Crossing time			77		

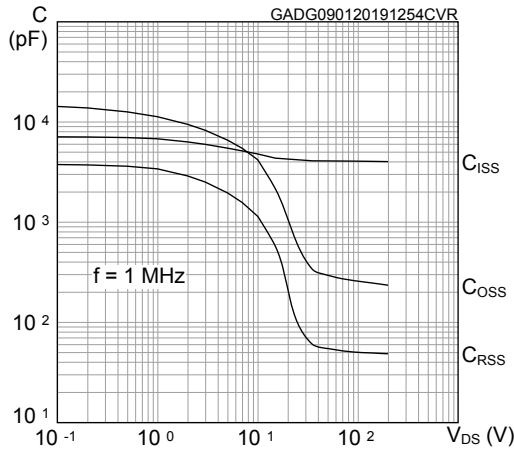
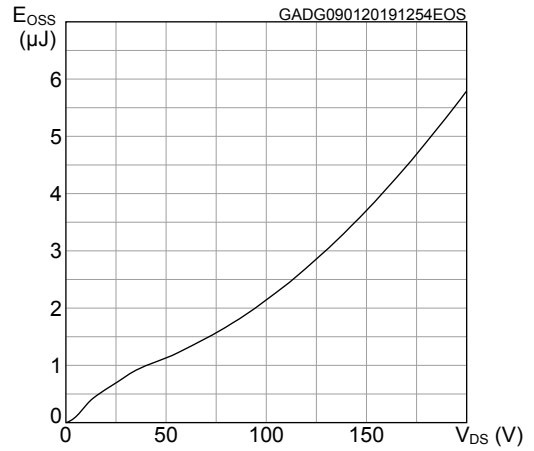
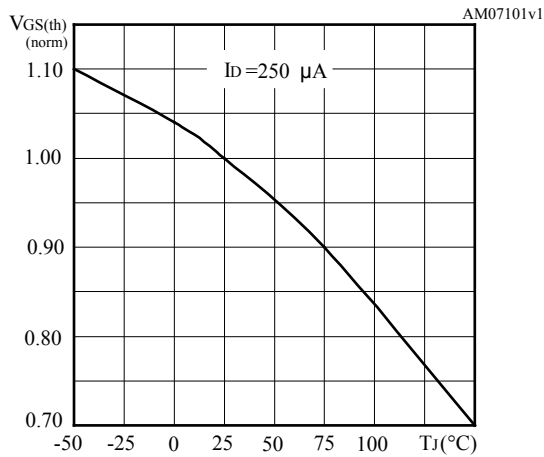
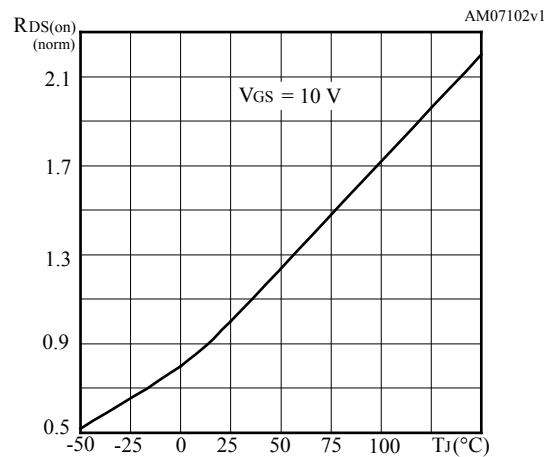
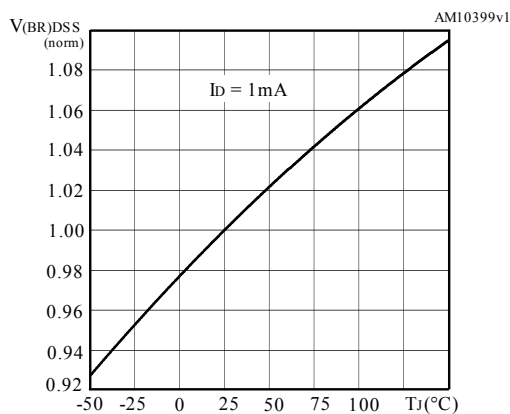
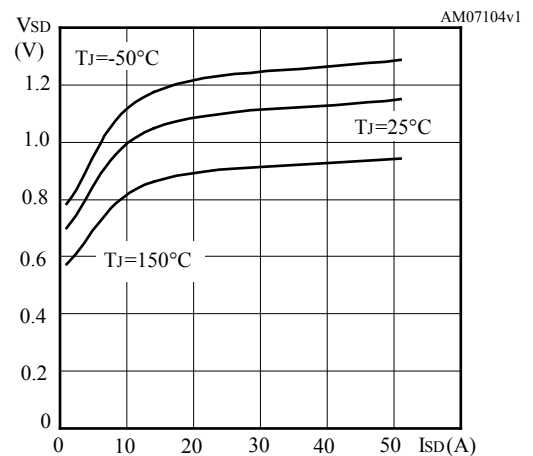
**Table 6. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		65	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				232	
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 65 \text{ A}$ , $V_{GS} = 0 \text{ V}$	-		1.6	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 65 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$ , $V_{DD} = 60 \text{ V}$ (see <a href="#">Figure 15. Test circuit for inductive load switching and diode recovery times</a> )	-	178		ns
$Q_{rr}$	Reverse recovery charge			1.4		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current			16		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 65 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$ , $V_{DD} = 60 \text{ V}$ , $T_j = 150 \text{ }^\circ\text{C}$ (see <a href="#">Figure 15. Test circuit for inductive load switching and diode recovery times</a> )	-	219		ns
$Q_{rr}$	Reverse recovery charge			2.1		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current			20		A

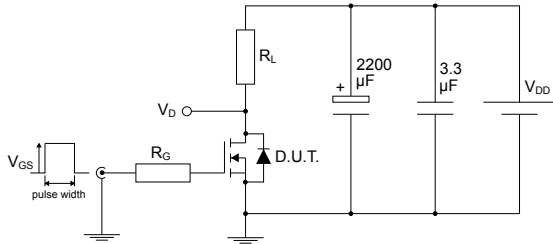
1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%.

## 2.1 Electrical characteristics (curves)

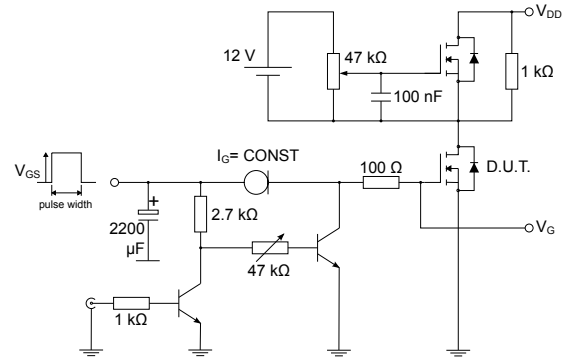
**Figure 1. Safe operating area**

**Figure 2. Thermal impedance**

**Figure 3. Output characteristics**

**Figure 4. Transfer characteristics**

**Figure 5. Gate charge vs gate-source voltage**

**Figure 6. Static drain-source on-resistance**


**Figure 7. Capacitance variations**

**Figure 8. Output capacitance stored energy**

**Figure 9. Normalized gate threshold voltage vs temperature**

**Figure 10. Normalized on-resistance vs temperature**

**Figure 11. Normalized  $V_{(BR)DSS}$  vs temperature**

**Figure 12. Source-drain diode forward characteristics**


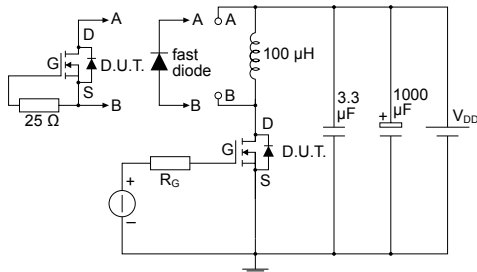
### 3 Test circuits

**Figure 13. Test circuit for resistive load switching times**


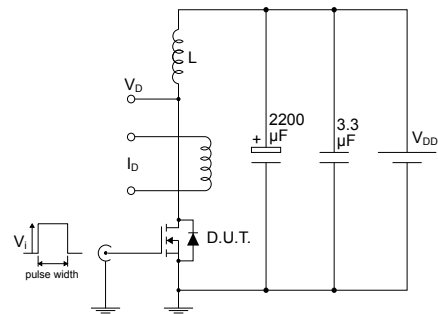
AM01488v1

**Figure 14. Test circuit for gate charge behavior**


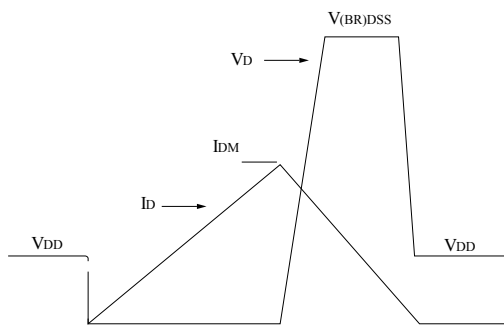
AM01469v1

**Figure 15. Test circuit for inductive load switching and diode recovery times**


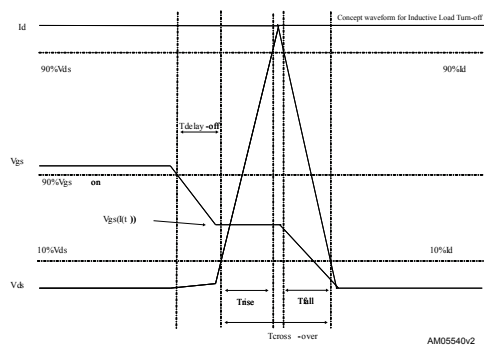
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**Figure 16. Unclamped inductive load test circuit**


AM01471v1

**Figure 17. Unclamped inductive waveform**


AM01472v1

**Figure 18. Switching time waveform**


AM05540v2

## 4 Package information

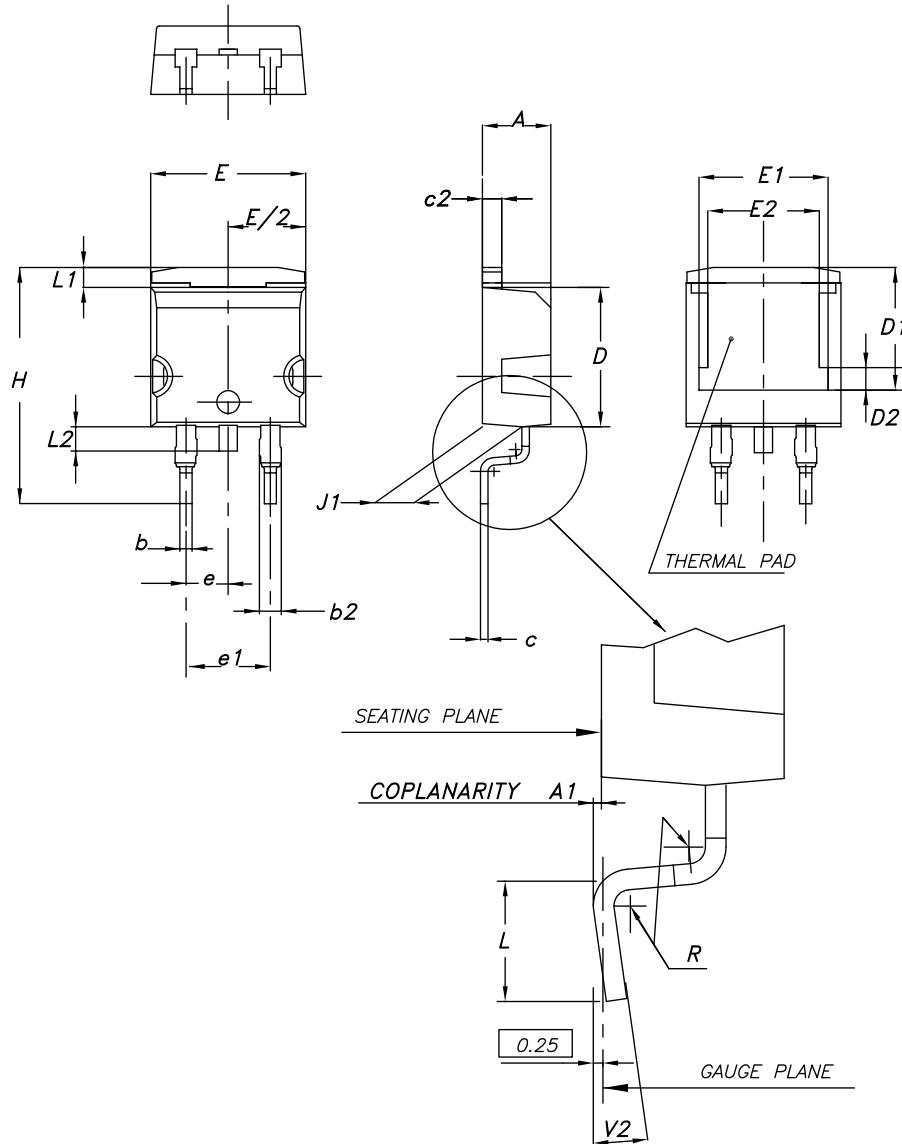
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In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK<sup>®</sup>** packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.



### 4.1 D<sup>2</sup>PAK (TO-263) type A2 package information

Figure 19. D<sup>2</sup>PAK (TO-263) type A2 package outline

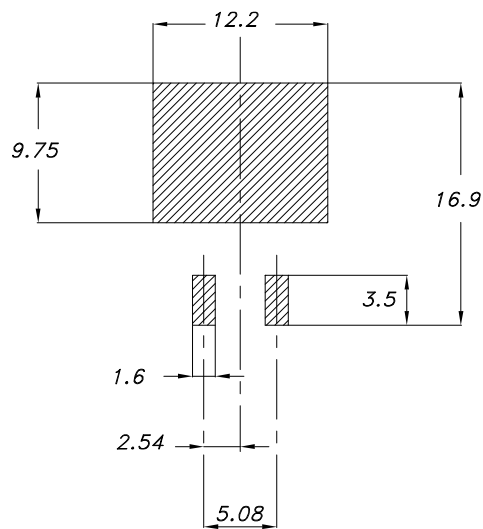


0079457\_A2\_25

**Table 7. D<sup>2</sup>PAK (TO-263) type A2 package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10.00		10.40
E1	8.70	8.90	9.10
E2	7.30	7.50	7.70
e		2.54	
e1	4.88		5.28
H	15.00		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.40	
V2	0°		8°

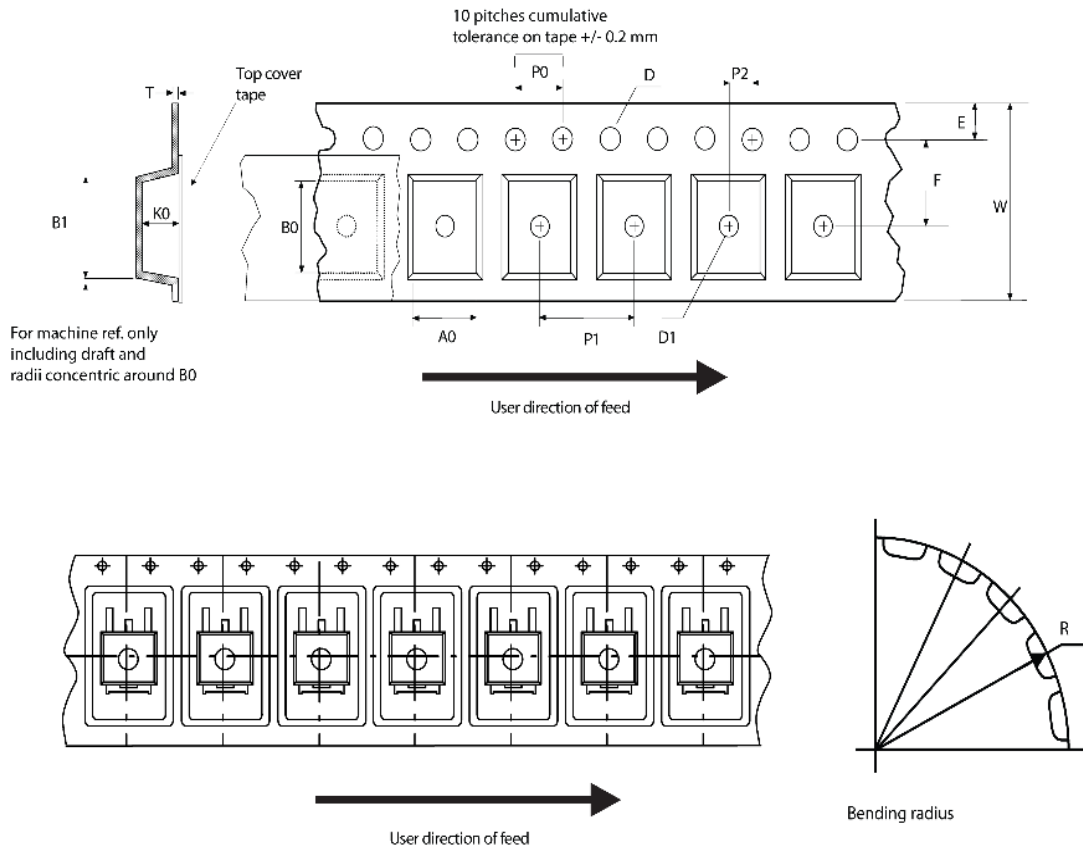
**Figure 20. D<sup>2</sup>PAK (TO-263) recommended footprint (dimensions are in mm)**



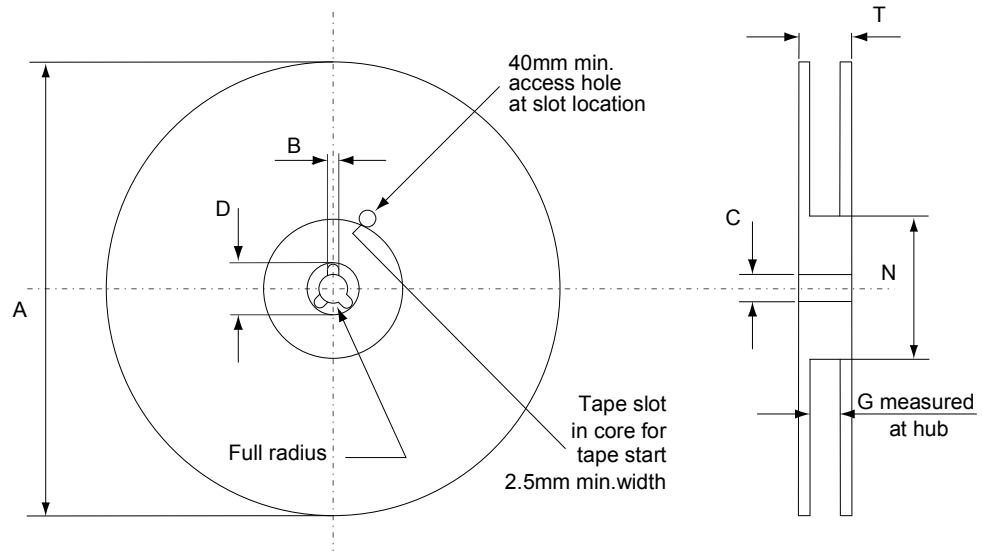
Footprint

## 4.2 D<sup>2</sup>PAK packing information

**Figure 21. D<sup>2</sup>PAK tape outline**



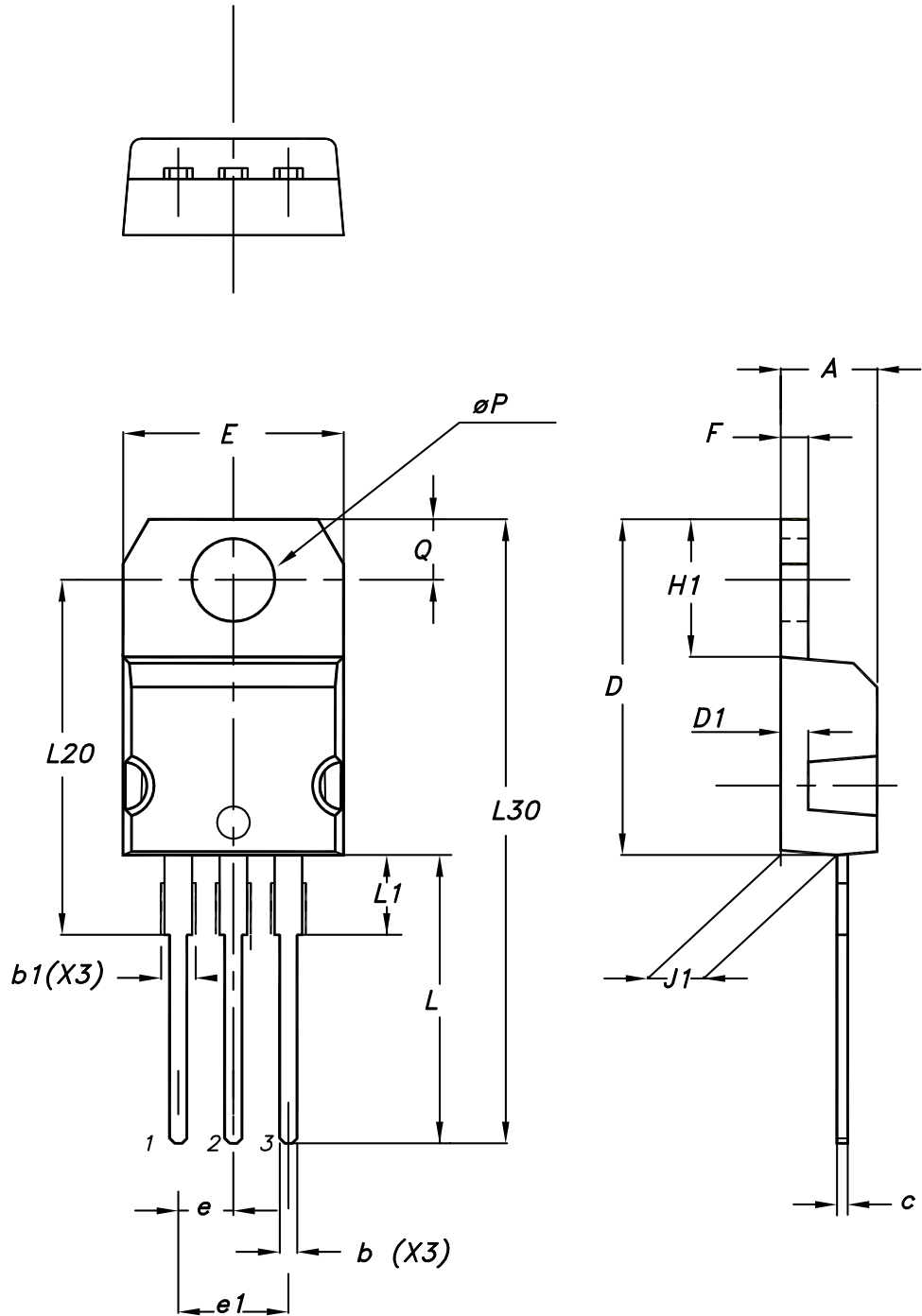
AM08852v1

**Figure 22. D<sup>2</sup>PAK reel outline**


AM06038v1

**Table 8. D<sup>2</sup>PAK tape and reel mechanical data**

Tape			Reel			
Dim.	mm		Dim.	mm		
	Min.	Max.		Min.	Max.	
A0	10.5	10.7	A		330	
B0	15.7	15.9	B	1.5		
D	1.5	1.6	C	12.8	13.2	
D1	1.59	1.61	D	20.2		
E	1.65	1.85	G	24.4	26.4	
F	11.4	11.6	N	100		
K0	4.8	5.0	T		30.4	
P0	3.9	4.1	Base quantity Bulk quantity			
P1	11.9	12.1				1000
P2	1.9	2.1				1000
R	50					
T	0.25	0.35				
W	23.7	24.3				

**4.3 TO-220 type A package information**
**Figure 23. TO-220 type A package outline**


0015988\_typeA\_Rev\_22

**Table 9. TO-220 type A package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95

## Revision history

**Table 10. Document revision history**

Date	Version	Changes
01-Jul-2009	1	First release
03-Jul-2010	2	Document status promoted from preliminary data to datasheet
16-Jan-2019	3	Updated title, features and internal schematic diagram on cover page. Updated <a href="#">Section 1 Electrical ratings</a> , <a href="#">Section 2 Electrical characteristics</a> and <a href="#">Section 4.1 D<sup>2</sup>PAK (TO-263) type A2 package information</a> . Minor text changes.

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