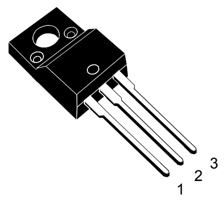
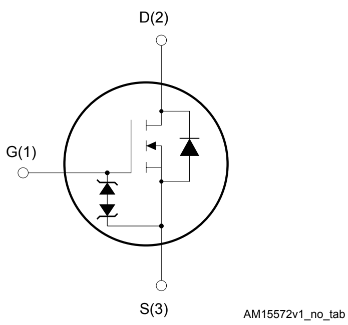
STF24N60M2

Datasheet

N-channel 600 V, 168 mΩ typ., 18 A MDmesh M2 Power MOSFET in a TO-220FP package



TO-220FP



Product status link
STF24N60M2

Product summary	
Order code	STF24N60M2
Marking	24N60M2
Package	TO-220FP
Packing	Tube

Features

Order code	V_{DS} @T_{Jmax}	$R_{DS(on)}$ max.	I_D
STF24N60M2	650 V	190 mΩ	18 A

- Extremely low gate charge
- Excellent output capacitance (C_{oss}) profile
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications
- LCC converters
- Resonant converters

Description

This device is an N-channel Power MOSFET developed using MDmesh M2 technology. Thanks to its strip layout and an improved vertical structure, the device exhibits low on-resistance and optimized switching characteristics, rendering it suitable for the most demanding high efficiency converters.

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	±25	V
I_D (1)	Drain current (continuous) at T_C = 25 °C	18	A
	Drain current (continuous) at T_C = 100 °C	12	A
I_{DM} (2)	Drain current (pulsed)	72	A
P_{TOT}	Total power dissipation at T_C = 25 °C	30	W
dv/dt (3)	Peak diode recovery voltage slope	15	V/ns
dv/dt (4)	MOSFET dv/dt ruggedness	50	V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s; T_C = 25 °C)	2.5	kV
T_{stg}	Storage temperature range	-55 to 150	°C
T_j	Operating junction temperature range		

1. *Limited by maximum junction temperature.*
2. *Pulse width limited by safe operating area.*
3. *I_{SD} ≤ 18 A, di/dt ≤ 400 A/µs; $V_{DS(peak)}$ < $V_{(BR)DSS}$, V_{DD} = 400 V*
4. *V_{DS} ≤ 480 V*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	4.2	°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient	62.5	°C/W

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_{jmax})	3.5	A
E_{AS}	Single pulse avalanche energy (starting T_j=25 °C, I_D= I_{AR}, V_{DD}=50 V)	180	mJ

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified).

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0 V	600			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 600 V			1	µA
		V_{GS} = 0 V, V_{DS} = 600 V, T_C = 125 °C [(1)]			100	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ± 25 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 9 A		168	190	mΩ

1. *Defined by design, not subject to production test.*

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0 V	-	1060	-	pF
C_{oss}	Output capacitance		-	55	-	pF
C_{rss}	Reverse transfer capacitance		-	2.2	-	pF
$C_{oss\ eq.}$ [(1)]	Equivalent output capacitance	V_{DS} = 0 to 480 V, V_{GS} = 0 V	-	258	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz, I_D = 0 A	-	7	-	Ω
Q_g	Total gate charge	V_{DD} = 480 V, I_D = 18 A, V_{GS} = 0 to 10 V (see Figure 14. Test circuit for gate charge behavior)	-	29	-	nC
Q_{gs}	Gate-source charge		-	6	-	nC
Q_{gd}	Gate-drain charge		-	12	-	nC

1. *$C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.*

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 300 V, I_D = 9 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	14	-	ns
t_r	Rise time		-	9	-	ns
$t_{d(off)}$	Turn-off delay time		-	60	-	ns
t_f	Fall time		-	15	-	ns

Table 7. **Source-drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} (1)	Source-drain current		-		18	A
I_{SDM} (2)	Source-drain current (pulsed)		-		72	A
V_{SD} (3)	Forward on voltage	I_{SD} = 18 A, V_{GS} = 0 V	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 18 A, di/dt = 100 A/µs	-	332		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 60 V (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	4		µC
I_{RRM}	Reverse recovery current		-	24		A
t_{rr}	Reverse recovery time	I_{SD} = 18 A, di/dt = 100 A/µs	-	450		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 60 V, T_j = 150 °C	-	5.5		µC
I_{RRM}	Reverse recovery current	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	25		A

1. *Limited by maximum junction temperature.*
2. *Pulse width limited by safe operating area.*
3. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%.*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

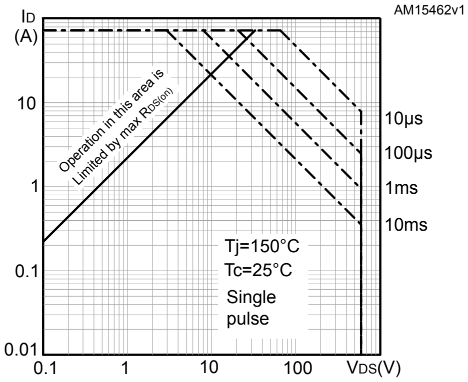


Figure 2. Thermal impedance

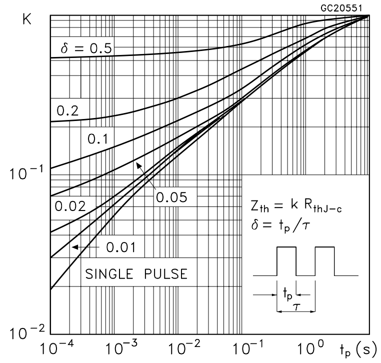


Figure 3. Output characteristics

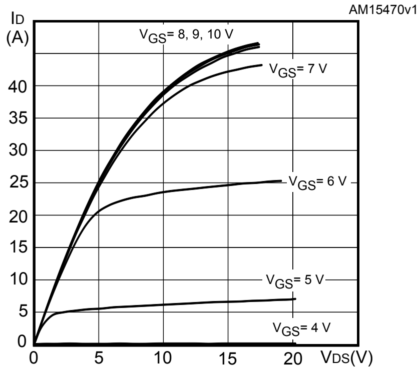


Figure 4. Transfer characteristics

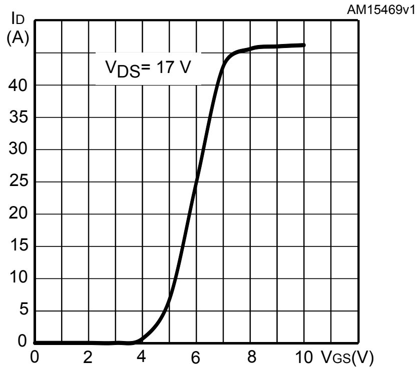


Figure 5. Gate charge vs gate-source voltage

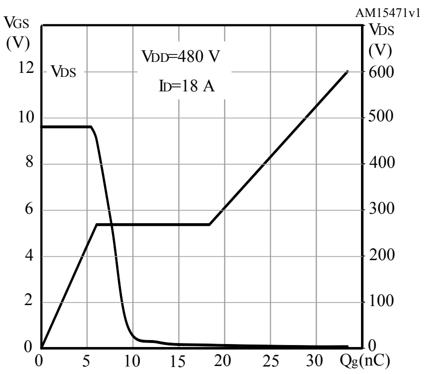


Figure 6. Static drain-source on-resistance

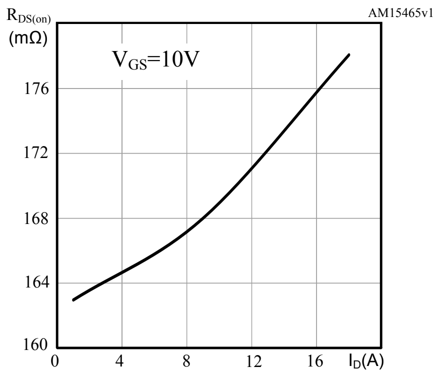


Figure 7. **Capacitance variations**

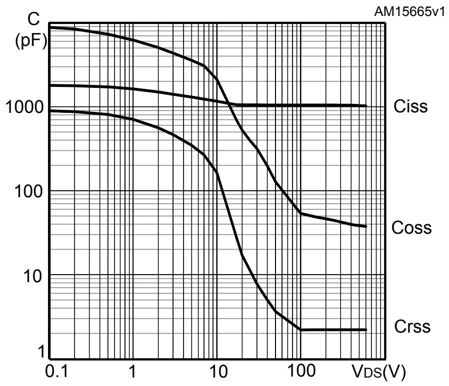


Figure 8. **Output capacitance stored energy**

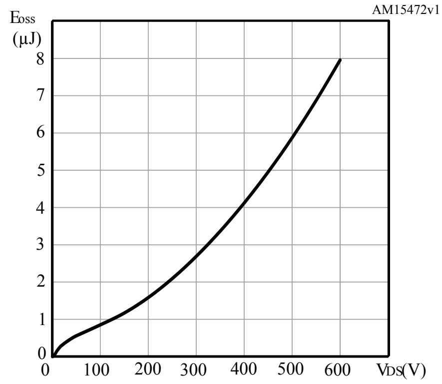


Figure 9. **Normalized gate threshold voltage vs temperature**

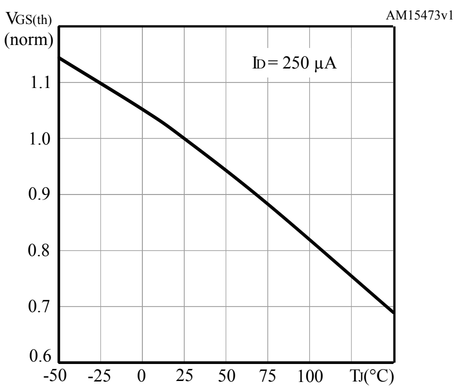


Figure 10. **Normalized on-resistance vs temperature**

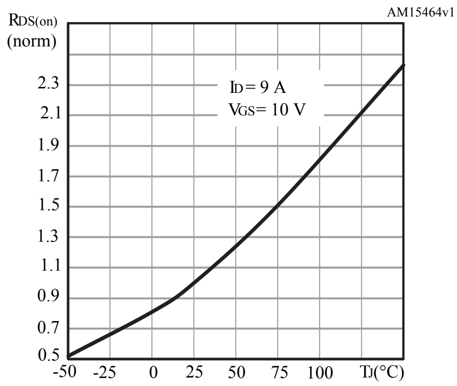


Figure 11. **Source-drain diode forward characteristics**

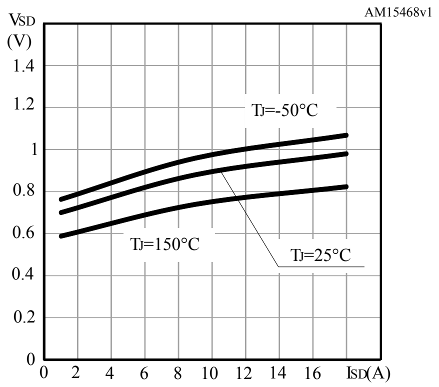
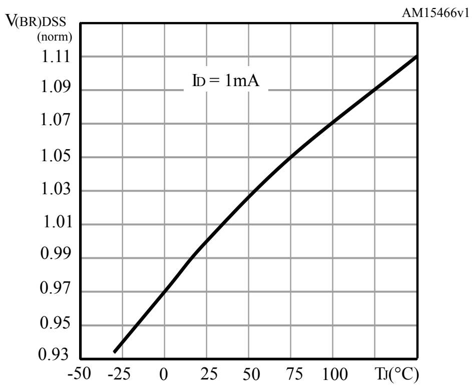


Figure 12. **Normalized $V_{(BR)DSS}$ vs temperature**



3 Test circuits

Figure 13. Test circuit for resistive load switching times

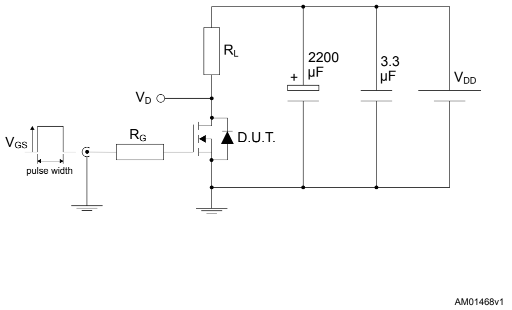


Figure 14. Test circuit for gate charge behavior

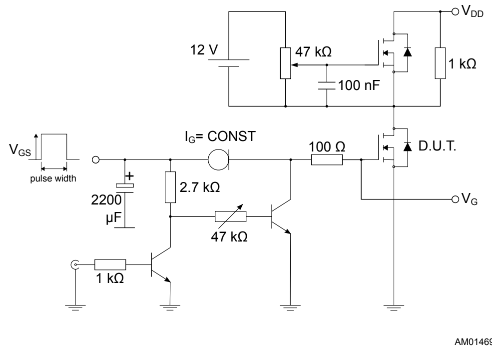


Figure 15. Test circuit for inductive load switching and diode recovery times

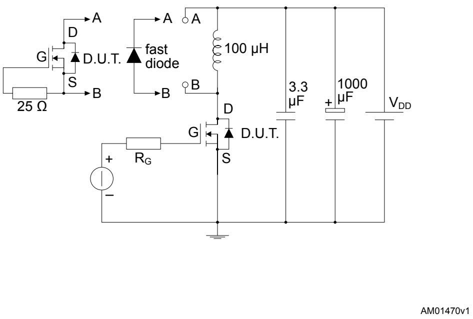


Figure 16. Unclamped inductive load test circuit

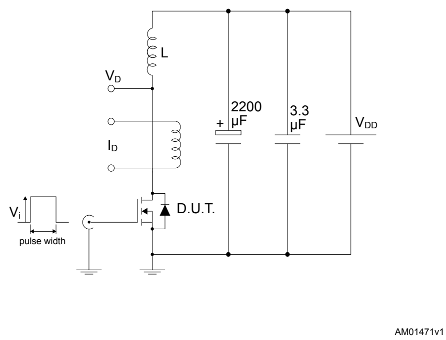


Figure 17. Unclamped inductive waveform

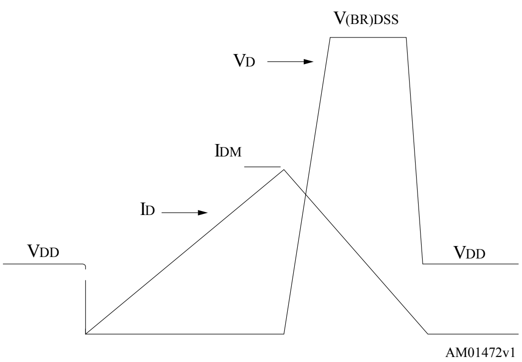
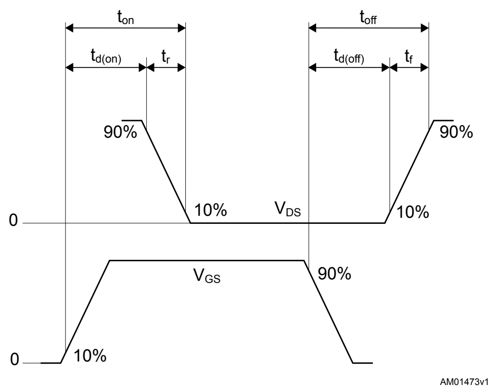


Figure 18. Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 TO-220FP package information

Figure 19. TO-220FP package outline

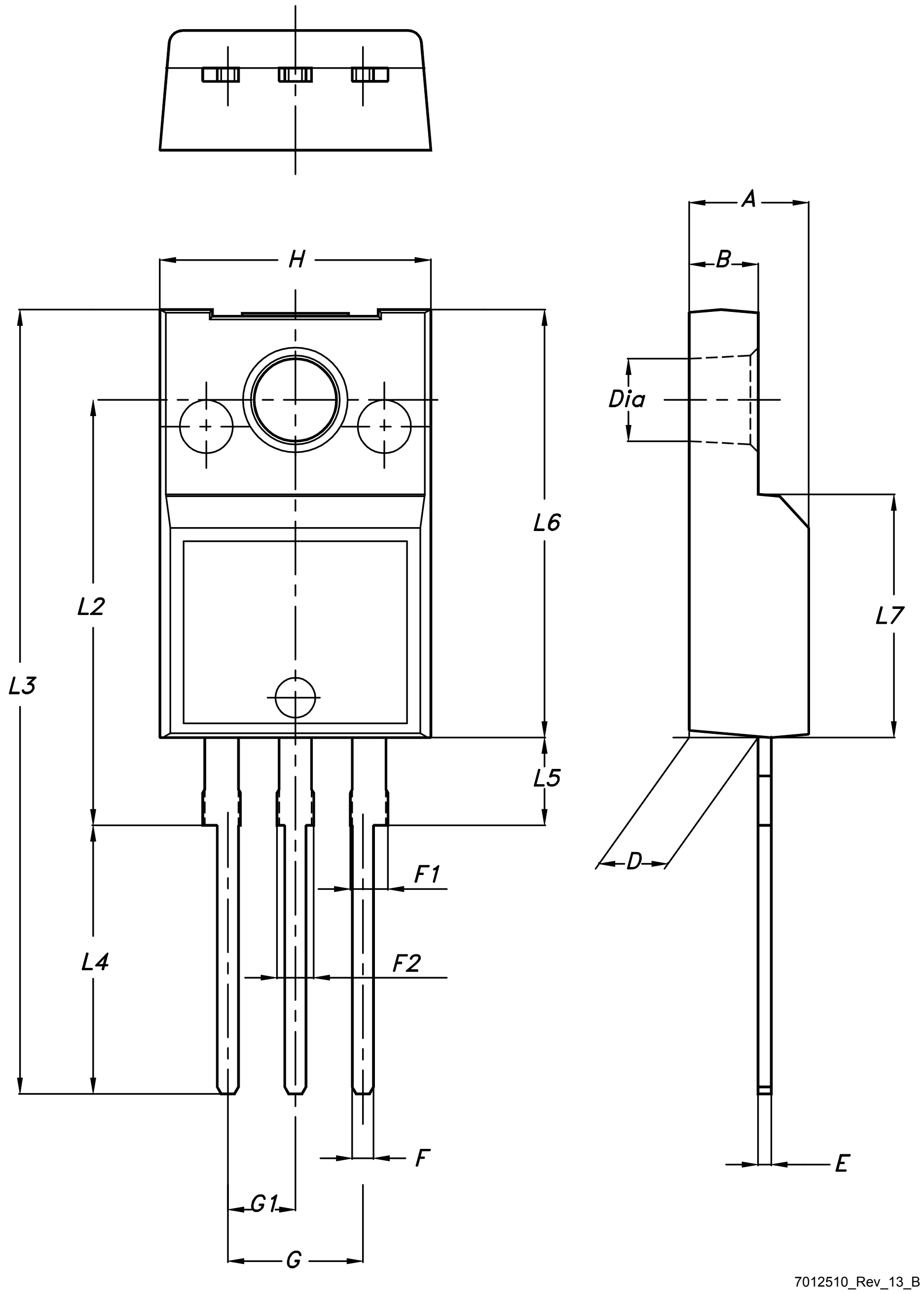


Table 8. **TO-220FP package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
B	2.50		2.70
D	2.50		2.75
E	0.45		0.70
F	0.75		1.00
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.20
G1	2.40		2.70
H	10.00		10.40
L2		16.00	
L3	28.60		30.60
L4	9.80		10.60
L5	2.90		3.60
L6	15.90		16.40
L7	9.00		9.30
Dia	3.00		3.20

Revision history

Table 9. Document revision history

Date	Revision	Changes
10-Dec-2012	1	First release.
20-Dec-2012	2	Added MOSFET dv/dt ruggedness in *Table 2: Absolute maximum ratings*.
14-Jan-2013	3	Modified: *Figure 16, 17*
28-May-2013	4	– Modified: *Figure 16, 17, 18* and *19* – Minor text changes
28-Feb-2014	5	– Modified: $R_{thj\text{-}case}$ value in *Table 3* – Modified: *Figure 12* – Minor text changes
07-Apr-2014	6	– Added: TO-3PF package – Added: *Section 4.3: TO-3PF, STFW24N60M2* – Minor text changes
19-Feb-2020	7	The part numbers STFI24N60M2 and STFW24N60M2 have been moved to a separate datasheet. Removed maturity status indication from cover page. The document status is production data. Minor text changes.

Contents