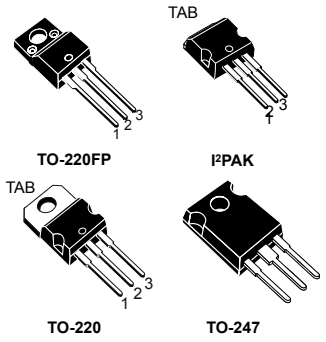
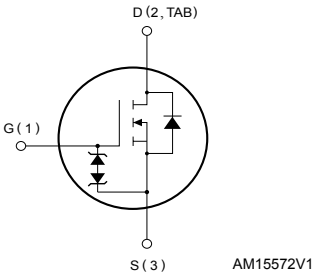
STF33N60M2, STI33N60M2
STP33N60M2, STW33N60M2

Datasheet

N-channel 600 V, 0.108 Ω typ., 26 A, MDmesh M2 Power MOSFETs in TO-220FP, I²PAK, TO-220 and TO-247 packages





Features

Order codes	V_{DS} @ T_{Jmax}	$R_{DS(on)}$ max.	I_D	Package
STF33N60M2	650 V	0.125 Ω	26 A	TO-220FP
STI33N60M2				I²PAK
STP33N60M2				TO-220
STW33N60M2				TO-247

- Extremely low gate charge
- Excellent output capacitance (C_{OSS}) profile
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications
- LLC converters, resonant converters

Description

These devices are N-channel Power MOSFETs developed using the MDmesh M2 technology. Thanks to their strip layout and improved vertical structure, these devices exhibit low on-resistance and optimized switching characteristics, rendering them suitable for the most demanding high-efficiency converters.

Product status links
STF33N60M2
STI33N60M2
STP33N60M2
STW33N60M2

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		TO-220FP	I²PAK, TO-220, TO-247	
V_{GS}	Gate-source voltage	±25		V
I_D	Drain current (continuous) at T_C = 25 °C	26(1)	26	A
	Drain current (continuous) at T_C = 100 °C	16(1)	16	A
I_{DM}(2)	Drain current (pulsed)	104(1)	104	A
P_{TOT}	Total power dissipation at T_C = 25 °C	35	190	W
dv/dt(3)	Peak diode recovery voltage slope	15		V/ns
dv/dt(4)	MOSFET dv/dt ruggedness	50		V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s, T_C = 25 °C)	2500		V
T_{stg}	Storage temperature range	-50 to 150		°C
T_j	Operating junction temperature range			

1. *Limited by maximum junction temperature.*
2. *Pulse width is limited by safe operating area.*
3. *I_{SD} ≤ 26 A, di/dt ≤ 400 A/µs, $V_{DS\ peak}$ < $V_{(BR)DSS}$, V_{DD} = 400 V*
4. *V_{DS} ≤ 480 V*

Table 2. Thermal data

Symbol	Parameter	Value			Unit
		TO-220FP	I²PAK TO-220	TO-247	
$R_{thj\text{-}case}$	Thermal resistance junction-case	3.6	0.66		°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	62.5		50	°C/W

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_{jmax})	5	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	450	mJ

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified).

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0 V	600			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 600 V			1	µA
		V_{GS} = 0 V, V_{DS} = 600 V, T_C = 125 °C(1)			100	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±25 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 13 A		0.108	0.125	Ω

1. *Defined by design, not subject to production test.*

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0 V	-	1781	-	pF
C_{oss}	Output capacitance		-	85	-	pF
C_{rss}	Reverse transfer capacitance		-	2.5	-	pF
$C_{oss\ eq.}$(1)	Equivalent output capacitance	V_{DS} = 0 to 480 V, V_{GS} = 0 V	-	135	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz, I_D = 0 V	-	5.2	-	Ω
Q_g	Total gate charge	V_{DD} = 480 V, I_D = 26 A, V_{GS} = 0 to 10 V (see Figure 19. Test circuit for gate charge behavior)	-	45.5	-	nC
Q_{gs}	Gate-source charge		-	9.9	-	nC
Q_{gd}	Gate-drain charge		-	18.5	-	nC

1. *$C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.*

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 300 V, I_D = 13 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 18. Test circuit for resistive load switching times and Figure 23. Switching time waveform)	-	16	-	ns
t_r	Rise time		-	9.6	-	ns
$t_{d(off)}$	Turn-off delay time		-	109	-	ns
t_f	Fall time		-	9	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		26	A
I_{SDM}(1)	Source-drain current (pulsed)		-		104	A
V_{SD}(2)	Forward on voltage	I_{SD} = 26 A, V_{GS} = 0 V	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 26 A, di/dt = 100 A/µs	-	375		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 60 V	-	5.6		µC
I_{RRM}	Reverse recovery current	(see Figure 20. Test circuit for inductive load switching and diode recovery times)	-	30		A
t_{rr}	Reverse recovery time	I_{SD} = 26 A, di/dt = 100 A/µs	-	478		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 60 V, T_j = 150 °C	-	7.7		µC
I_{RRM}	Reverse recovery current	(see Figure 20. Test circuit for inductive load switching and diode recovery times)	-	35.5		A

1. *Pulse width limited by safe operating area.*
2. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%.*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area for TO-220FP

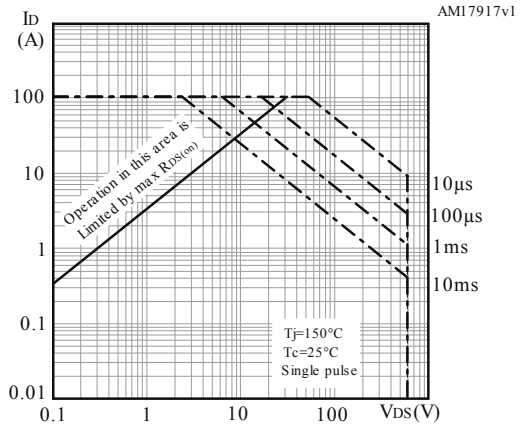


Figure 2. Thermal impedance for TO-220FP

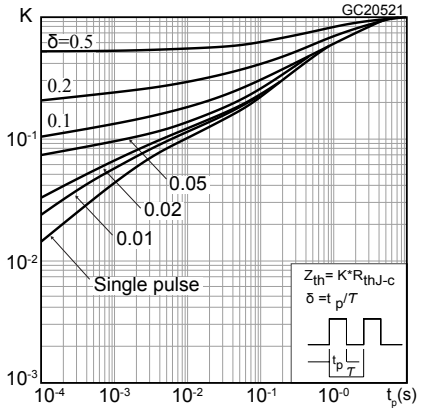


Figure 3. Safe operating area for I²PAK and TO-220

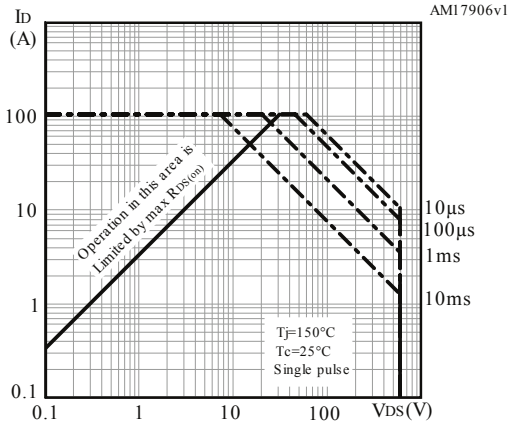


Figure 4. Thermal impedance for I²PAK and TO-220

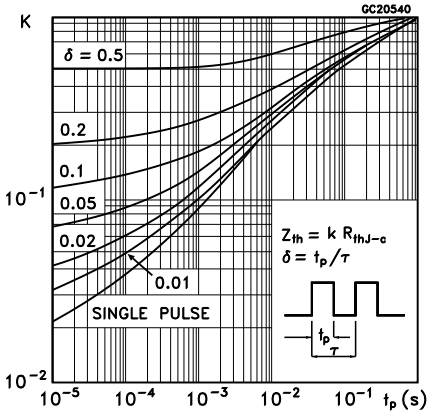


Figure 5. Safe operating area for TO-247

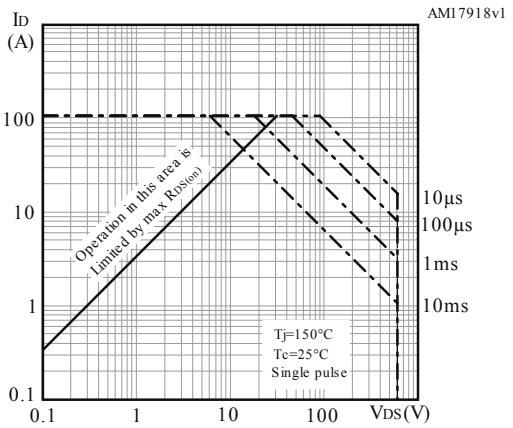


Figure 6. Thermal impedance for TO-247

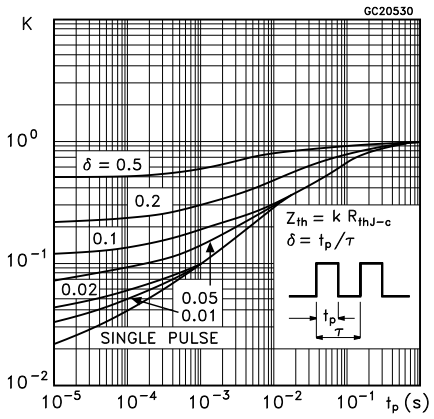


Figure 7. Output characteristics

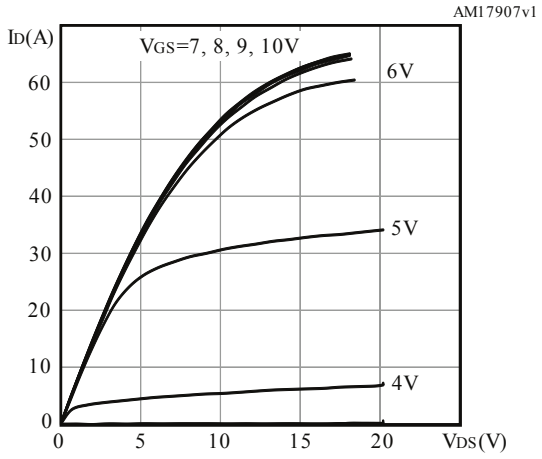


Figure 8. Transfer characteristics

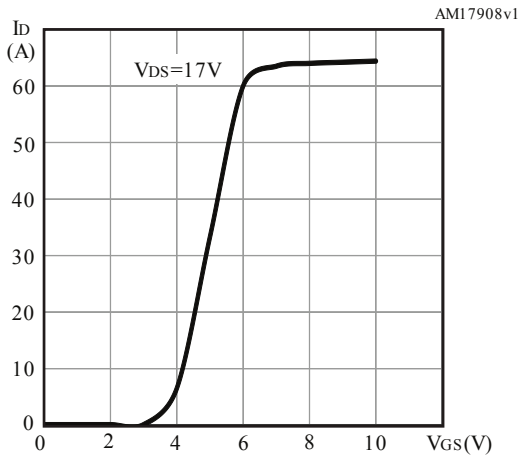


Figure 9. Gate charge vs gate-source voltage

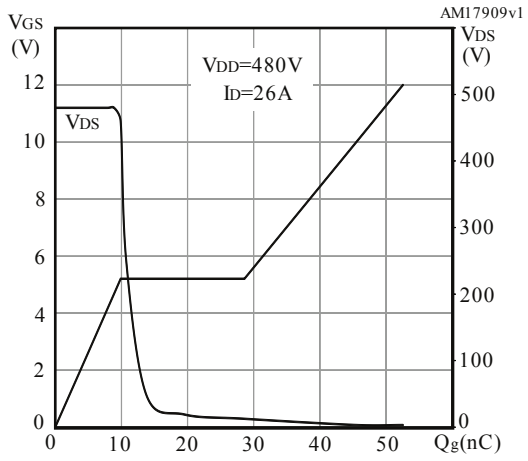


Figure 10. Static drain-source on-resistance

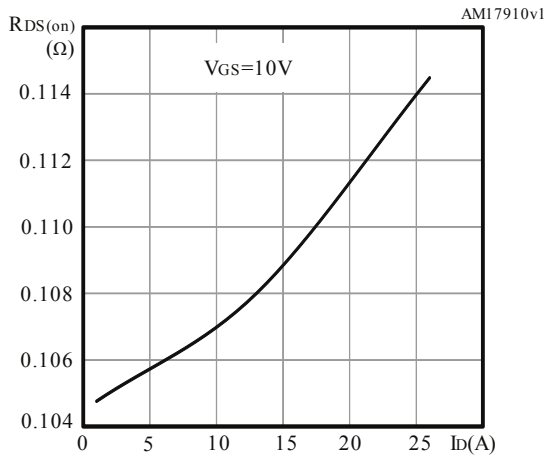


Figure 11. Capacitance variations

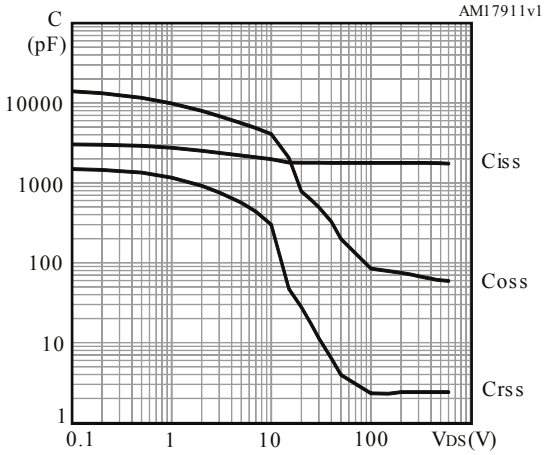


Figure 12. Normalized gate threshold voltage vs temperature

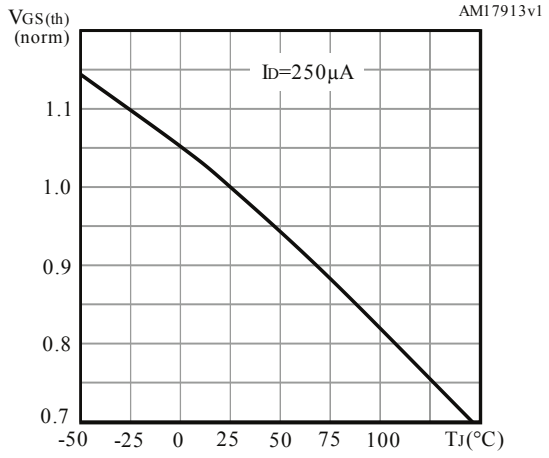


Figure 13. Normalized on-resistance vs temperature

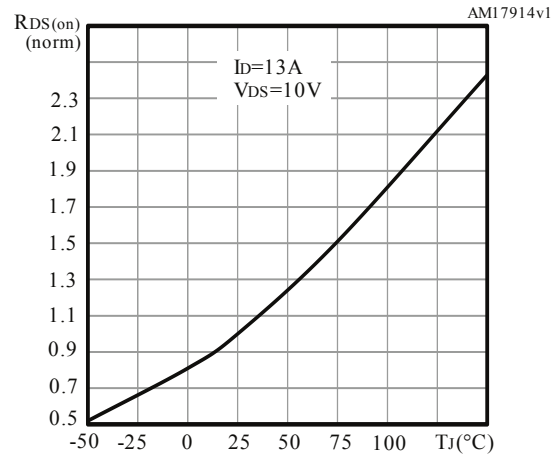


Figure 14. Source-drain diode forward characteristics

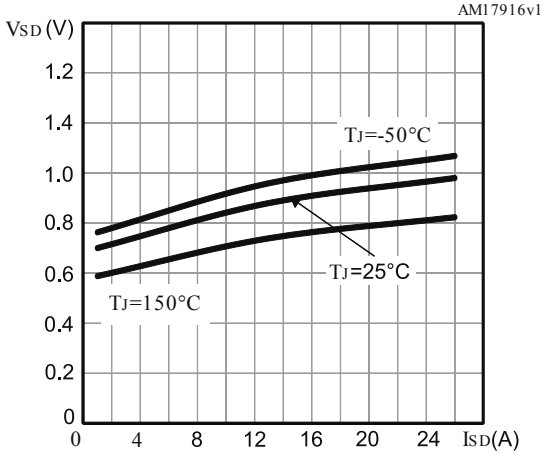


Figure 15. Normalized $V_{(BR)DSS}$ vs temperature

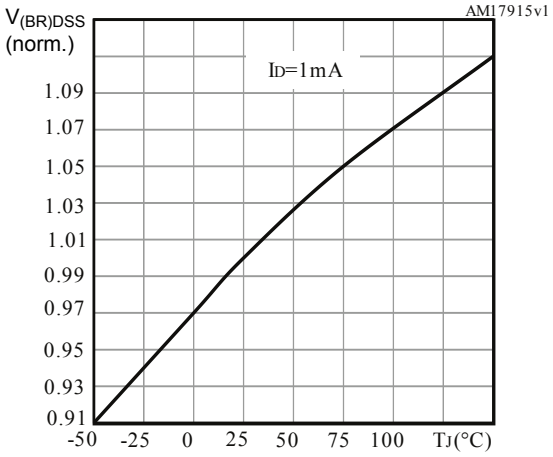


Figure 16. Output capacitance stored energy

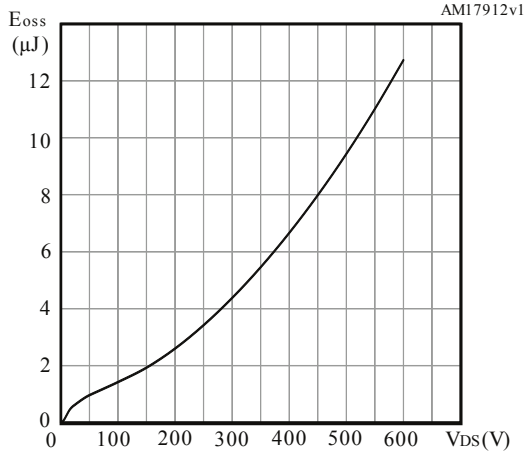
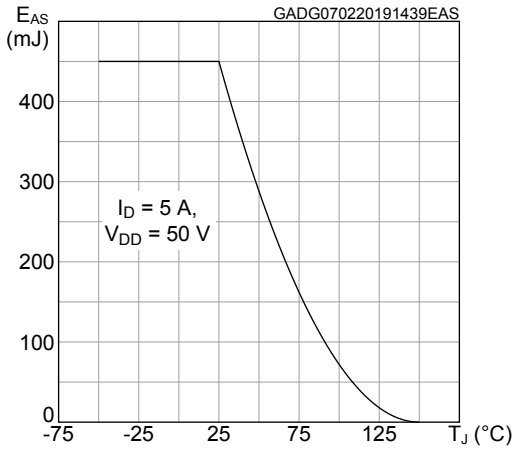


Figure 17. Maximum avalanche energy vs temperature



3 Test circuits

Figure 18. Test circuit for resistive load switching times

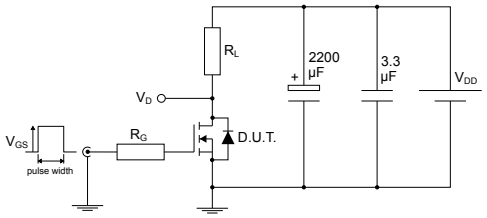


Figure 19. Test circuit for gate charge behavior

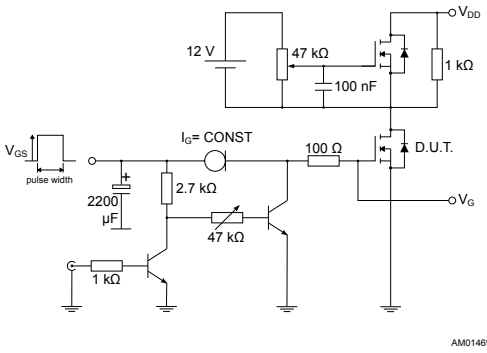


Figure 20. Test circuit for inductive load switching and diode recovery times

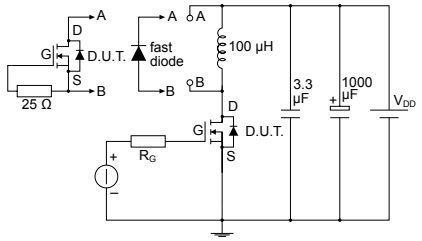


Figure 21. Unclamped inductive load test circuit

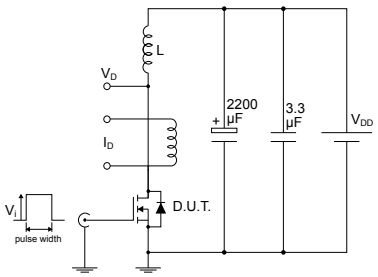


Figure 22. Unclamped inductive waveform

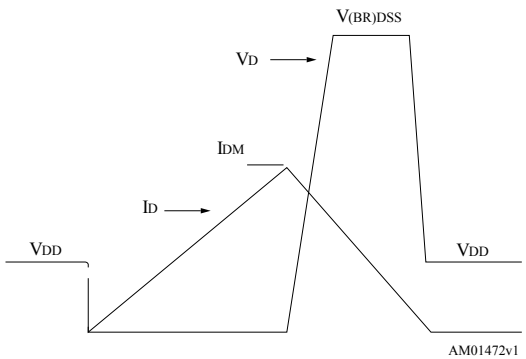
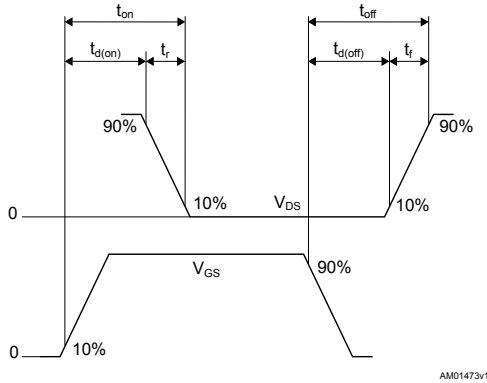


Figure 23. Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 TO-220FP package information

Figure 24. TO-220FP package outline

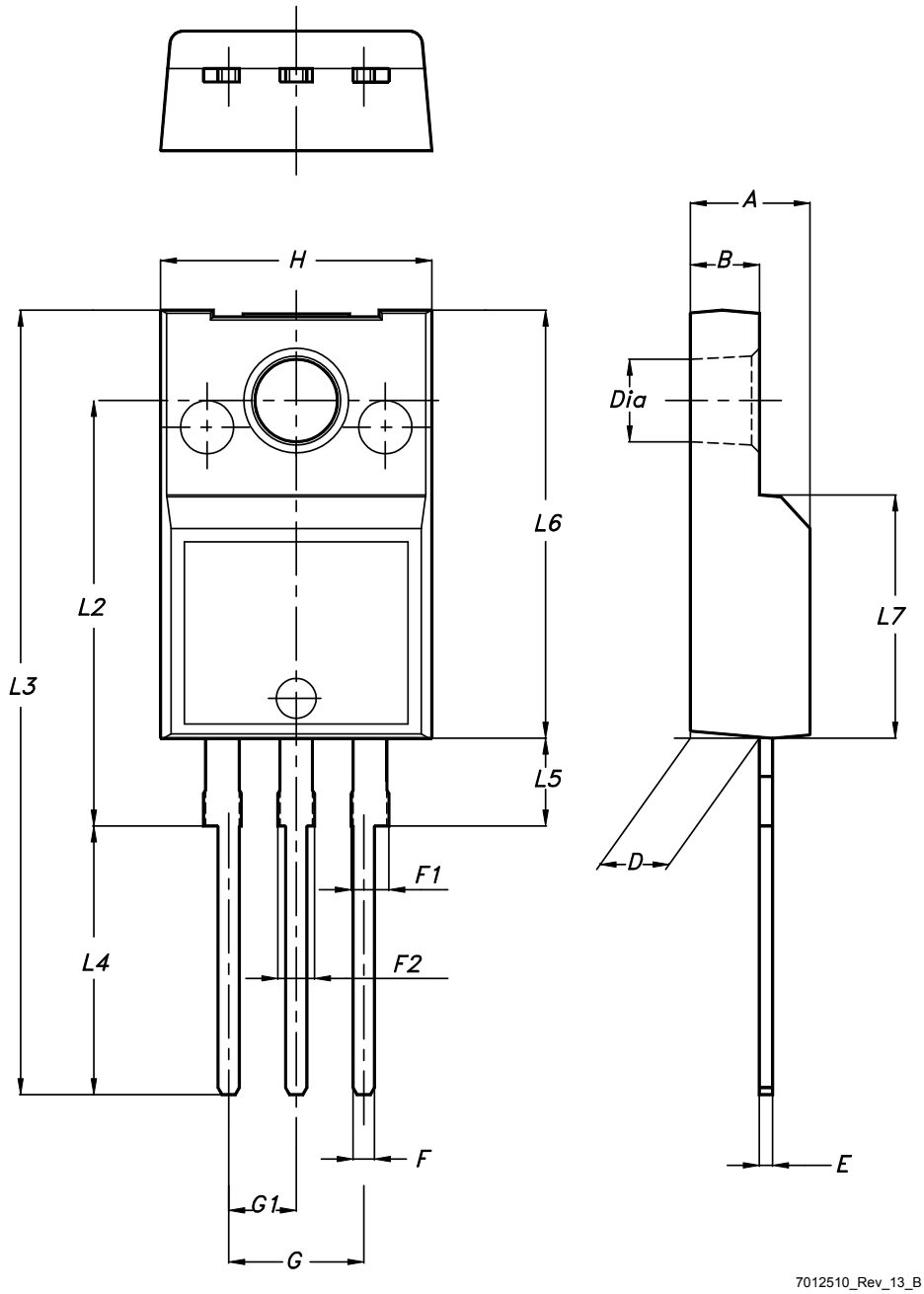


Table 8. **TO-220FP package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
B	2.50		2.70
D	2.50		2.75
E	0.45		0.70
F	0.75		1.00
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.20
G1	2.40		2.70
H	10.00		10.40
L2		16.00	
L3	28.60		30.60
L4	9.80		10.60
L5	2.90		3.60
L6	15.90		16.40
L7	9.00		9.30
Dia	3.00		3.20

4.2 I²PAK package information

Figure 25. I²PAK package outline

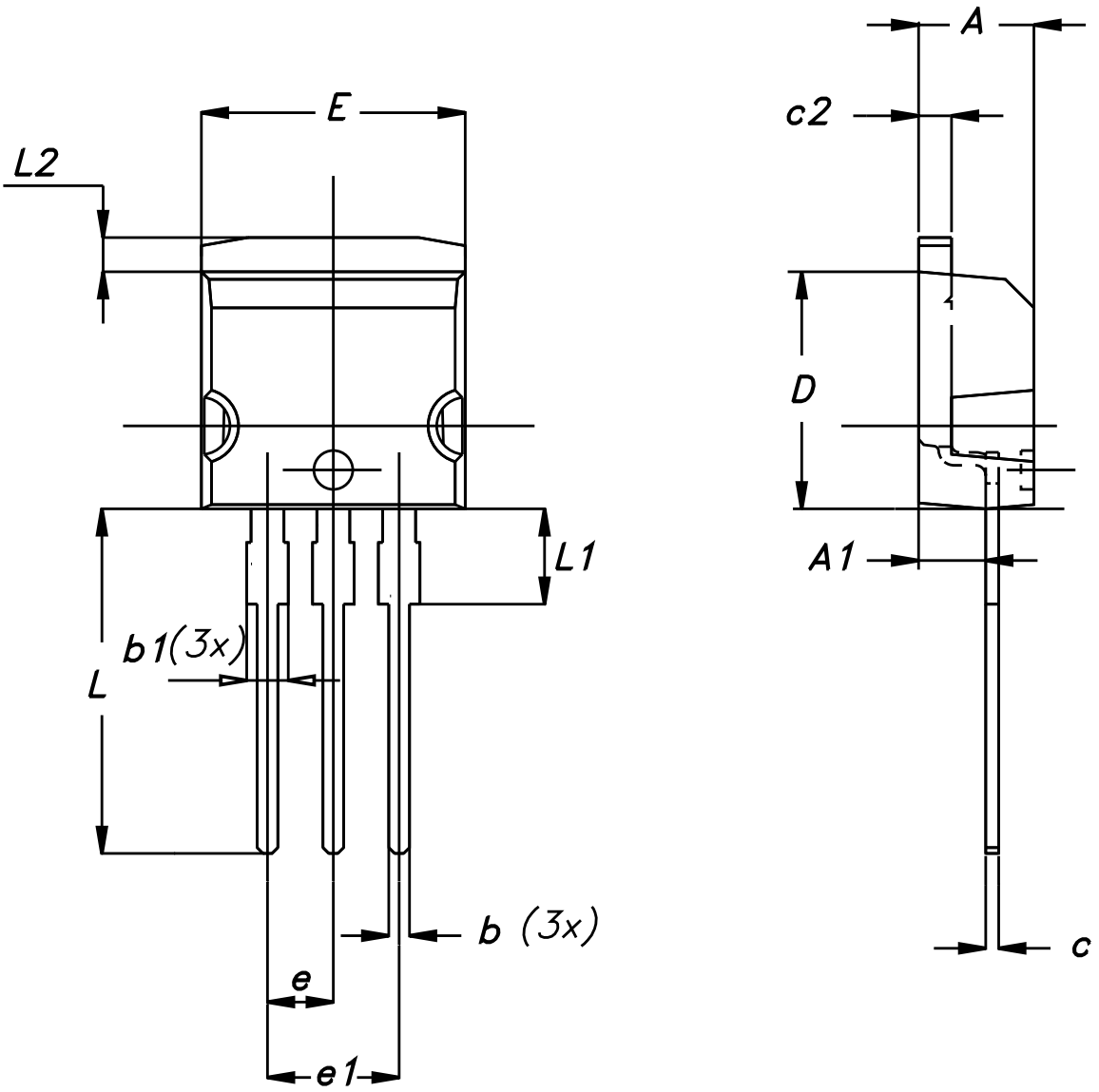


Table 9. I²PAK package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40	-	4.60
A1	2.40	-	2.72
b	0.61	-	0.88
b1	1.14	-	1.70
c	0.49	-	0.70
c2	1.23	-	1.32
D	8.95	-	9.35
e	2.40	-	2.70
e1	4.95	-	5.15
E	10	-	10.40
L	13	-	14
L1	3.50	-	3.93
L2	1.27	-	1.40

4.3 TO-220 type A package information

Figure 26. **TO-220 type A package outline**

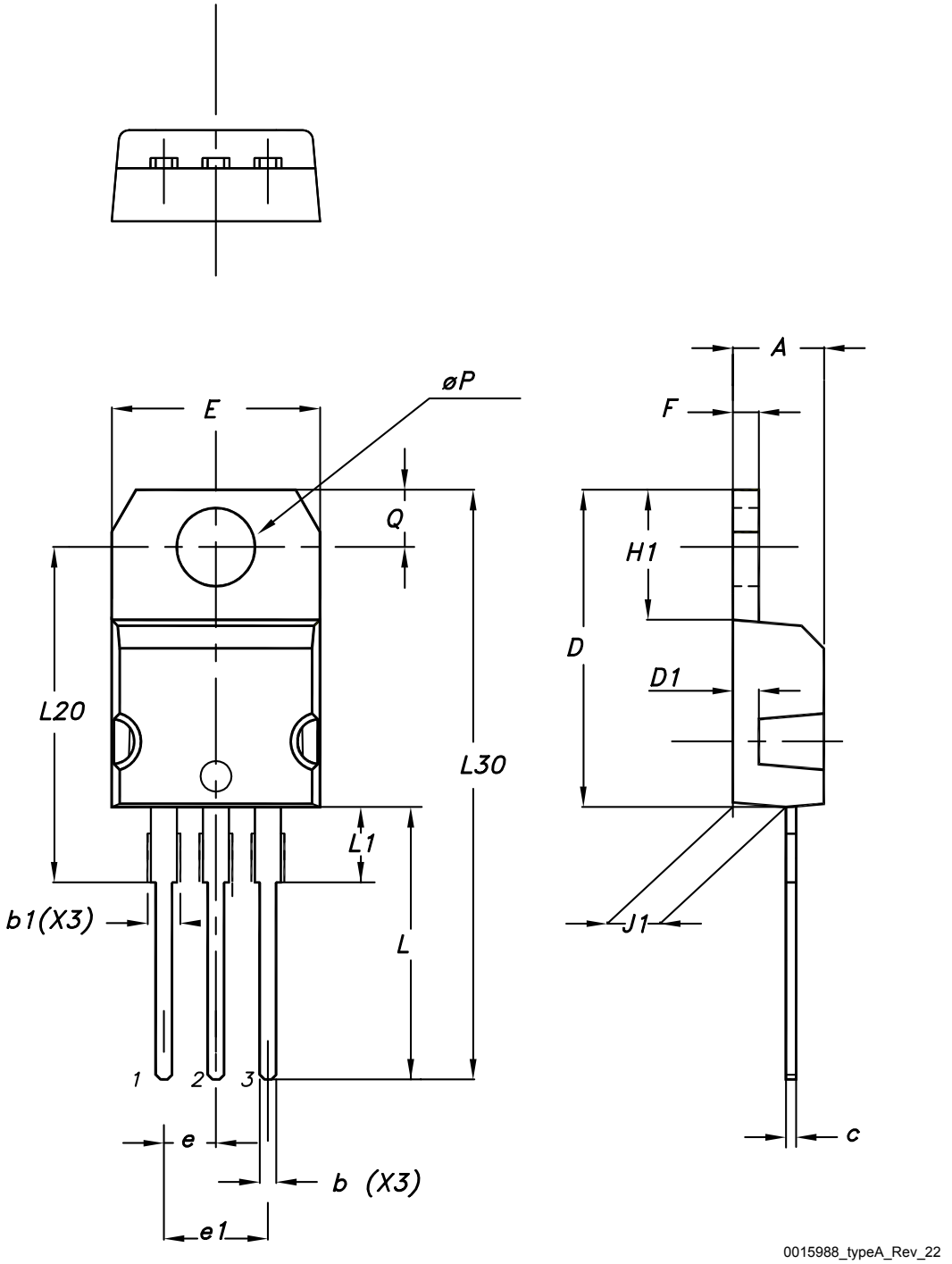
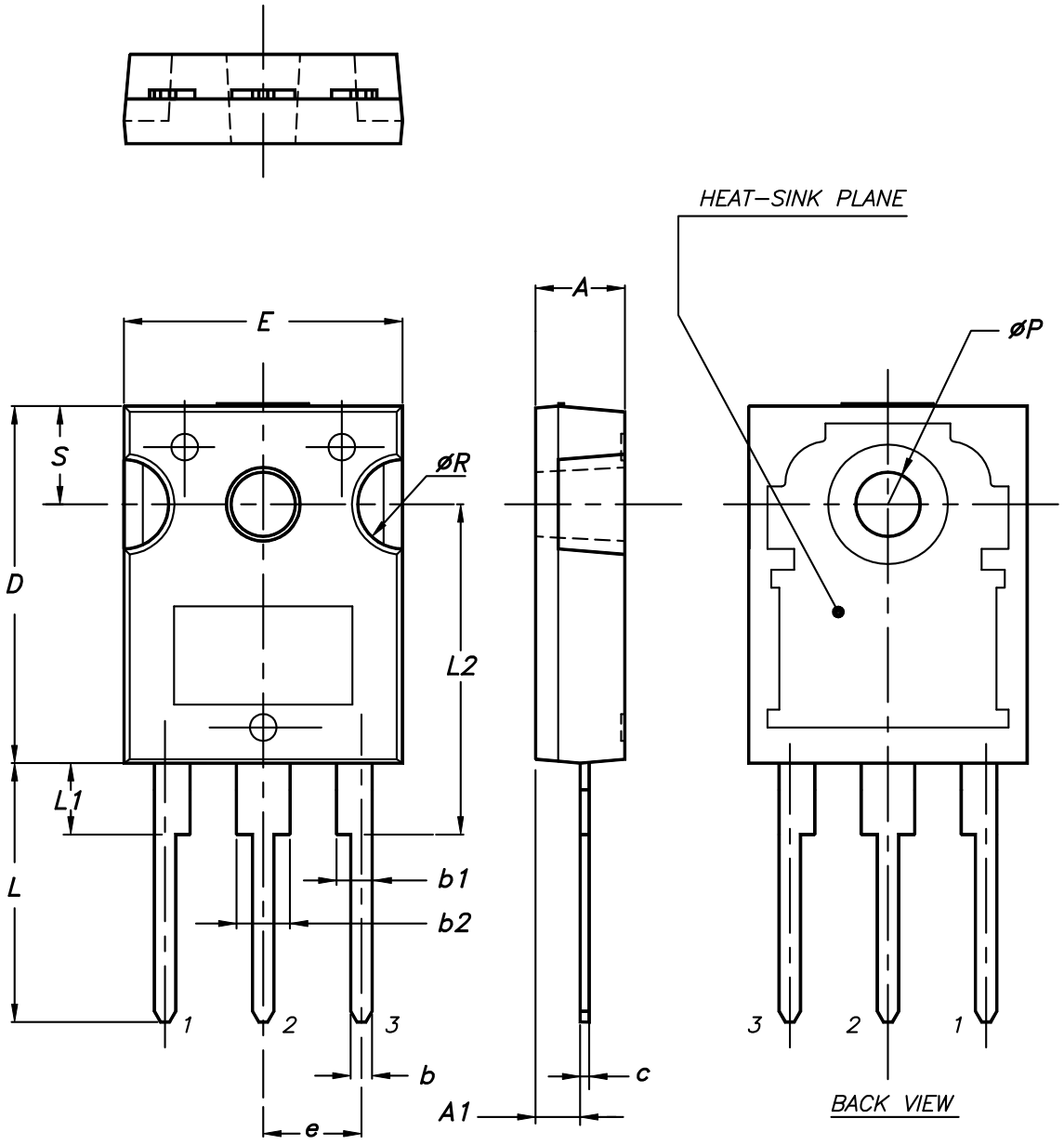


Table 10. **TO-220 type A package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95

4.4 TO-247 package information

Figure 27. **TO-247 package outline**



0075325_9

Table 11. **TO-247 package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70

5 Ordering information

Table 12. **Order codes**

Order code	Marking	Package	Packing
STF33N60M2	33N60M2	TO-220FP	Tube
STI33N60M2		I^2PAK	
STP33N60M2		TO-220	
STW33N60M2		TO-247	

Revision history

Table 13. **Document revision history**

Date	Version	Changes
13-Sep-2013	1	First release.
19-Nov-2013	2	Modified: $R_{DS(on)}$ and I_D values in cover page Modified: values in *Table 4* Modified: $R_{DS(on)}$ typical and maximum values in *Table 5*, the entire typical values in *Table 6, 7* and *8* Added: *Section 2.1: Electrical characteristics (curves)* Minor text changes
14-Jun-2019	3	Removed maturity status indication from cover page. Updated title, features and description. Updated Table 3. Avalanche characteristics. Added Figure 17. Maximum avalanche energy vs temperature. Minor text changes

Contents