

N-channel 650 V, 0.160 Ω typ., 18 A MDmesh M5 Power MOSFETs in TO-220FP, I²PAKFP and TO-3PF packages

Datasheet - production data

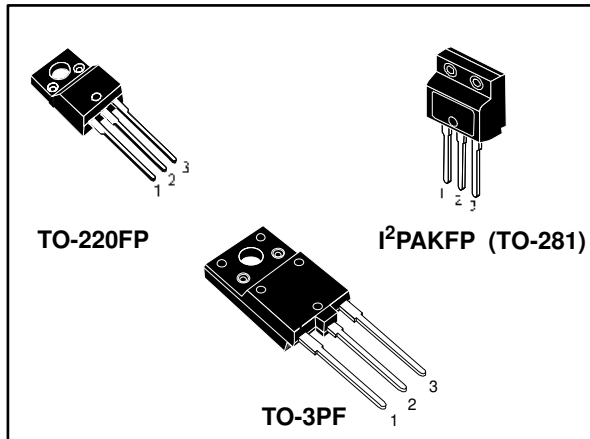
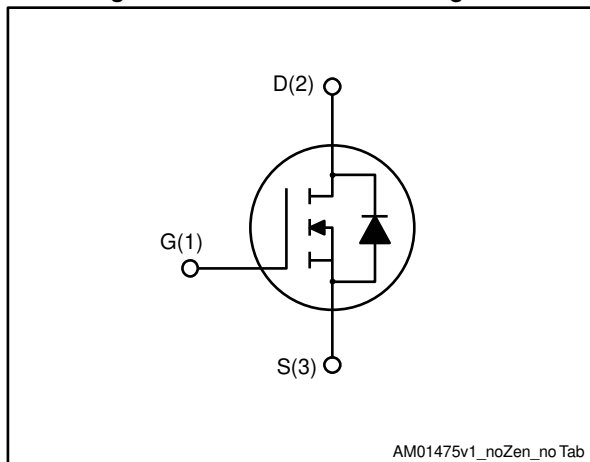


Figure 1: Internal schematic diagram



Features

Order code	V _{DS} @ T _{Jmax}	R _{DS(on)} max	I _D
STF20N65M5	710 V	0.190 Ω	18 A
STF120N65M5			
STFW20N65M5			

- Extremely low R_{DS(on)}
- Low gate charge and input capacitance
- Excellent switching performance
- 100% avalanche tested

Applications

- Switching applications

Description

These devices are N-channel Power MOSFET based on the MDmesh™ M5 innovative vertical process technology combined with the well-known PowerMESH™ horizontal layout. The resulting products offer extremely low on-resistance, making them particularly suitable for applications requiring high power and superior efficiency.

Table 1: Device summary

Order code	Marking	Package	Packaging
STF20N65M5	20N65M5	TO-220FP	Tube
STF120N65M5		I ² PAKFP (TO-281)	
STFW20N65M5		TO-3PF	

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value		Unit
		TO-220FP, I ² PAKFP	TO-3PF	
V _{GS}	Gate- source voltage	±25		V
I _D	Drain current (continuous) at T _C = 25 °C	18 ⁽¹⁾		A
I _D	Drain current (continuous) at T _C = 100 °C	11.3 ⁽¹⁾		A
I _{DM} ⁽²⁾	Drain current (pulsed)	36 ⁽¹⁾		A
P _{TOT}	Total dissipation at T _C = 25 °C	30	48	W
dv/dt ⁽³⁾	Peak diode recovery voltage slope	15		V/ns
V _{ISO} ⁽⁴⁾	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s; T _C = 25 °C)	2500	3500	V
T _{stg}	Storage temperature range	- 55 to 150		°C
T _j	Operating junction temperature range			

Notes:

⁽¹⁾Limited by maximum junction temperature.

⁽²⁾Pulse width limited by safe operating area

⁽³⁾I_{SD} ≤ 18 A, di/dt = 400 A/μs, V_{DS(peak)} < V_{(BR)DSS}, V_{DD} = 400 V

⁽⁴⁾V_{DS} ≤ 520 V

Table 3: Thermal data

Symbol	Parameter	Value		Unit
		TO-220FP, I ² PAKFP	TO-3PF	
R _{thj-case}	Thermal resistance junction-case	4.17	2.6	°C/W
R _{thj-amb}	Thermal resistance junction-ambient	62.5	50	°C/W

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I _{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T _{jmax})	4	°C/W
E _{AS}	Single pulse avalanche energy (starting T _J = 25 °C, I _D = I _{AR} , V _{DD} = 50 V)	270	mJ

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 5: On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	V _{GS} = 0, I _D = 1 mA	650			V
I _{DSS}	Zero gate voltage drain current	V _{GS} = 0, V _{DS} = 650 V			1	μA
		V _{GS} = 0, V _{DS} = 650 V, T _C = 125 °C ⁽¹⁾			100	μA
I _{GSS}	Gate-body leakage current	V _{DS} = 0, V _{GS} = ± 25 V			±100	nA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 250 μA	3	4	5	V
R _{DS(on)}	Static drain-source on-resistance	V _{GS} = 10 V, I _D = 9 A		0.160	0.190	Ω

Notes:

⁽¹⁾Defined by design, not subject to production test

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C _{iss}	Input capacitance	V _{GS} = 0, V _{DS} = 100 V, f = 1 MHz	-	1434	-	pF
C _{oss}	Output capacitance		-	38	-	pF
C _{rss}	Reverse transfer capacitance		-	3.7	-	pF
C _{o(tr)} ⁽¹⁾	Equivalent capacitance time related	V _{GS} = 0, V _{DS} = 0 to 520 V	-	118	-	pF
C _{o(er)} ⁽²⁾	Equivalent capacitance energy related		-	35	-	pF
R _G	Intrinsic gate resistance	f = 1 MHz, I _D = 0 A	-	3.5	-	Ω
Q _g	Total gate charge	V _{DD} = 520 V, I _D = 9 A, V _{GS} = 0 to 10 V (see Figure 18: "Test circuit for gate charge behavior")	-	36	-	nC
Q _{gs}	Gate-source charge		-	7.5	-	nC
Q _{gd}	Gate-drain charge		-	18	-	nC

Notes:

⁽¹⁾C_{o(tr)} is a constant capacitance value that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

⁽²⁾C_{o(er)} is a constant capacitance value that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(V)}$	Voltage delay time	$V_{DD} = 400 \text{ V}$, $I_D = 12 \text{ A}$, $R_G = 4.7 \text{ } \Omega$, $V_{GS} = 10 \text{ V}$ (see Figure 19: "Test circuit for inductive load switching and diode recovery times" and Figure 22: "Switching time waveform")	-	43	-	ns
$t_{r(V)}$	Voltage rise time		-	7.5	-	ns
$t_{f(i)}$	Current fall time		-	7.5	-	ns
$t_{c(off)}$	Crossing time		-	11.5	-	ns

Table 8: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		18	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		36	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 18 \text{ A}$, $V_{GS} = 0$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 18 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 100 \text{ V}$ (see Figure 19: "Test circuit for inductive load switching and diode recovery times")	-	288		ns
Q_{rr}	Reverse recovery charge		-	4		μC
I_{RRM}	Reverse recovery current		-	27		A
t_{rr}	Reverse recovery time	$I_{SD} = 18 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 100 \text{ V}$, $T_j = 150 \text{ }^\circ\text{C}$ (see Figure 19: "Test circuit for inductive load switching and diode recovery times")	-	342		ns
Q_{rr}	Reverse recovery charge		-	4.7		μC
I_{RRM}	Reverse recovery current		-	28		A

Notes:

(1)Pulse width limited by safe operating area

(2)Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curve)

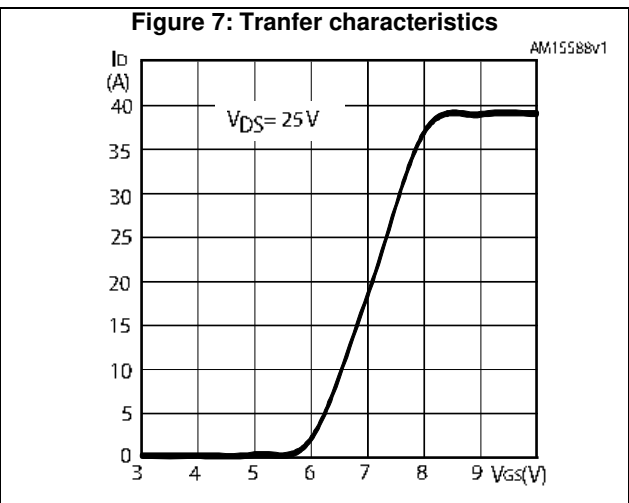
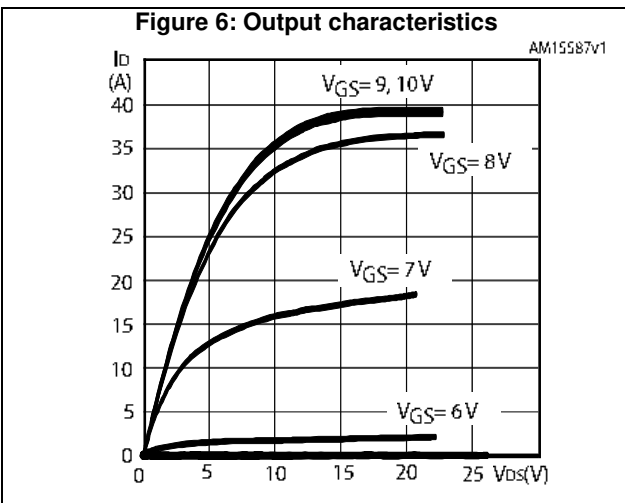
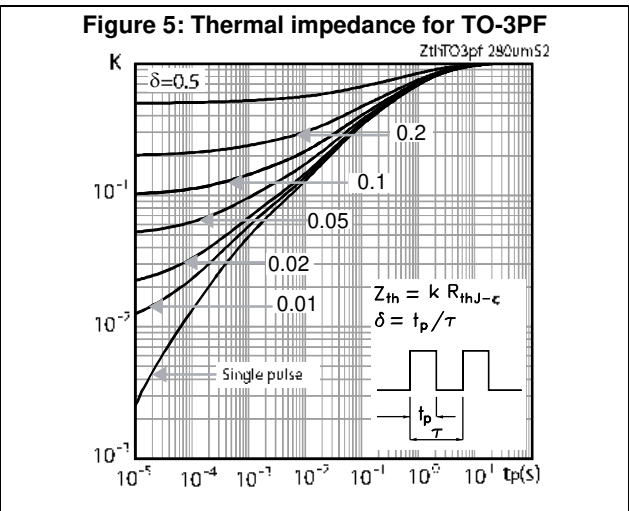
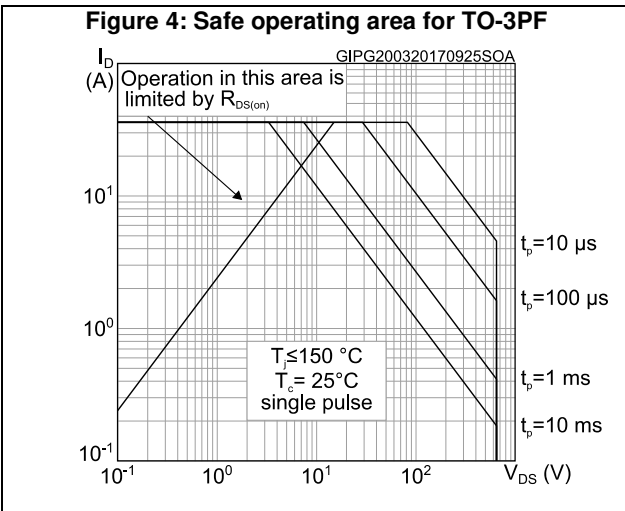
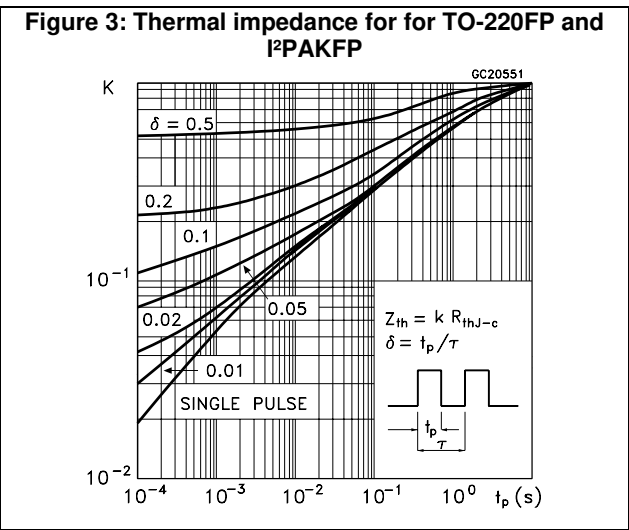
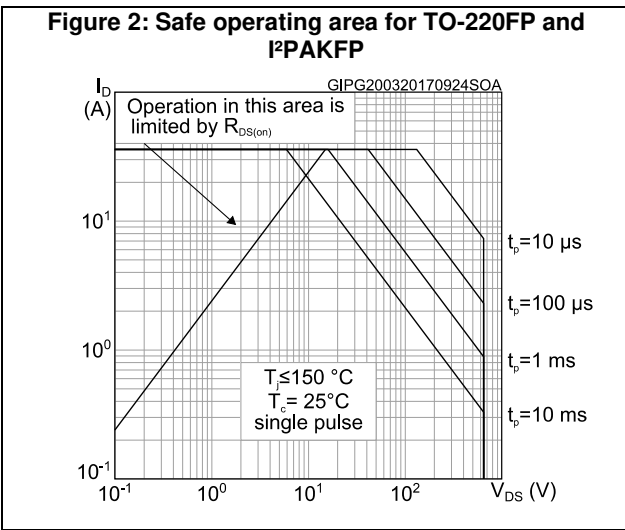


Figure 8: Gate charge vs gate-source voltage

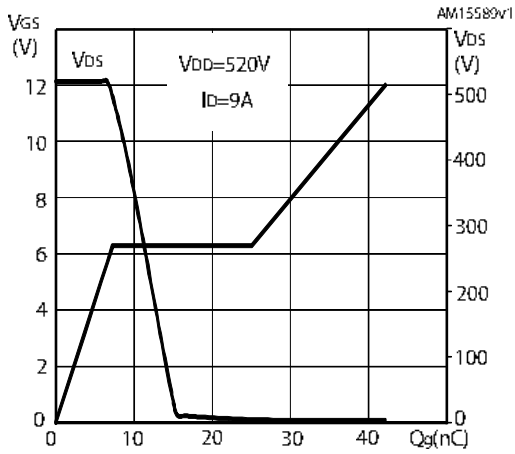


Figure 9: Static drain-source on-resistance

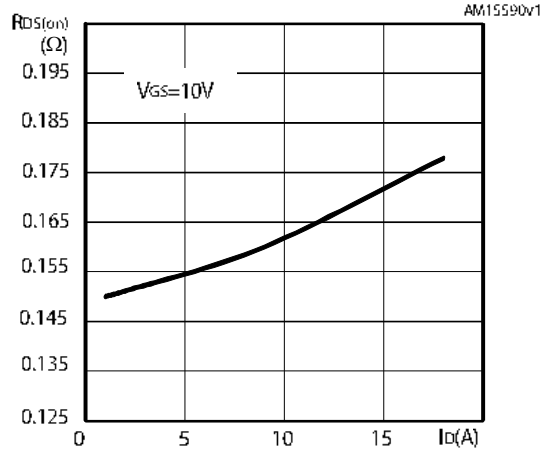


Figure 10: Capacitance variations

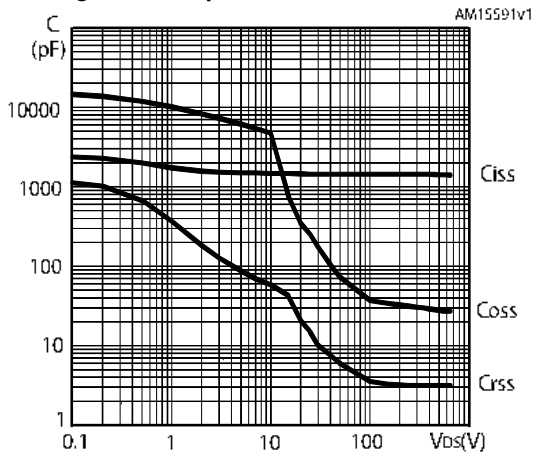


Figure 11: Output capacitance stored energy

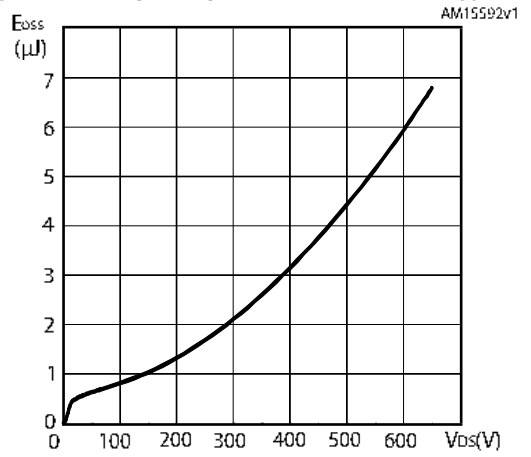


Figure 12: Normalized gate threshold voltage vs temperature

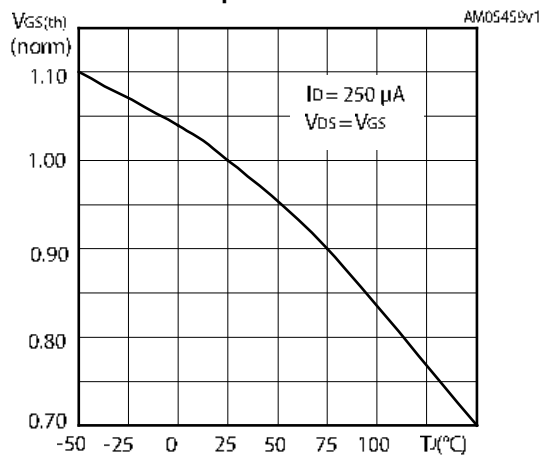
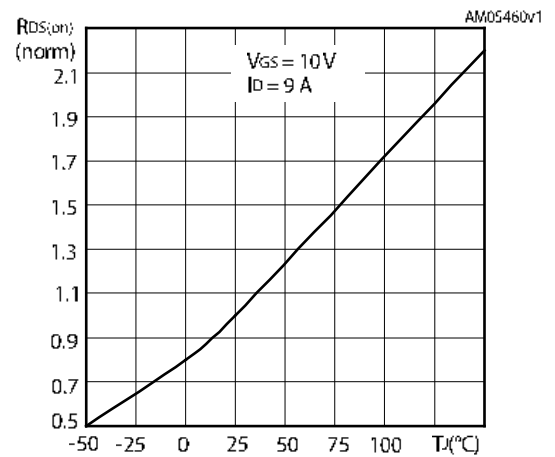
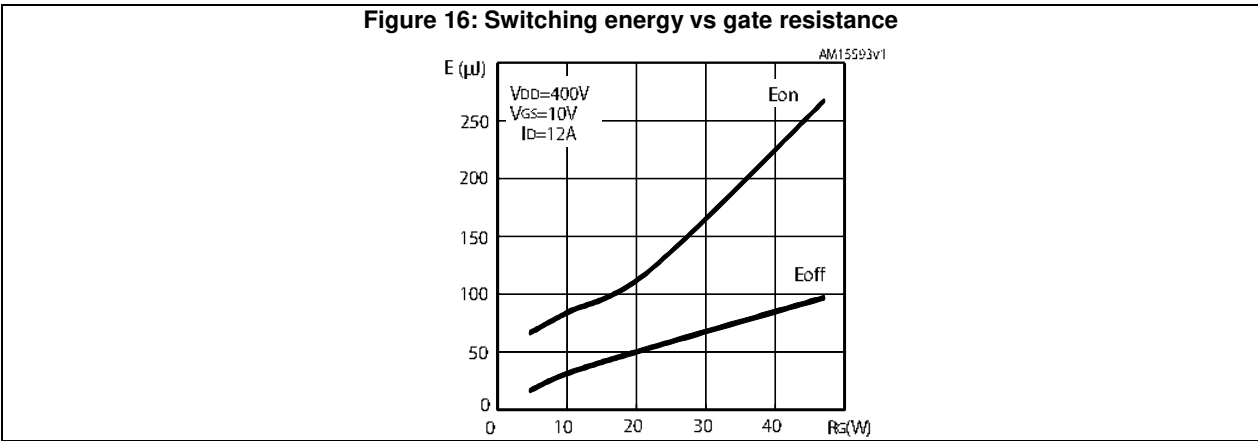
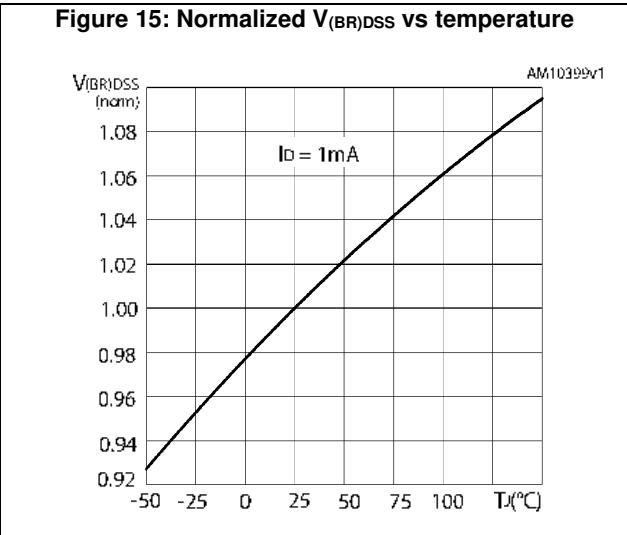
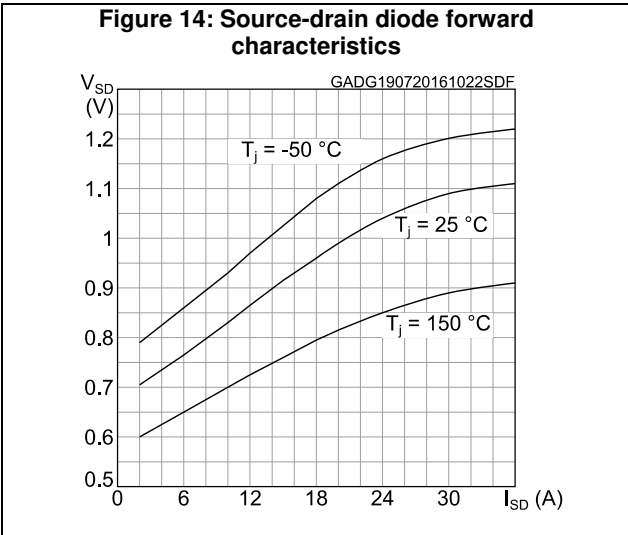


Figure 13: Normalized on-resistance vs temperature



Electrical characteristics

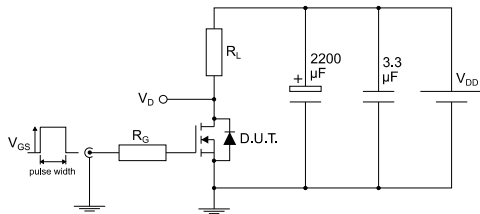
STF20N65M5,STFI20N65M5,STFW20N65M5



E_{on} including reverse recovery of a SiC diode.

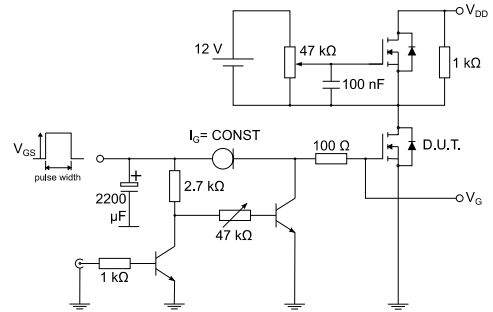
3 Test circuits

Figure 17: Test circuit for resistive load switching times



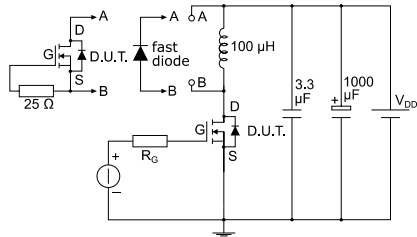
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Figure 18: Test circuit for gate charge behavior



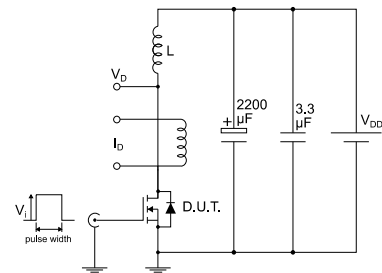
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Figure 19: Test circuit for inductive load switching and diode recovery times



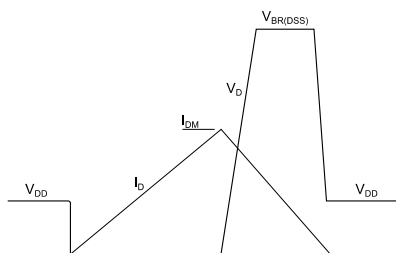
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Figure 20: Unclamped inductive load test circuit



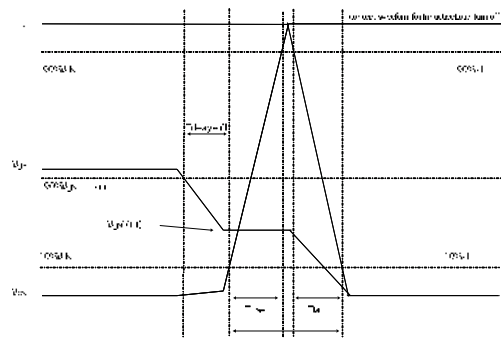
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Figure 21: Unclamped inductive waveform



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Figure 22: Switching time waveform



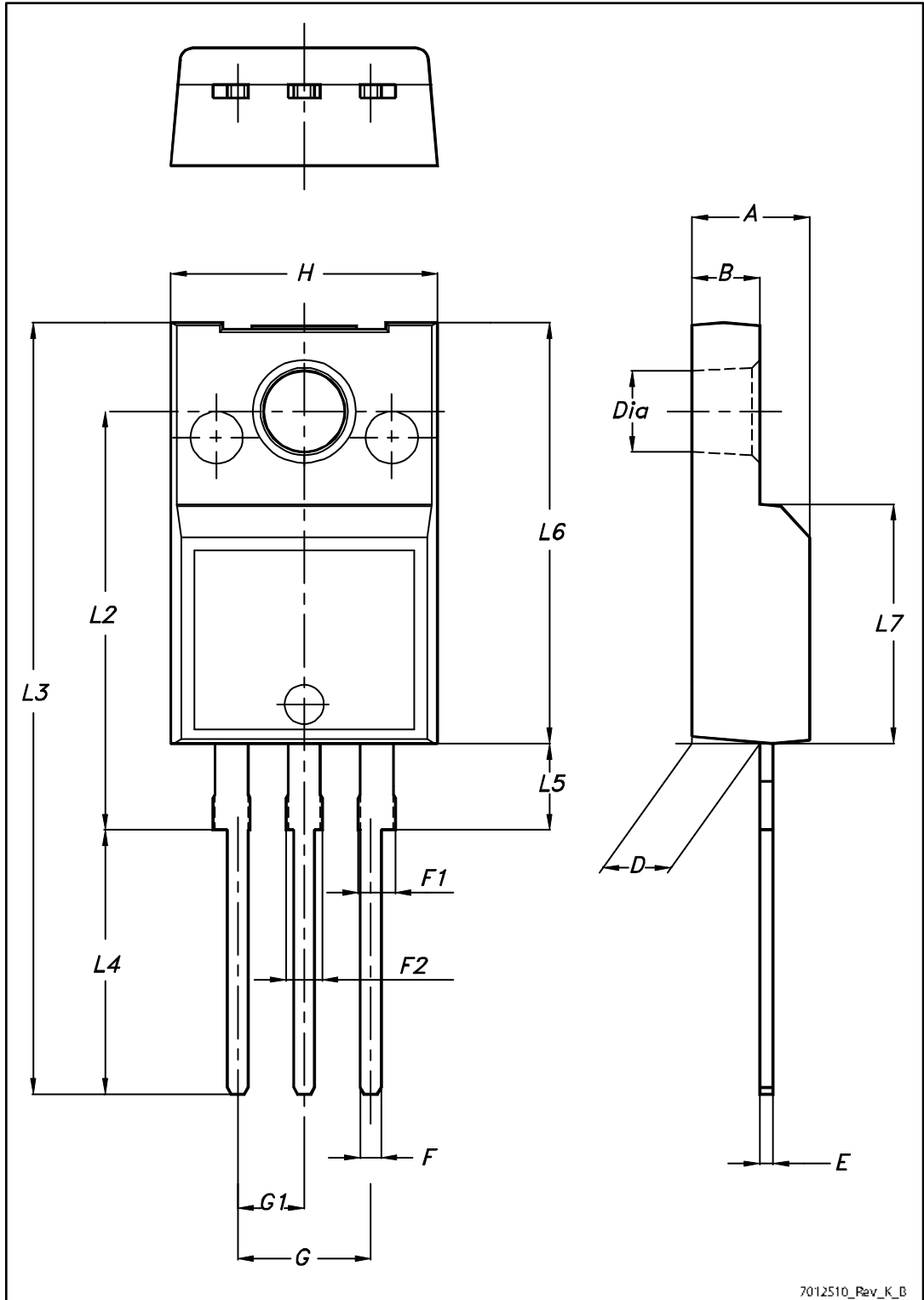
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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 TO-220FP package information

Figure 23: TO-220FP package outline



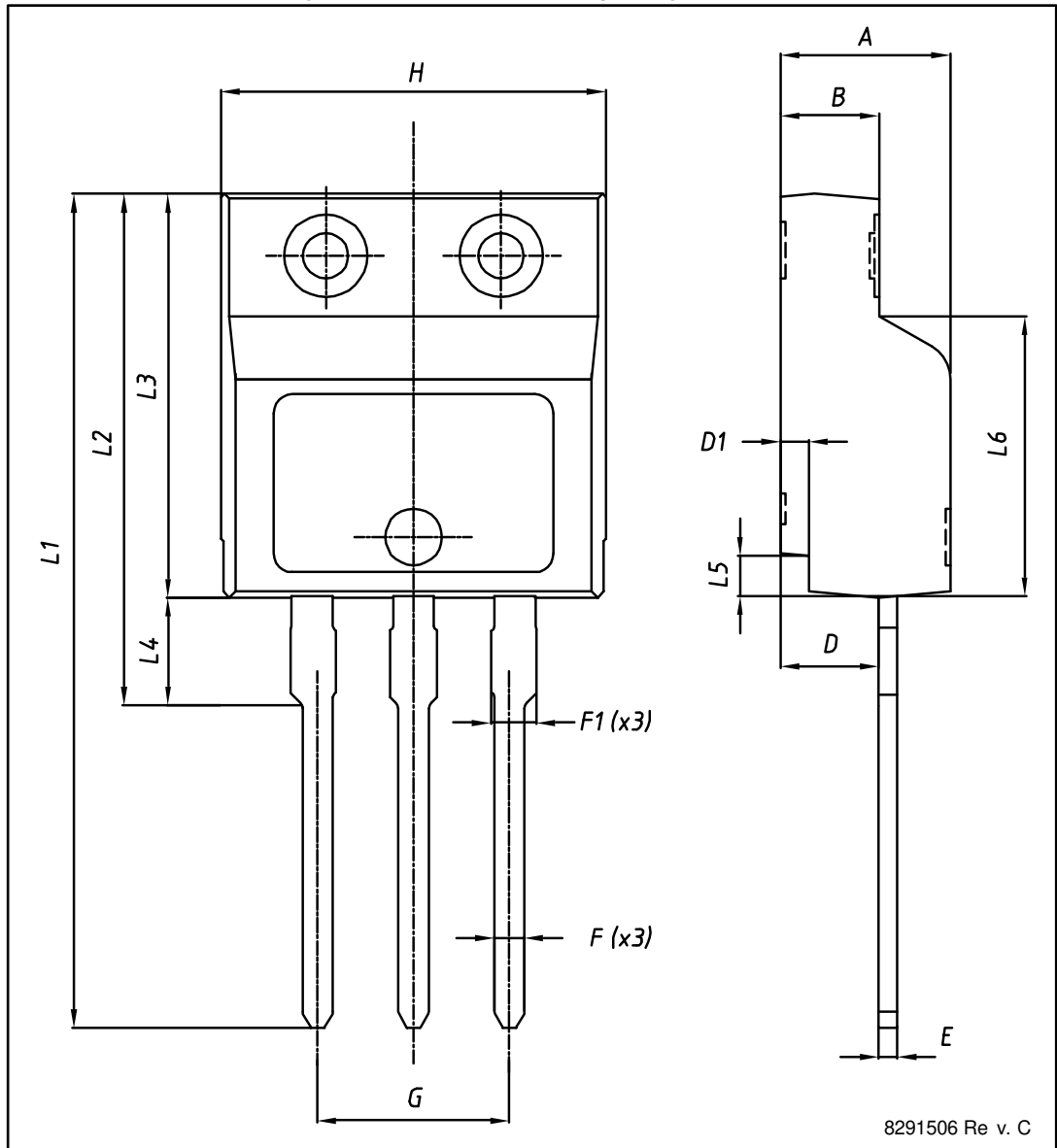
7012510_Rev_K_B

Table 9: TO-220FP package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

4.2 I²PAKFP (TO-281) package information

Figure 24: I²PAKFP (TO-281) package outline



8291506 Re v. C

Table 10: I²PAKFP (TO-281) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
B	2.50		2.70
D	2.50		2.75
D1	0.65		0.85
E	0.45		0.70
F	0.75		1.00
F1			1.20
G	4.95		5.20
H	10.00		10.40
L1	21.00		23.00
L2	13.20		14.10
L3	10.55		10.85
L4	2.70		3.20
L5	0.85		1.25
L6	7.50	7.60	7.70

4.3 TO-3PF package information

Figure 25: TO-3PF package outline

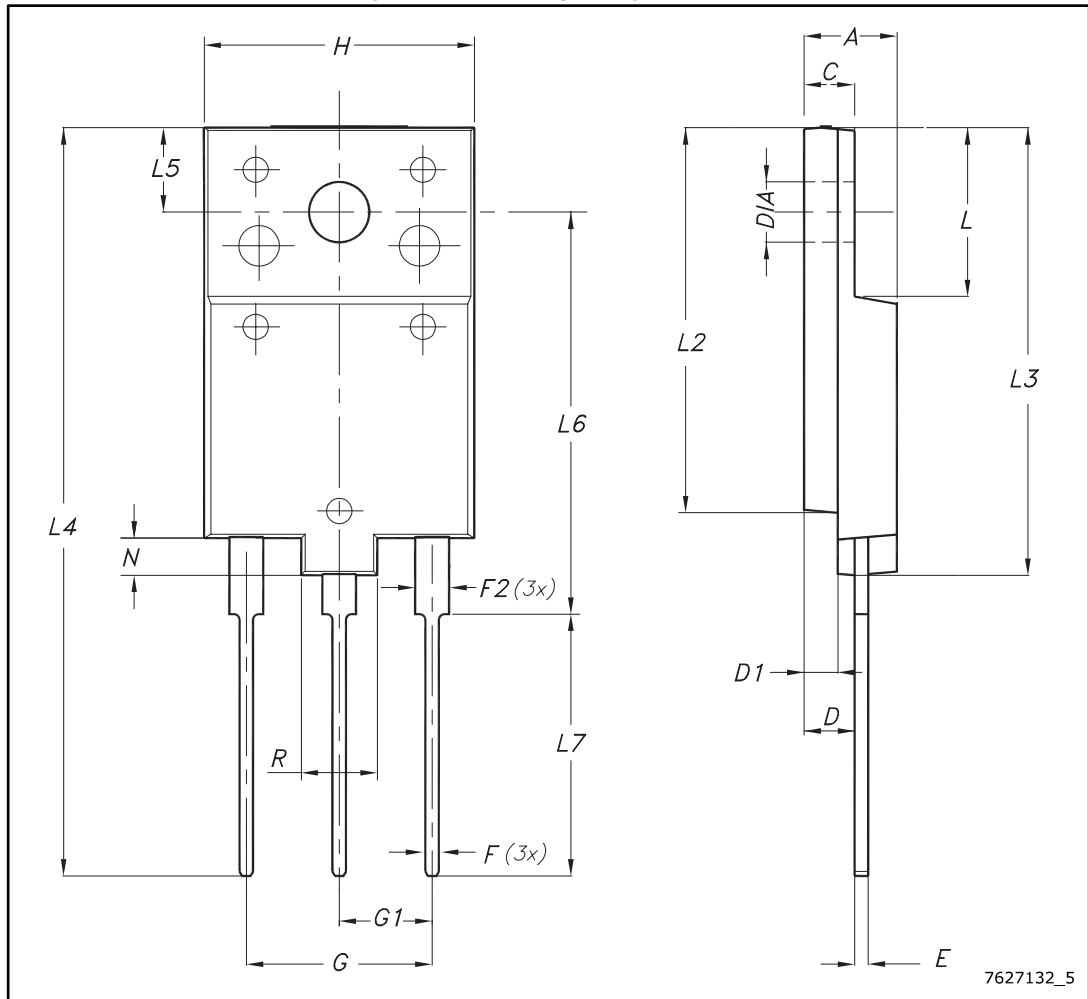


Table 11: TO-3PF mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	5.30		5.70
C	2.80		3.20
D	3.10		3.50
D1	1.80		2.20
E	0.80		1.10
F	0.65		0.95
F2	1.80		2.20
G	10.30		11.50
G1		5.45	
H	15.30		15.70
L	9.80	10	10.20
L2	22.80		23.20
L3	26.30		26.70
L4	43.20		44.40
L5	4.30		4.70
L6	24.30		24.70
L7	14.60		15
N	1.80		2.20
R	3.80		4.20
Dia	3.40		3.80

5 Revision history

Table 12: Document revision history

Date	Revision	Changes
01-Feb-2013	1	First release. Part numbers previously included in datasheet DM00049308
21-Jul-2016	2	Added device in TO-3PF. Modified: <i>Table 2: "Absolute maximum ratings", Table 5: "On /off states"</i> . Modified: <i>Figure 2: "Safe operating area for TO-220FP and I²PAKFP", Figure 4: "Safe operating area for TO-3PF", Figure 5: "Thermal impedance for TO-3PF"</i> . Minor text changes
22-Mar-2017	3	Modified <i>Table 2: "Absolute maximum ratings", Table 8: "Source drain diode"</i> . Modified <i>Figure 2: "Safe operating area for TO-220FP and I²PAKFP", Figure 4: "Safe operating area for TO-3PF", Figure 12: "Normalized gate threshold voltage vs temperature ", Figure 13: "Normalized on-resistance vs temperature" and Figure 14: "Source-drain diode forward characteristics "</i> . Minor text changes.

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