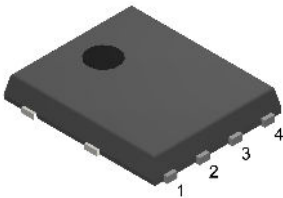
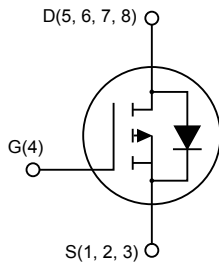


## P-channel 30 V, 24 mΩ typ., 9 A STripFET F6 DeepGATE Power MOSFET in a PowerFLAT 5x6 package


**PowerFLAT 5x6**


AM01475v4


**Product status link**
[STL30P3LLH6](#)
**Product summary**

<b>Order code</b>	STL30P3LLH6
<b>Marking</b>	30P3L
<b>Package</b>	PowerFLAT 5x6
<b>Packing</b>	Tape and reel

### Features

Order code	V <sub>DS</sub>	R <sub>DS(on)</sub> max.	I <sub>D</sub>	P <sub>TOT</sub>
STL30P3LLH6	30 V	30 mΩ	9 A	4.8 W

- Very low on-resistance
- Very low gate charge
- High avalanche ruggedness
- Low gate drive power loss

### Applications

- Switching applications

### Description

This device is a P-channel Power MOSFET developed using the STripFET F6 technology, with a new trench gate structure. The resulting Power MOSFET exhibits very low R<sub>DS(on)</sub> in all packages.

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	30	V
$V_{GS}$	Gate-source voltage	±20	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ °C}$	30	A
	Drain current (continuous) at $T_C = 100\text{ °C}$	18.75	A
$I_D^{(2)}$	Drain current (continuous) at $T_{pcb} = 25\text{ °C}$	9	A
	Drain current (continuous) at $T_{pcb} = 100\text{ °C}$	6.4	A
$I_{DM}^{(2)(3)}$	Drain current (pulsed)	36	A
$P_{TOT}^{(1)}$	Total power dissipation at $T_C = 25\text{ °C}$	75	W
$P_{TOT}^{(2)}$	Total power dissipation at $T_{pcb} = 25\text{ °C}$	4.8	W
	Derating factor <sup>(2)</sup>	0.03	W/°C
$T_{stg}$	Storage temperature range	-55 to 175	°C
$T_J$	Operating junction temperature range	175	°C

1. This value is rated according to  $R_{thj-c}$ .
2. This value is rated according to  $R_{thj-pcb}$ .
3. Pulse width is limited by safe operating area.

**Table 2. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	2.00	°C/W
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb, single operation	31.3	°C/W

1. When mounted on an FR-4 board of 1 inch<sup>2</sup>, 2oz Cu, steady state.

**Note:** For the P-channel Power MOSFETs the actual polarity of the voltages and the current must be reversed.

## 2 Electrical characteristics

$T_C = 25\text{ °C}$  unless otherwise specified

**Table 3. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$ , $I_D = 250\text{ }\mu\text{A}$	30			V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$ , $V_{DS} = 30\text{ V}$			1	$\mu\text{A}$
		$V_{GS} = 0\text{ V}$ , $V_{DS} = 30\text{ V}$ , $T_C = 125\text{ °C}$			10	$\mu\text{A}$
$I_{GSS}$	Gate-body leakage current	$V_{DS} = 0\text{ V}$ , $V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	1			V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$ , $I_D = 4.5\text{ A}$		24	30	m $\Omega$
		$V_{GS} = 4.5\text{ V}$ , $I_D = 4.5\text{ A}$		32	40	m $\Omega$

**Table 4. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{GS} = 0\text{ V}$ , $V_{DS} = 25\text{ V}$ , $f = 1\text{ MHz}$	-	1450	-	pF
$C_{oss}$	Output capacitance		-	178	-	pF
$C_{rss}$	Reverse transfer capacitance		-	120	-	pF
$Q_g$	Total gate charge	$V_{DD} = 24\text{ V}$ , $I_D = 9\text{ A}$ , $V_{GS} = 4.5\text{ V}$ (see Figure 13. Gate charge test circuit)	-	12	-	nC
$Q_{gs}$	Gate-source charge		-	4.4	-	nC
$Q_{gd}$	Gate-drain charge		-	5	-	nC

**Table 5. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 24\text{ V}$ , $I_D = 4.5\text{ A}$ , $R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$ (see Figure 12. Switching times test circuit for resistive load)	-	15	-	ns
$t_r$	Rise time		-	15	-	ns
$t_{d(off)}$	Turn-off delay time		-	24	-	ns
$t_f$	Fall time		-	21	-	ns

*Note:* For the P-channel Power MOSFETs the actual polarity of the voltages and the current must be reversed.

**Table 6. Source-drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		9	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		36	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0\text{ V}$ , $I_{SD} = 4.5\text{ A}$	-		1.1	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 4.5\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ ,	-	15		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 16\text{ V}$ , $T_J = 150\text{ }^\circ\text{C}$	-	6.5		nC
$I_{RRM}$	Reverse recovery current	(see Figure 14. Test circuit for inductive load switching and diode recovery times)	-	0.9		A

1. Pulse width is limited by safe operating area.

2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%.

**Note:** For the P-channel Power MOSFETs the actual polarity of the voltages and the current must be reversed.

## 2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

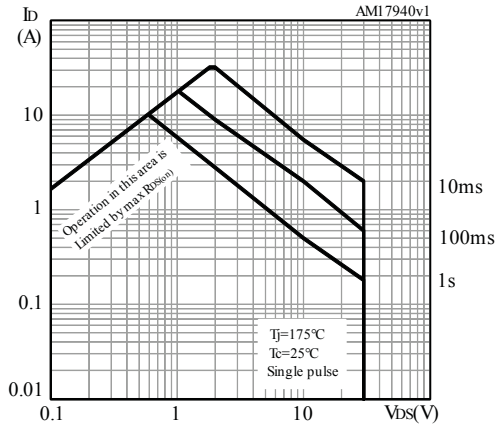


Figure 2. Thermal impedance

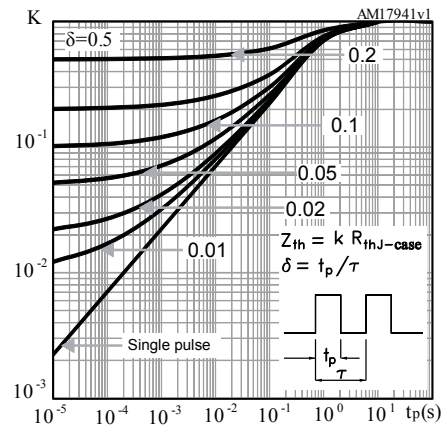


Figure 3. Output characteristics

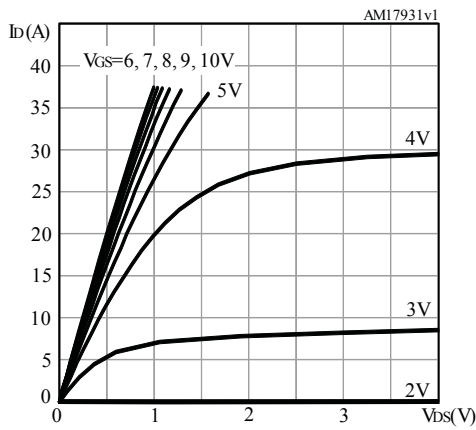


Figure 4. Transfer characteristics

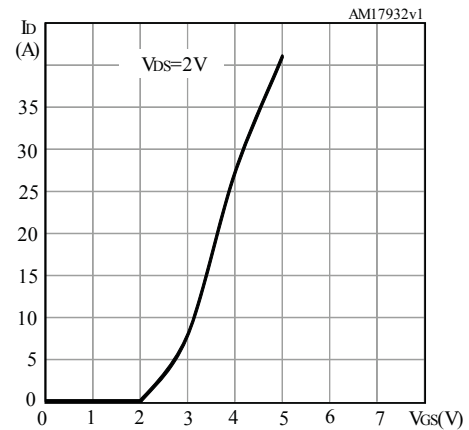


Figure 5. Gate charge vs gate-source voltage

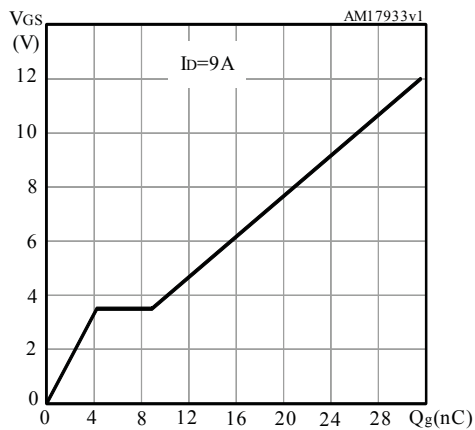
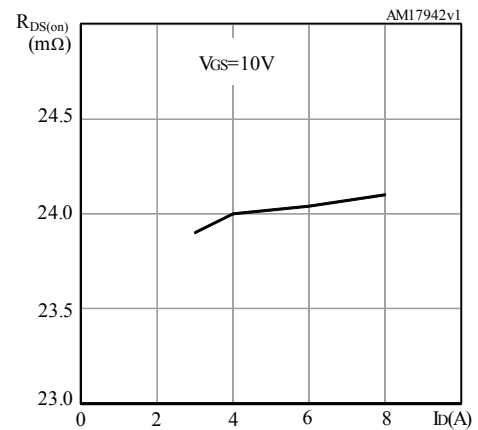
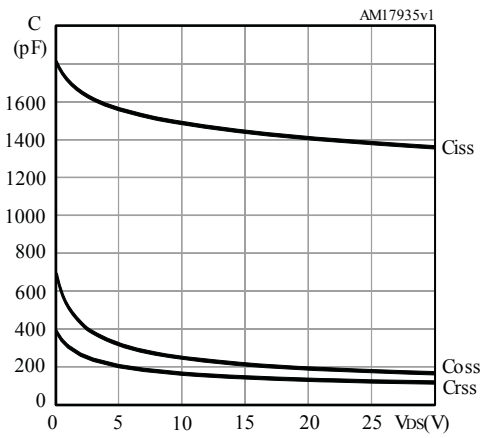


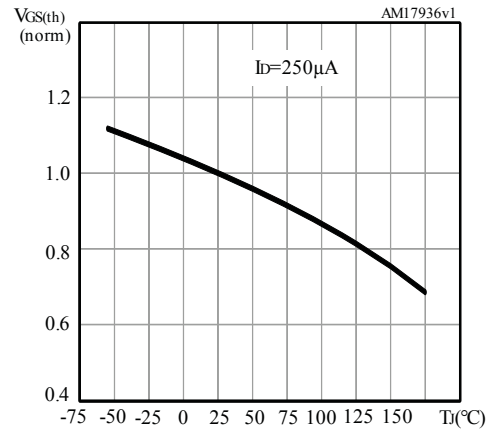
Figure 6. Static drain-source on-resistance



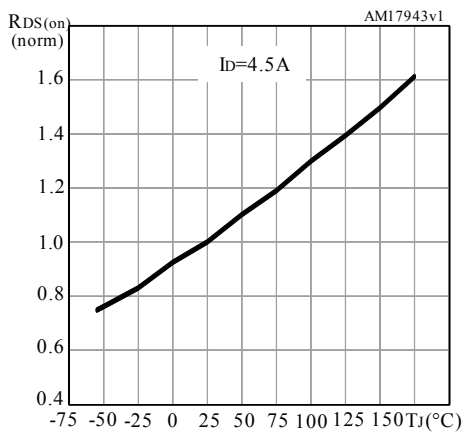
**Figure 7. Capacitance variations**



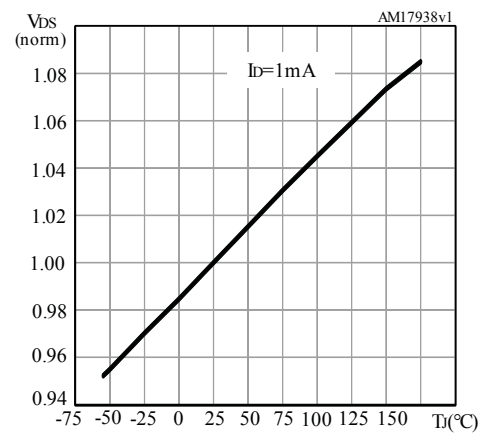
**Figure 8. Normalized gate threshold voltage vs temperature**



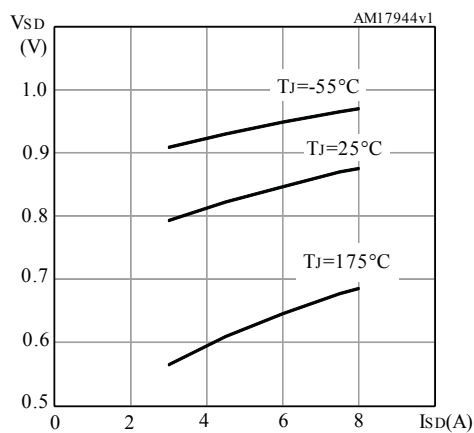
**Figure 9. Normalized on-resistance vs temperature**



**Figure 10. Normalized V<sub>DS</sub> vs temperature**



**Figure 11. Source-drain diode forward characteristics**



### 3 Test circuits

Figure 12. Switching times test circuit for resistive load

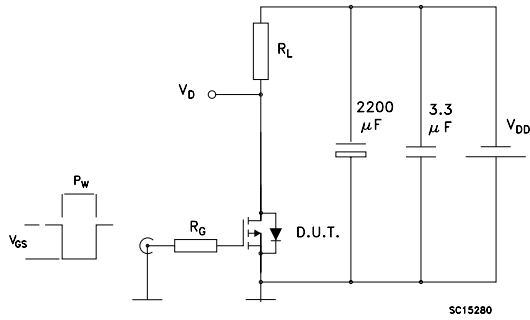


Figure 13. Gate charge test circuit

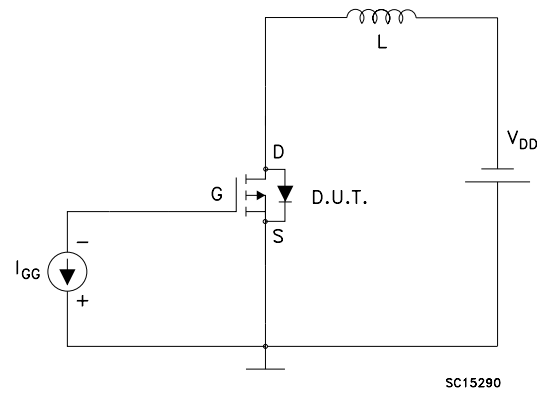
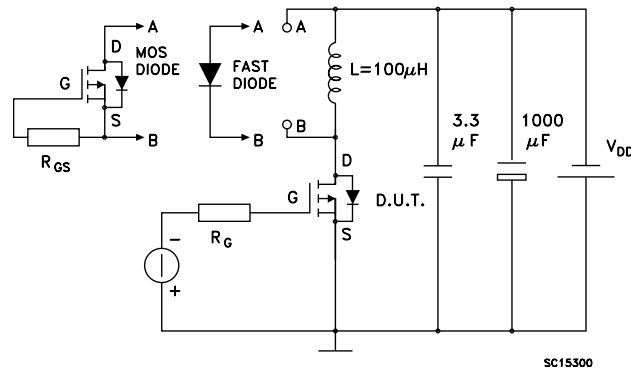


Figure 14. Test circuit for inductive load switching and diode recovery times

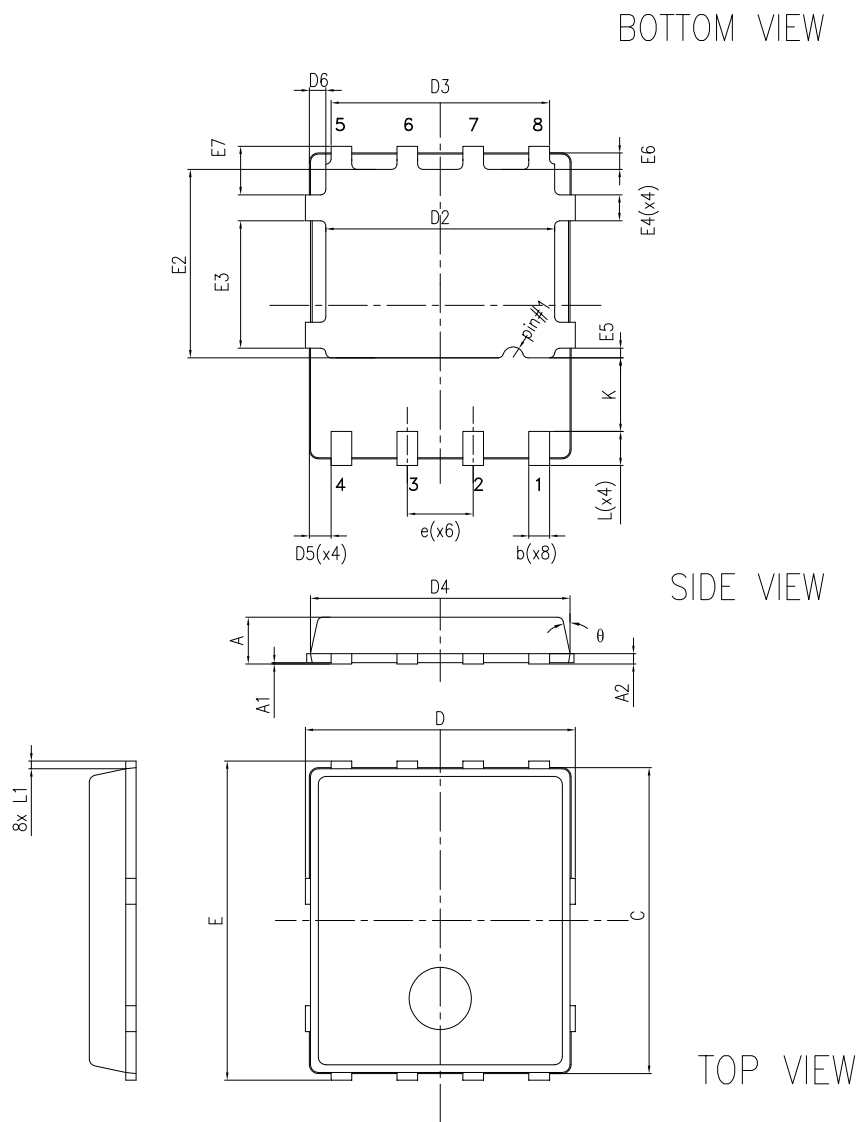


## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 4.1 PowerFLAT 5x6 type R package information

Figure 15. PowerFLAT 5x6 type R package outline



A0ER\_8231817\_Rev20

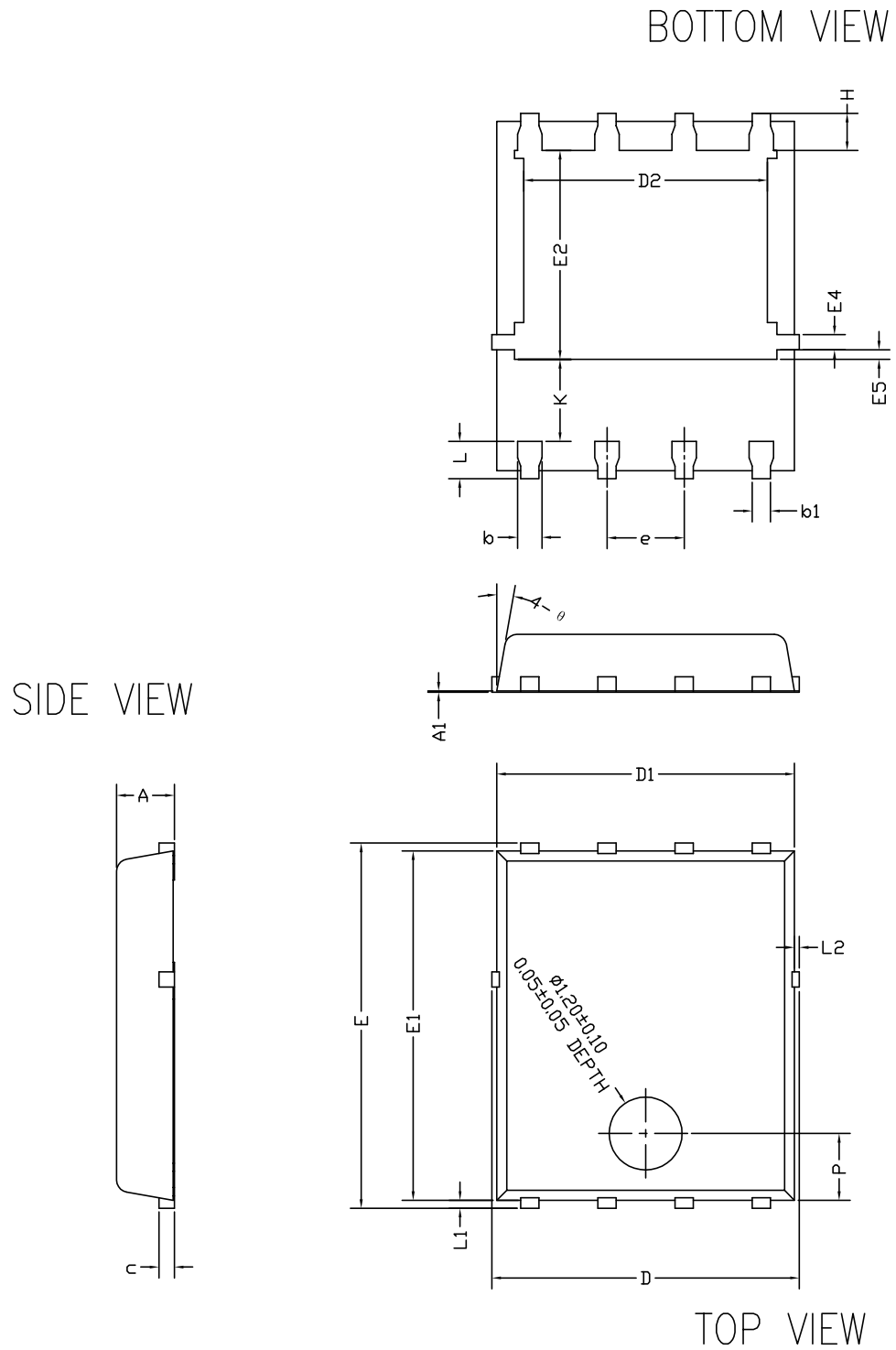


**Table 7. PowerFLAT 5x6 type R mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
C	5.80	6.00	6.20
D	5.00	5.20	5.40
D2	4.15		4.45
D3	4.05	4.20	4.35
D4	4.80	5.00	5.20
D5	0.25	0.40	0.55
D6	0.15	0.30	0.45
e		1.27	
E	5.95	6.15	6.35
E2	3.50		3.70
E3	2.35		2.55
E4	0.40		0.60
E5	0.08		0.28
E6	0.20	0.325	0.45
E7	0.75	0.90	1.05
K	1.275		1.575
L	0.60		0.80
L1	0.05	0.15	0.25
θ	0°		12°

## 4.2 PowerFLAT 5x6 type R SUBCON package information

Figure 16. PowerFLAT 5x6 type R SUBCON package outline

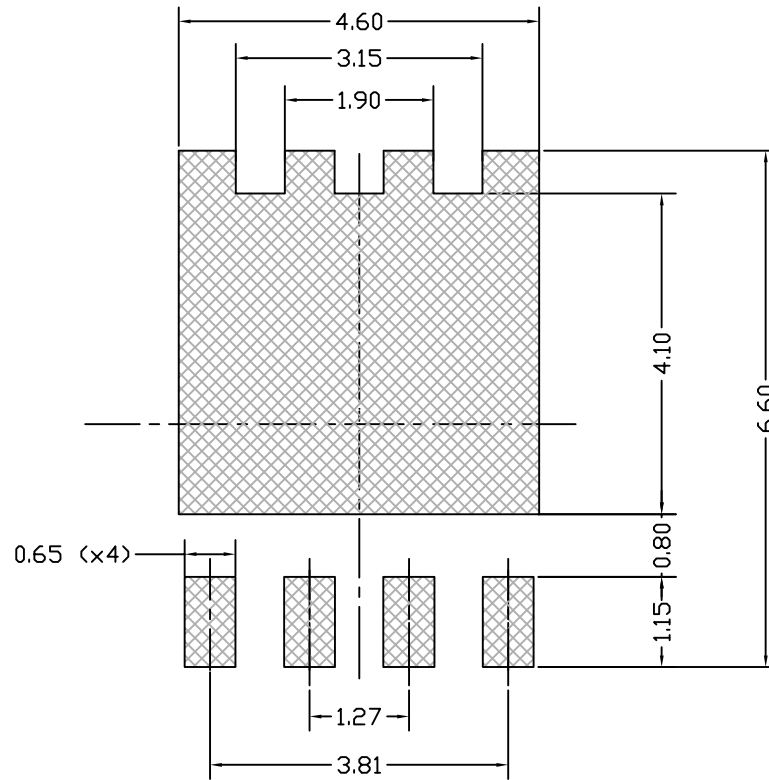


8472137\_SUBCON\_998G\_Type\_R\_REV4

**Table 8. PowerFLAT 5x6 type R SUBCON package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	0.90	0.95	1.00
A1		0.02	
b	0.35	0.40	0.45
b1		0.30	
c	0.21	0.25	0.34
D			5.10
D1	4.80	4.90	5.00
D2	3.91	4.01	4.11
e	1.17	1.27	1.37
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.34	3.44	3.54
E4	0.15	0.25	0.35
E5	0.06	0.16	0.26
H	0.51	0.61	0.71
K	1.10		
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
L2			0.10
P	1.00	1.10	1.20
$\theta$	8°	10°	12°

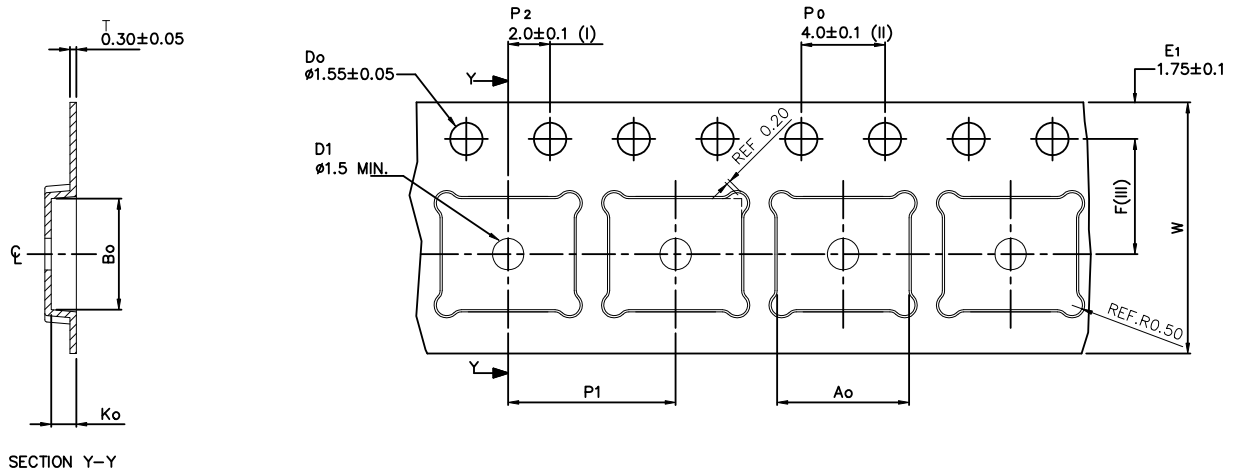
Figure 17. PowerFLAT 5x6 recommended footprint (dimensions are in mm)



8231817\_FOOTPRINT\_simp\_Rev\_20

### 4.3 PowerFLAT 5x6 packing information

Figure 18. PowerFLAT 5x6 tape (dimensions are in mm)



A <sub>0</sub>	6.30	+/- 0.1
B <sub>0</sub>	5.30	+/- 0.1
K <sub>0</sub>	1.20	+/- 0.1
F	5.50	+/- 0.1
P <sub>1</sub>	8.00	+/- 0.1
W	12.00	+/- 0.3

(I) Measured from centreline of sprocket hole to centreline of pocket.

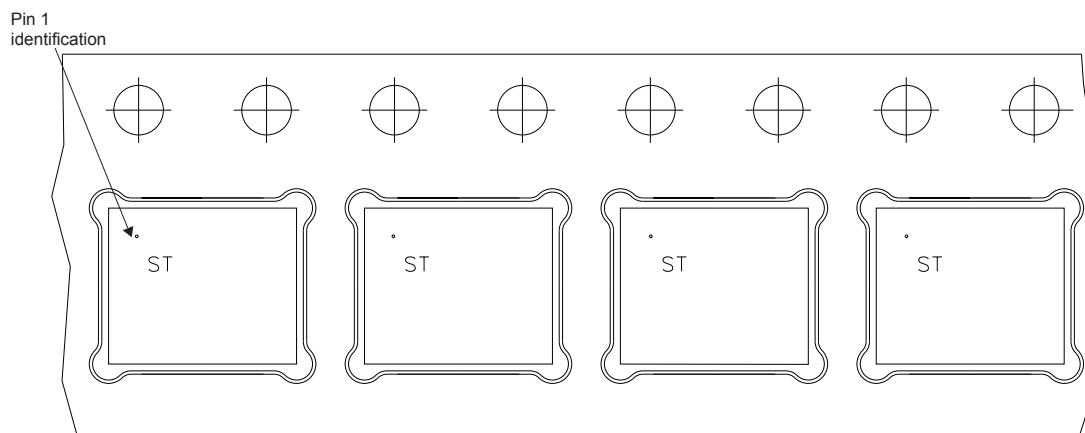
(II) Cumulative tolerance of 10 sprocket holes is  $\pm 0.20$ .

(III) Measured from centreline of sprocket hole to centreline of pocket

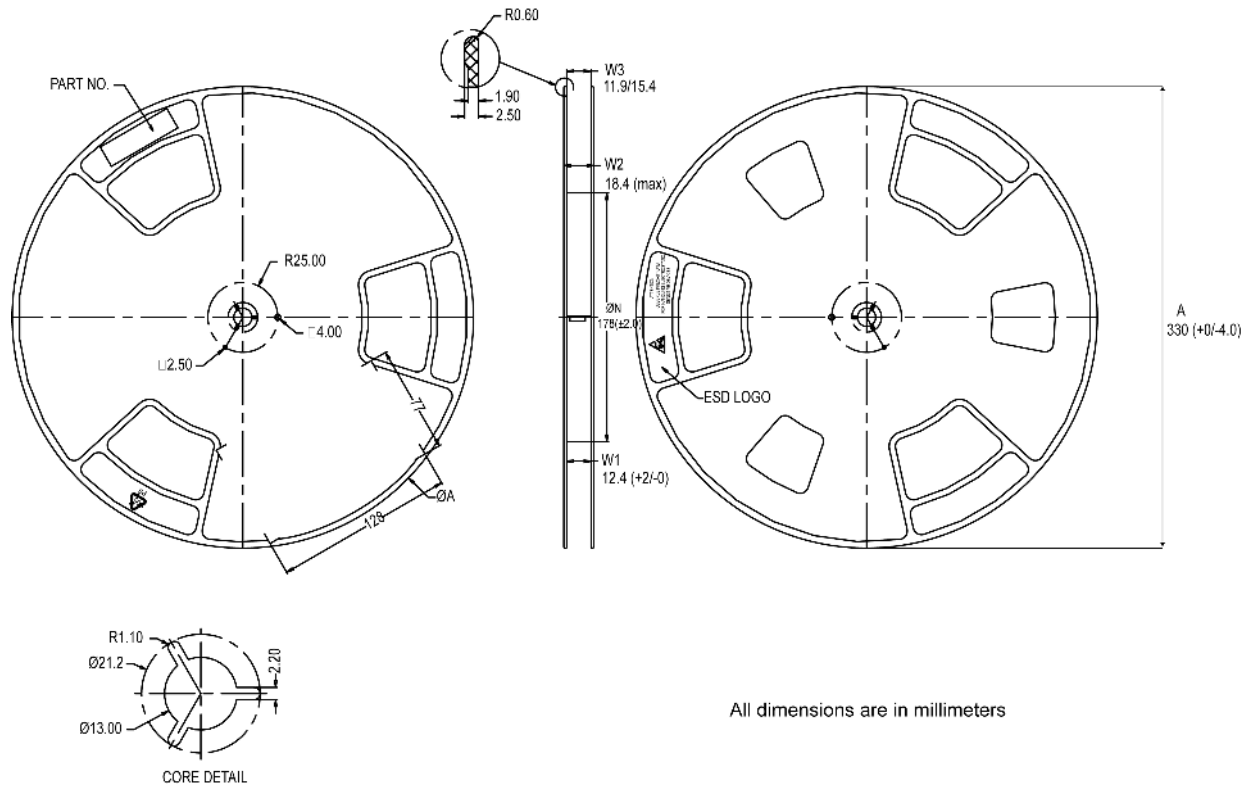
Base and bulk quantity 3000 pcs  
All dimensions are in millimeters

8234350\_Tape\_rev\_C

Figure 19. PowerFLAT 5x6 package orientation in carrier tape



**Figure 20. PowerFLAT 5x6 reel**



8234350\_Reel\_rev\_C

## Revision history

**Table 9. Document revision history**

Date	Revision	Changes
20-Mar-2013	1	First release
28-Nov-2013	2	<ul style="list-style-type: none"> <li>– Modified: title</li> <li>– Modified: <math>I_D</math>, <math>P_{TOT}</math> values and <i>Figure 1</i> in cover page</li> <li>– Modified: <math>V_{GS}</math>, <math>I_D</math> (at <math>T_{pcb} = 125\text{ °C}</math> and <math>T_{pcb} = 100\text{ °C}</math>), <math>I_{DM}</math>, <math>P_{TOT}</math> (at <math>T_C = 25\text{ °C}</math> and <math>T_{pcb} = 25\text{ °C}</math>) and <math>T_{stg}</math> in <i>Table 2</i></li> <li>– Modified: <math>R_{thj-pcb}</math> value in <i>Table 3</i></li> <li>– Modified: <math>I_{GSS}</math> (<math>V_{GS}</math> - test condition) value and <math>I_D</math> (for <math>R_{DS(on)}</math>) in <i>Table 4</i></li> <li>– Modified: <math>Q_g</math> value in <i>Table 5</i></li> <li>– Modified: <math>I_D</math> value in <i>Table 6</i></li> <li>– Modified: <math>I_{SD}</math> and <math>I_{SDM}</math> in <i>Table 7</i></li> <li>– Added: <i>Section 2.1: Electrical characteristics (curves)</i></li> <li>– Minor text changes</li> </ul>
08-Jan-2014	3	<ul style="list-style-type: none"> <li>– Modified: <math>T_J</math> value in <i>Table 2</i></li> <li>– Modified: <i>Figure 6</i></li> <li>– Updated: <i>Section 4: Package mechanical data</i></li> <li>– Minor text changes</li> </ul>
03-Feb-2020	4	<p>Updated <i>Section 4 Package information</i>.</p> <p>Minor text changes.</p>
18-Feb-2020	5	Updated <a href="#">Internal schematic</a> in cover page.

## Contents

<b>1</b>	<b>Electrical ratings</b> .....	<b>2</b>
<b>2</b>	<b>Electrical characteristics</b> .....	<b>3</b>
<b>2.1</b>	Electrical characteristics (curves) .....	<b>5</b>
<b>3</b>	<b>Test circuits</b> .....	<b>7</b>
<b>4</b>	<b>Package information</b> .....	<b>8</b>
<b>4.1</b>	PowerFLAT 5x6 type R package information .....	<b>8</b>
<b>4.2</b>	PowerFLAT 5x6 type R SUBCON package information .....	<b>9</b>
<b>4.3</b>	PowerFLAT 5x6 packing information .....	<b>12</b>
	<b>Revision history</b> .....	<b>15</b>



**IMPORTANT NOTICE – PLEASE READ CAREFULLY**

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, please refer to [www.st.com/trademarks](http://www.st.com/trademarks). All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2020 STMicroelectronics – All rights reserved