

N-channel 75 V, 4.5 mΩ typ., 18 A STripFET™ F6 Power MOSFET in PowerFLAT™ 5x6 package

Datasheet - production data

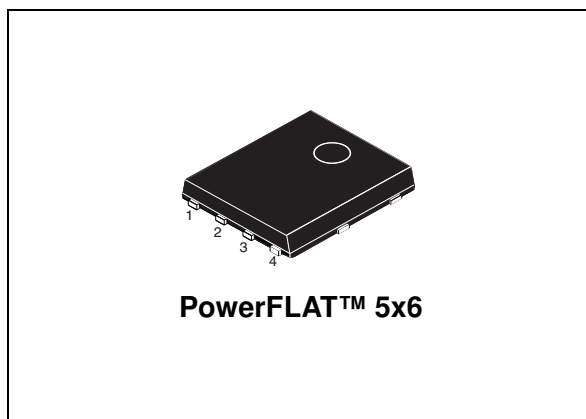
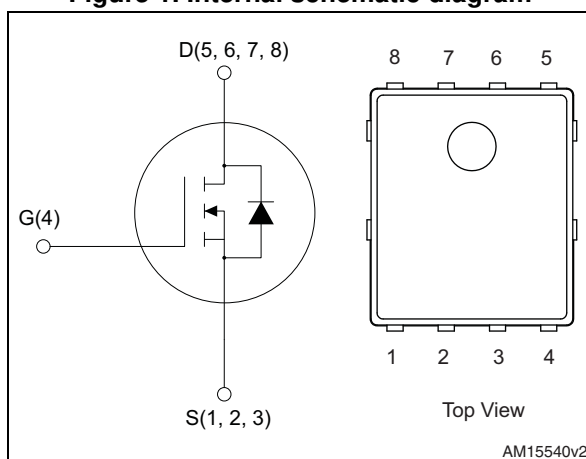


Figure 1. Internal schematic diagram



Features

| Order code | V _{DS} | R _{DS(on)} max | I _D |
|------------|-----------------|-------------------------|----------------|
| STL80N75F6 | 75 V | 5.5 mΩ | 18 A |

- Very low on-resistance
- Very low gate charge
- High avalanche ruggedness
- Low gate drive power loss

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using the STripFET™ F6 technology with a new trench gate structure. The resulting Power MOSFET exhibits very low R_{DS(on)} in all packages.

Table 1. Device summary

| Order code | Marking | Package | Packaging |
|------------|---------|----------------|---------------|
| STL80N75F6 | 80N75F6 | PowerFLAT™ 5x6 | Tape and reel |

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1 Electrical ratings

Table 2. Absolute maximum ratings

| Symbol | Parameter | Value | Unit |
|--------------------|--|-------------|------------------|
| V_{DS} | Drain-source voltage | 75 | V |
| V_{GS} | Gate-source voltage | ± 20 | V |
| $I_D^{(1)}$ | Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$ | 80 | A |
| $I_D^{(2)}$ | Drain current (continuous) at $T_{pcb} = 25\text{ }^\circ\text{C}$ | 18 | A |
| $I_D^{(2)}$ | Drain current (continuous) at $T_{pcb}=100\text{ }^\circ\text{C}$ | 11 | A |
| $I_{DM}^{(2),(3)}$ | Drain current (pulsed) | 72 | A |
| $P_{TOT}^{(1)}$ | Total dissipation at $T_C = 25\text{ }^\circ\text{C}$ | 80 | W |
| $P_{TOT}^{(2)}$ | Total dissipation at $T_{pcb} = 25\text{ }^\circ\text{C}$ | 4 | W |
| T_{stg} | Storage temperature | - 55 to 175 | $^\circ\text{C}$ |
| T_j | Operating junction temperature | | |

1. The value is rated according to R_{thj-c}
2. The value is rated according to $R_{thj-pcb}$
3. Pulse width limited by safe operating area

Table 3. Thermal data

| Symbol | Parameter | Value | Unit |
|---------------------|---------------------------------------|-------|---------------------------|
| $R_{thj-pcb}^{(1)}$ | Thermal resistance junction-pcb max | 31.3 | $^\circ\text{C}/\text{W}$ |
| $R_{thj-case}$ | Thermal resistance junction-case max. | 1.56 | $^\circ\text{C}/\text{W}$ |

1. When mounted on FR-4 board of 1 inch², 2 oz Cu, $t < 10$ sec

Table 4. Avalanche characteristics

| Symbol | Parameter | Max value | Unit |
|----------|--|-----------|------|
| I_{AS} | Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max) | 18 | A |
| E_{AS} | Single pulse avalanche energy (starting $T_j = 25\text{ }^\circ\text{C}$, $I_D = I_{AS}$, $V_{DD} = 50\text{ V}$) | 730 | mJ |

2 Electrical characteristics

($T_J = 25\text{ °C}$ unless otherwise specified)

Table 5. On/off states

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---------------|--|--|------|------|-----------|--------------------------------|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage | $I_D = 1\text{ mA}$, $V_{GS} = 0$ | 75 | | | V |
| I_{DSS} | Zero gate voltage drain current ($V_{GS} = 0$) | $V_{DS} = 75\text{ V}$, $V_{DS} = 75\text{ V}$, $T_C = 125\text{ °C}$ | | | 1 10 | μA μA |
| I_{GSS} | Gate body leakage current ($V_{DS} = 0$) | $V_{GS} = \pm 20\text{ V}$ | | | ± 100 | nA |
| $V_{GS(th)}$ | Gate threshold voltage | $V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$ | 2 | | 4 | V |
| $R_{DS(on)}$ | Static drain-source on-resistance | $V_{GS} = 10\text{ V}$, $I_D = 9\text{ A}$ | | 4.5 | 5.5 | m Ω |

Table 6. Dynamic

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-----------|------------------------------|--|------|------|------|----------|
| C_{iss} | Input capacitance | $V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0$ | - | 6100 | - | pF |
| C_{oss} | Output capacitance | | - | 530 | - | pF |
| C_{rss} | Reverse transfer capacitance | | - | 185 | - | pF |
| Q_g | Total gate charge | $V_{DD} = 37.5\text{ V}$, $I_D = 18\text{ A}$ $V_{GS} = 10\text{ V}$ (see Figure 14) | - | 78 | - | nC |
| Q_{gs} | Gate-source charge | | - | 24 | - | nC |
| Q_{gd} | Gate-drain charge | | - | 15 | - | nC |
| R_g | Gate input resistance | $f = 1\text{ MHz}$ Gate DC Bias = 0 test signal level = 20 mV open drain | - | 1.47 | - | Ω |

Table 7. Switching times

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|--------------|---------------------|---|------|------|------|------|
| $t_{d(on)}$ | Turn-on delay time | $V_{DD} = 37.5\text{ V}$, $I_D = 9\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$ (see Figure 13) | - | 28 | - | ns |
| t_r | Rise time | | - | 17 | - | ns |
| $t_{d(off)}$ | Turn-off delay time | | - | 66 | - | ns |
| t_f | Fall time | | - | 12 | - | ns |

Table 8. Source drain diode

| Symbol | Parameter | Test conditions | Min. | Typ. | Max | Unit |
|-----------------|-------------------------------|---|------|------|-----|------|
| I_{SD} | Source-drain current | | - | | 18 | A |
| $I_{SDM}^{(1)}$ | Source-drain current (pulsed) | | - | | 72 | A |
| $V_{SD}^{(2)}$ | Forward on voltage | $I_{SD} = 18 \text{ A}, V_{GS} = 0$ | - | | 1.5 | V |
| t_{rr} | Reverse recovery time | $I_{SD} = 18 \text{ A},$ $di/dt = 100 \text{ A}/\mu\text{s},$ $V_{DD} = 60 \text{ V}, T_J = 150 \text{ }^\circ\text{C}$ (see Figure 15) | - | 48 | | ns |
| Q_{rr} | Reverse recovery charge | | - | 96 | | nC |
| I_{RRM} | Reverse recovery current | | - | 4 | | A |

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

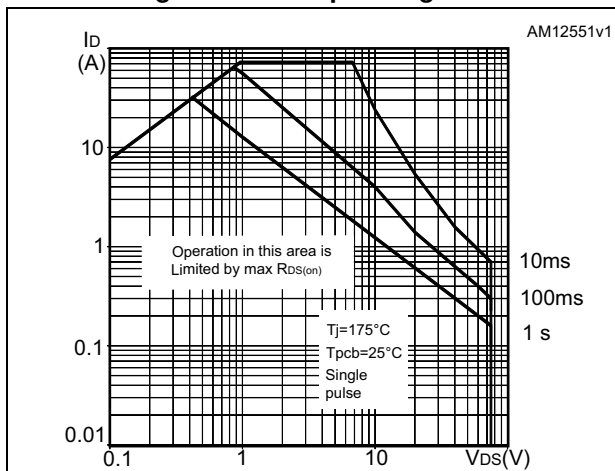


Figure 3. Thermal impedance

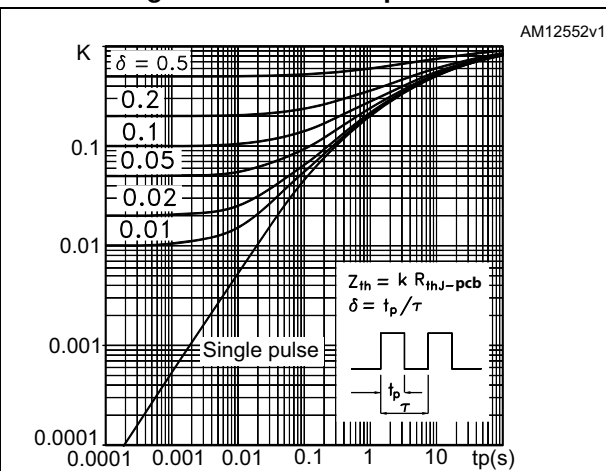


Figure 4. Output characteristics

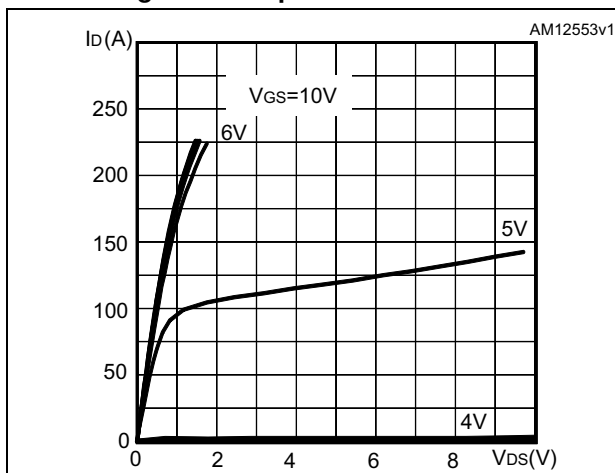


Figure 5. Transfer characteristics

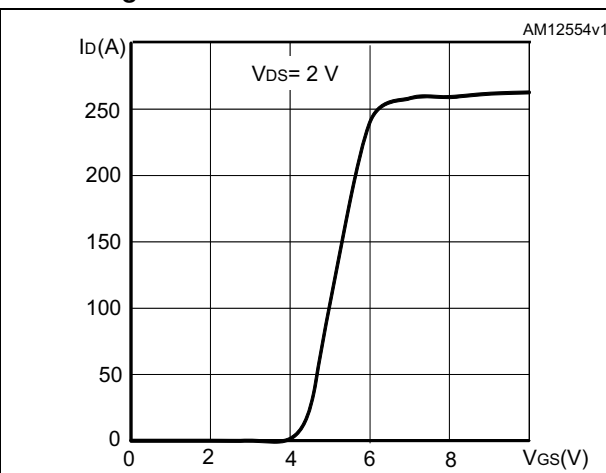


Figure 6. Gate charge vs gate-source voltage

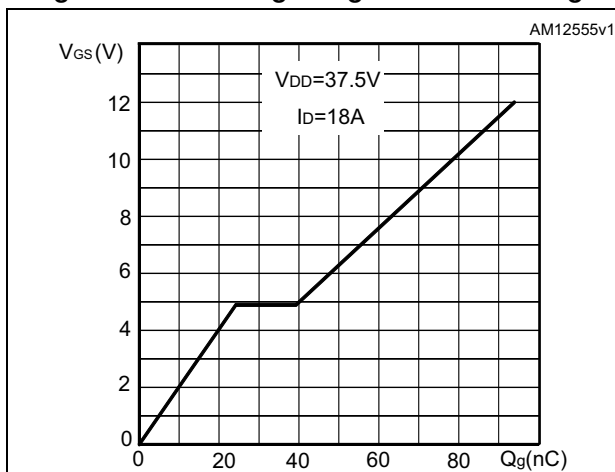


Figure 7. Static drain-source on-resistance

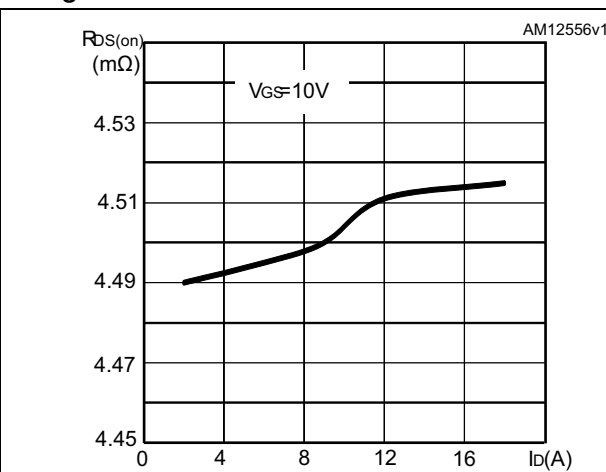


Figure 8. Capacitance variations

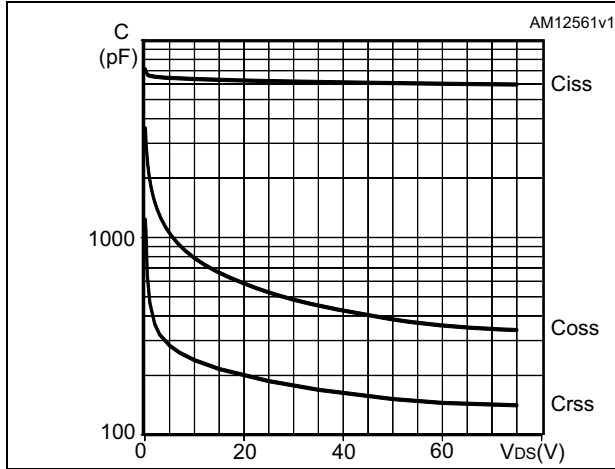


Figure 9. Normalized gate threshold voltage vs temperature

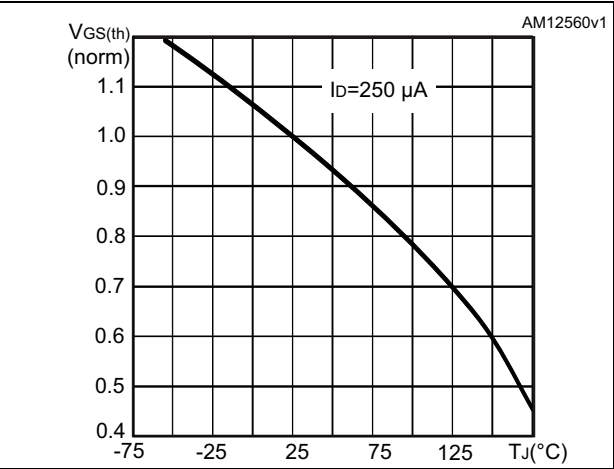


Figure 10. Normalized on-resistance vs temperature

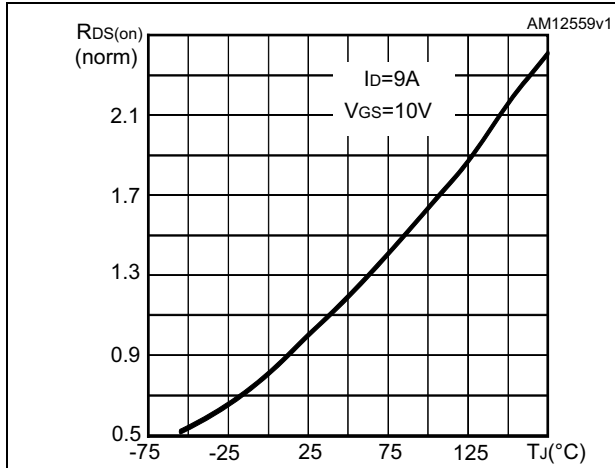


Figure 11. Source-drain diode forward characteristics

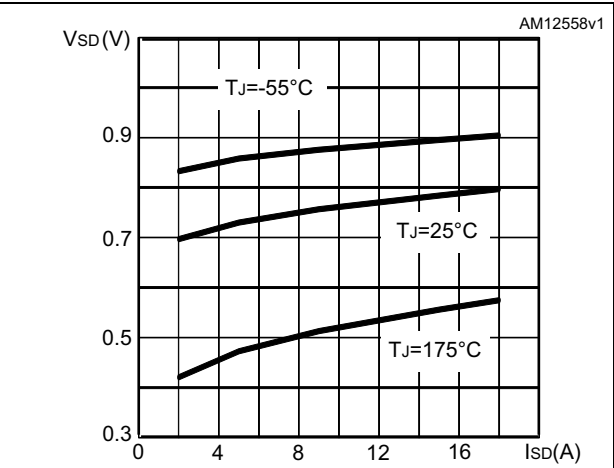
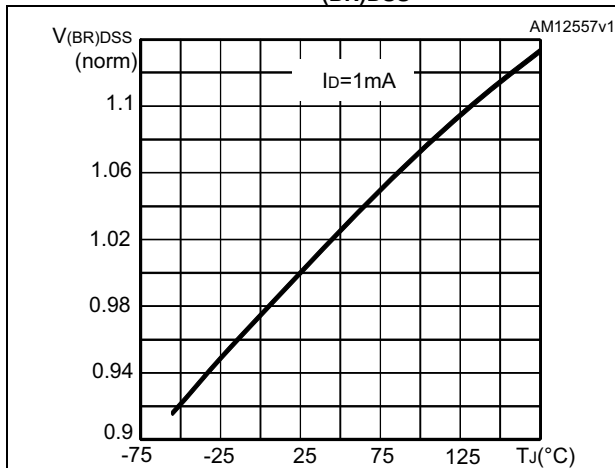


Figure 12. Normalized V_{(BR)DSS} vs temperature



3 Test circuits

Figure 13. Switching times test circuit for resistive load

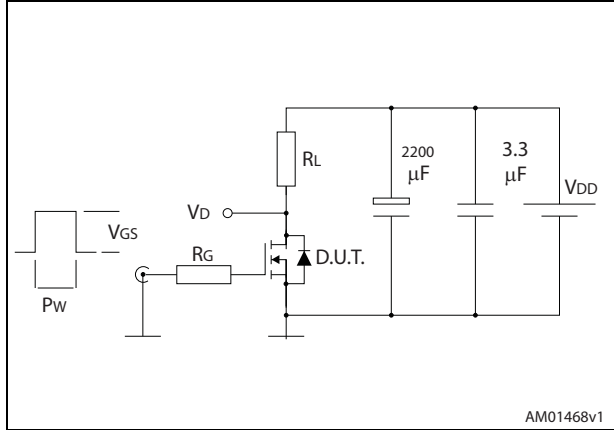


Figure 14. Gate charge test circuit

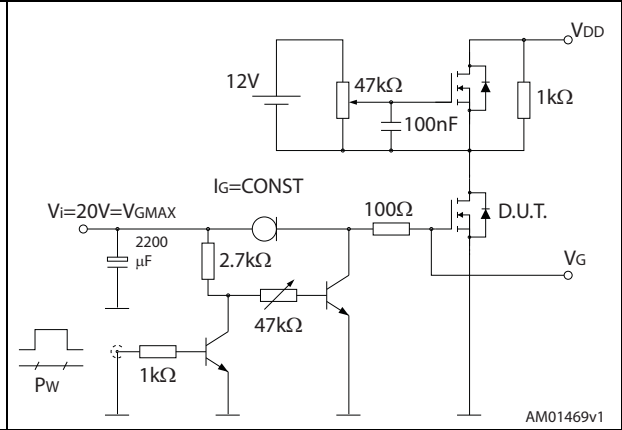


Figure 15. Test circuit for inductive load switching and diode recovery times

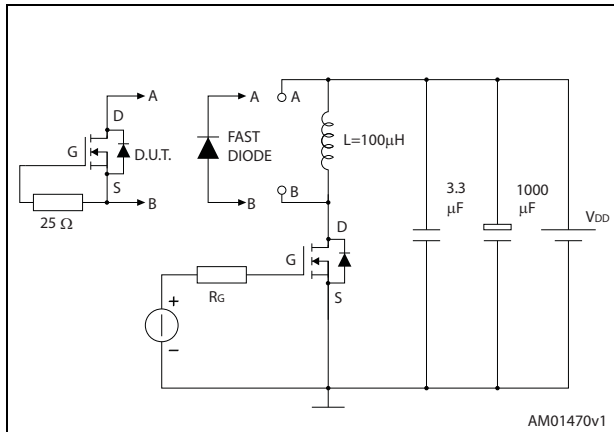


Figure 16. Unclamped inductive load test circuit

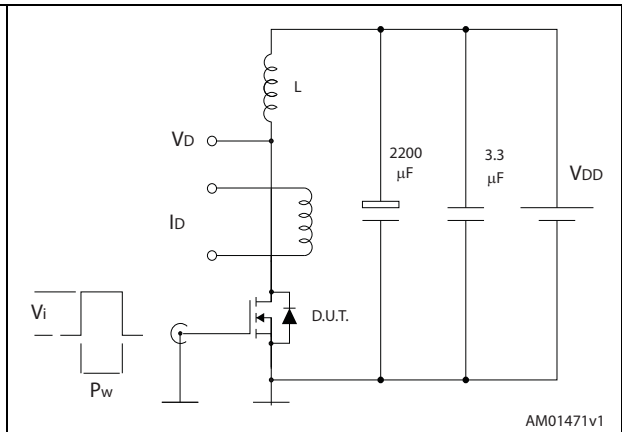


Figure 17. Unclamped inductive waveform

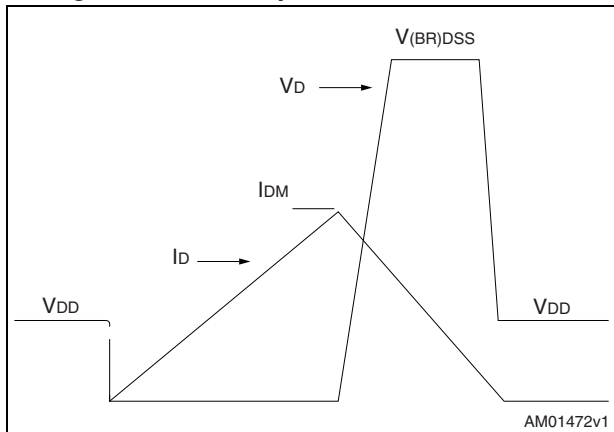
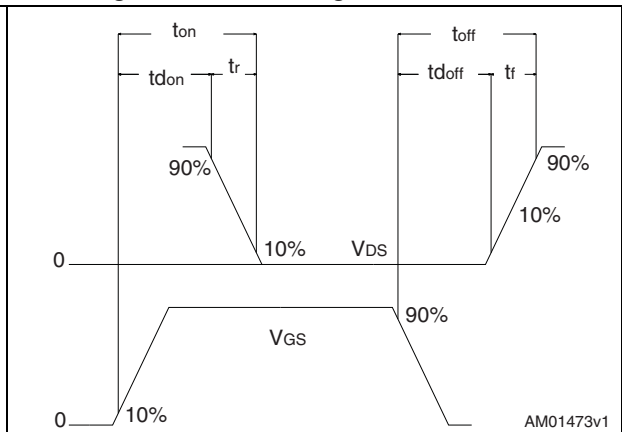


Figure 18. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

Figure 19. PowerFLAT™ 5x6 type S-C mechanical data

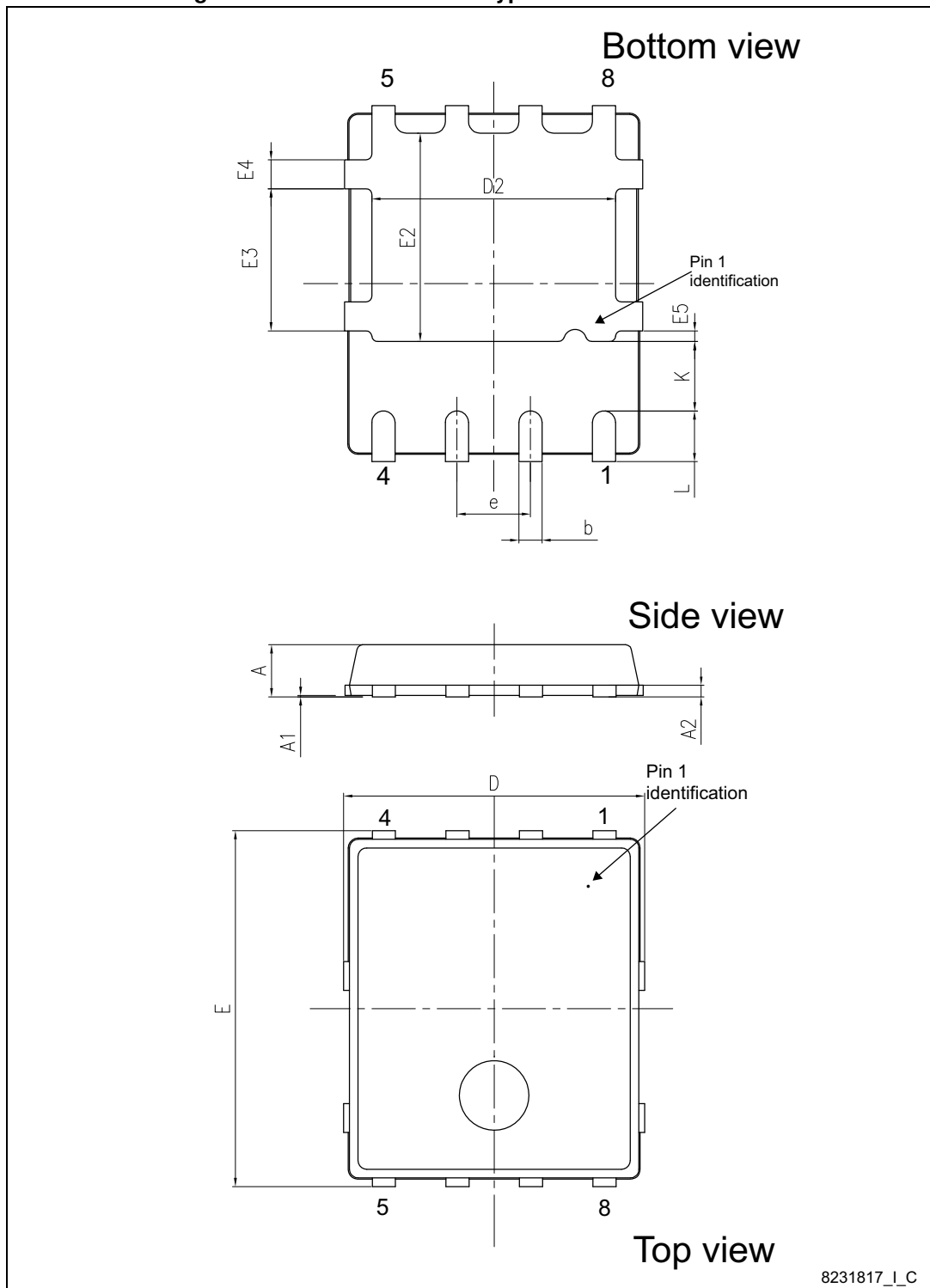
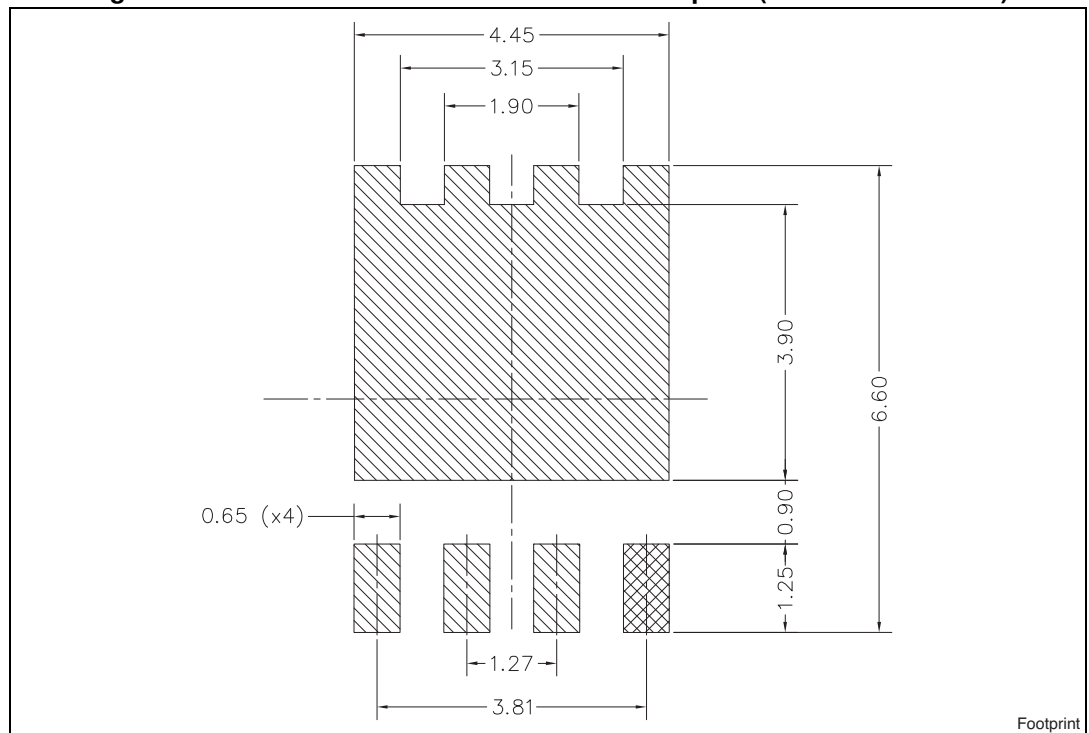


Table 9. PowerFLAT™ 5x6 type S-C mechanical data

| Dim. | mm | | |
|------|-------|------|-------|
| | Min. | Typ. | Max. |
| A | 0.80 | | 1.00 |
| A1 | 0.02 | | 0.05 |
| A2 | | 0.25 | |
| b | 0.30 | | 0.50 |
| D | | 5.20 | |
| D2 | 4.11 | | 4.31 |
| E | | 6.15 | |
| e | | 1.27 | |
| e1 | | 0.65 | |
| E2 | 3.50 | | 3.70 |
| E3 | 2.35 | | 2.55 |
| E4 | 0.40 | | 0.60 |
| E5 | 0.08 | | 0.28 |
| K | 1.05 | | 1.35 |
| L | 0.715 | | 1.015 |

Figure 20. PowerFLAT™ 5x6 recommended footprint (dimensions in mm)



5 Packaging mechanical data

Figure 21. PowerFLAT™ 5x6 tape^(a)

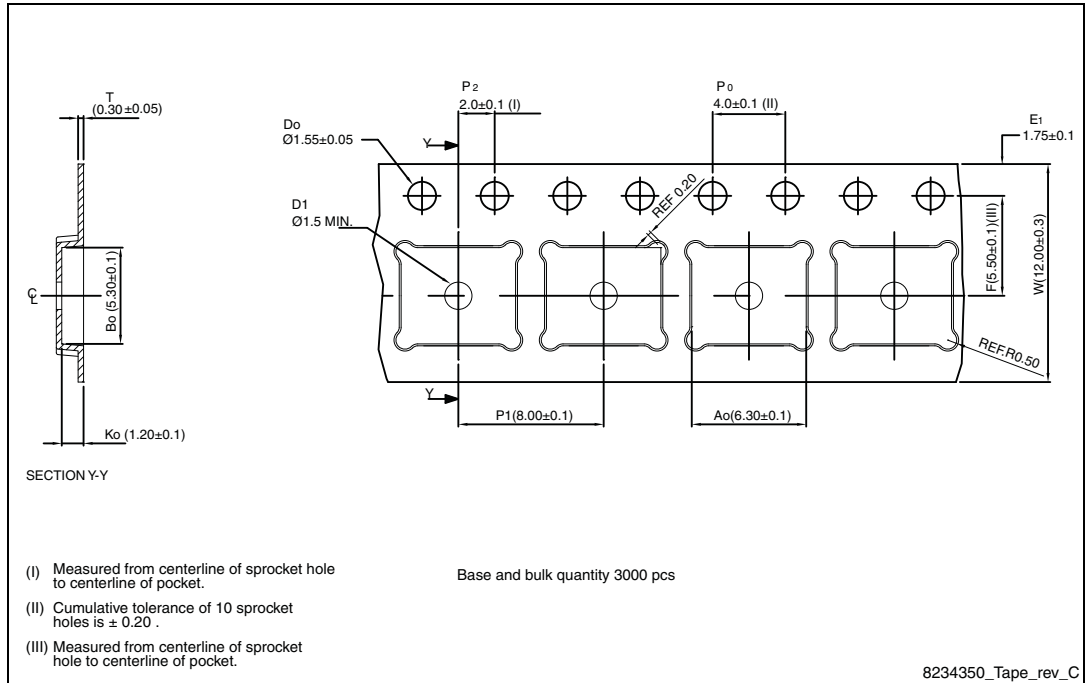
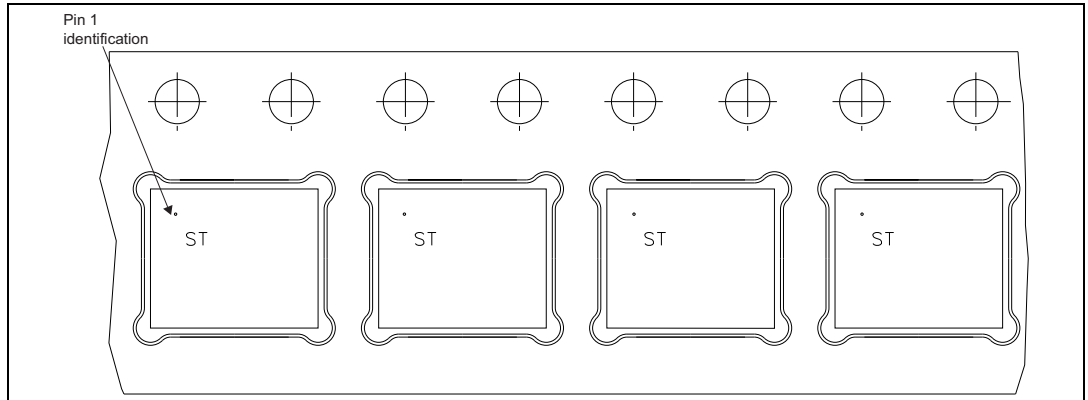
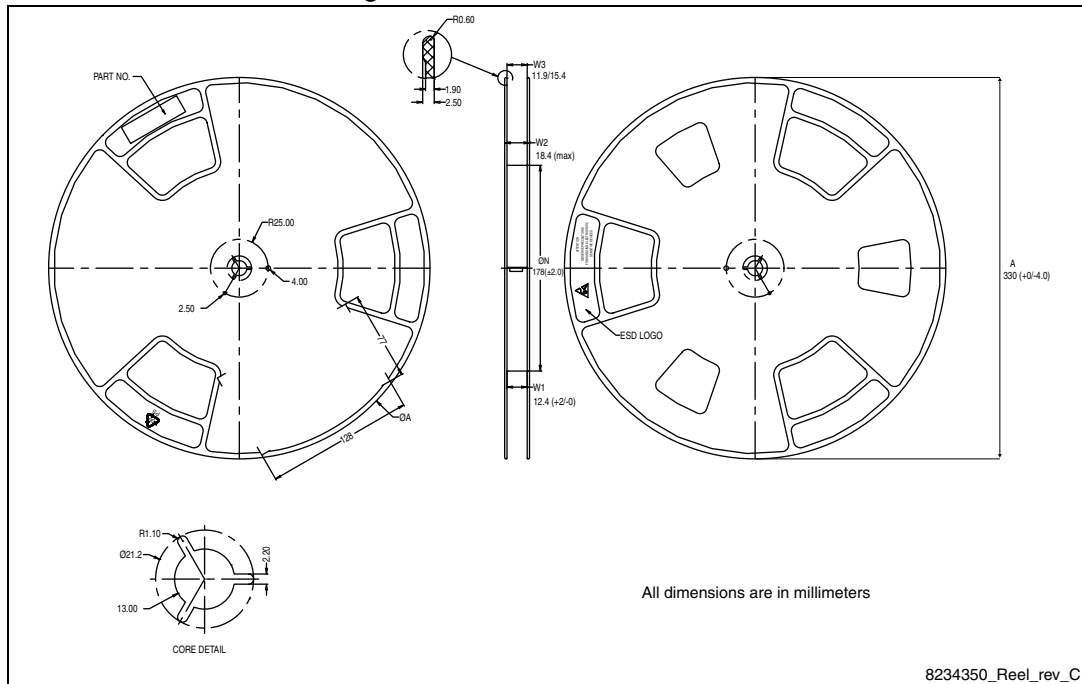


Figure 22. PowerFLAT™ 5x6 package orientation in carrier tape.



a. All dimensions are in millimeters.

Figure 23. PowerFLAT™ 5x6 reel



6 Revision history

Table 10. Document revision history

| Date | Revision | Changes |
|-------------|----------|---|
| 27-Apr-2011 | 1 | First release. |
| 10-Nov-2011 | 2 | Section 4: Package mechanical data has been updated. Minor text changes. |
| 11-Mar-2014 | 3 | <ul style="list-style-type: none"> – Modified: Table 2 (I_{DM} value), Table 4 (I_{AS}, E_{AS} values) Table 5 ($R_{DS(on)}$ typ. and max values), Table 6 (typ. and test conditions), Table 7 (test conditions and typ. values) Table 8 (test conditions, typ. and max values) – Added: Section 2.1: Electrical characteristics (curves). – Updated: Section 4: Package mechanical data – Minor text changes |
| 21-Aug-2014 | 4 | <ul style="list-style-type: none"> – Updated title, features and description in cover page. – Updated unit for $R_{DS(on)}$ in Table 5: On/off states and in Figure 7: Static drain-source on-resistance. – Updated Section 4: Package mechanical data. |

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