STD10NM65N - STF10NM65N
STP10NM65N - STU10NM65N

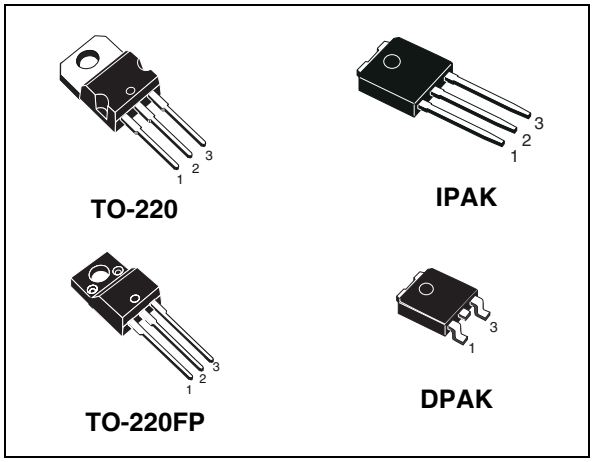
N-channel 650 V, 0.43 Ω, 9 A MDmesh™ II Power MOSFET
TO-220, TO-220FP, IPAK, DPAK

Features

Type	V_{DSS} (@Tjmax)	$R_{DS(on)}$ max	I_D
STD10NM65N	710 V	< 0.48 Ω	9 A
STF10NM65N	710 V	< 0.48 Ω	9 A(1)
STP10NM65N	710 V	< 0.48 Ω	9 A
STU10NM65N	710 V	< 0.48 Ω	9 A

1. Limited only by maximum temperature allowed

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance



Application

- Switching applications

Description

This series of devices implements the second generation of MDmesh™ Technology. This revolutionary Power MOSFET associates a new vertical structure to the Company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters.

Figure 1. Internal schematic diagram

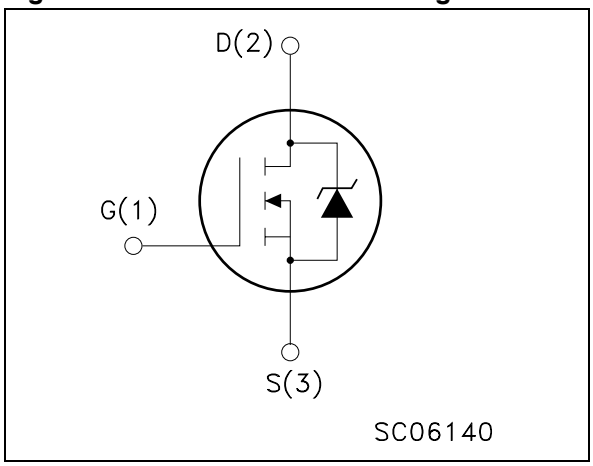


Table 1. Device summary

Order codes	Marking	Package	Packaging
STD10NM65N	10NM65N	DPAK	Tape & reel
STF10NM65N	10NM65N	TO-220FP	Tube
STP10NM65N	10NM65N	TO-220	Tube
STU10NM65N	10NM65N	IPAK	Tube

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		TO-220/IPAK DPAK	TO-220FP	
V_{DS}	Drain-source voltage (V_{GS} = 0)	650		V
V_{GS}	Gate-source voltage	± 25		V
I_D	Drain current (continuous) at T_C = 25 °C	9	9(1)	A
I_D	Drain current (continuous) at T_C = 100 °C	5.7	5.7(1)	A
I_{DM} (2)	Drain current (pulsed)	36	36(1)	A
P_{TOT}	Total dissipation at T_C = 25 °C	90	25	W
dv/dt (3)	Peak diode recovery voltage slope	15		V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t=1 s; T_C = 25 °C)	--	2500	V
T_{stg}	Storage temperature	-55 to 150		°C
T_j	Max. operating junction temperature	150		°C

1. Limited only by maximum temperature allowed
2. Pulse width limited by safe operating area
3. $I_{SD} \leq 9$ A, di/dt $\leq$ 400 A/µs, V_{DD} = 80% $V_{(BR)DSS}$

Table 3. Thermal data

Symbol	Parameter	TO-220	IPAK	DPAK	TO-220FP	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case max	1.38			5	°C/W
$R_{thj\text{-}pcb}$	Thermal resistance junction-pcb max	--	--	50	--	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-amb max	62.5	100	--	62.5	°C/W
T_l	Maximum lead temperature for soldering purpose	300				°C

Table 4. Avalanche characteristics

Symbol	Parameter	Max value	Unit
I_{AS}	Avalanche current, repetitive or not-repetitive (pulse width limited by Tj max)	2.5	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25 °C, $I_D = I_{AS}$, V_{DD}= 50 V)	200	mJ

2 Electrical characteristics

(T_{CASE}=25 °C unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0	650			V
dv/dt (1)	Drain source voltage slope	V_{DD}= 520 V, I_D= 9 A, V_{GS}= 10 V		25		V/ns
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = max rating V_{DS} = max rating, @125 °C			1 100	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 20 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2	3	4	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 4.5 A		0.43	0.48	Ω

1. Characteristics value at turn off on inductive load

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS}=15 V, I_D = 4.5 A		7.5		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 50 V, f = 1 MHz, V_{GS} = 0		850 53 4		pF pF pF
$C_{oss\ eq.}$ (2)	Equivalent output capacitance	V_{GS} = 0, V_{DS} = 0 to 520 V		90		pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 520 V, I_D = 9 A, V_{GS} = 10 V, *(see Figure 19)*		25 14 4		nC nC nC

1. Pulsed: pulse duration = 300 µs, duty cycle 1.5%
2. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7. Switching times

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off delay time Fall time	V_{DD} = 325 V, I_D = 4.5 A R_G = 4.7 Ω V_{GS} = 10 V *(see Figure 18)*		12 8 50 20		ns ns ns ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
I_{SD} I_{SDM} (1)	Source-drain current Source-drain current (pulsed)				9 36	A A
V_{SD} (2)	Forward on voltage	I_{SD} = 9 A, V_{GS} = 0			1.3	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 9 A, di/dt = 100 A/µs V_{DD} = 100 V *(see Figure 20)*		330 3 19		ns µC A
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 9 A, di/dt = 100 A/µs V_{DD} = 100 V, T_j = 150 °C *(see Figure 20)*		430 4 19		ns µC A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for TO-220

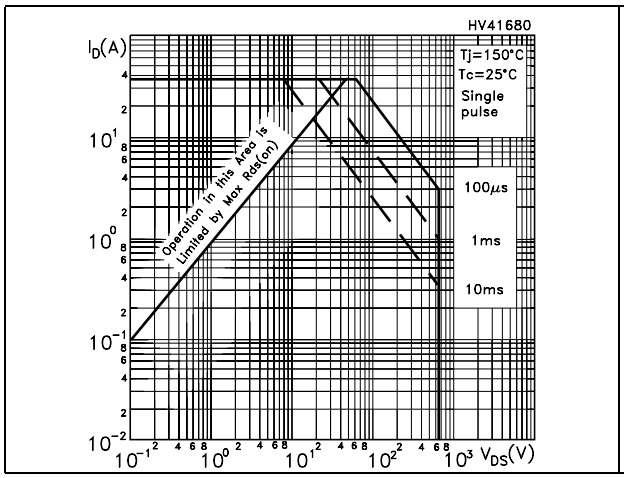


Figure 3. Thermal impedance for TO-220

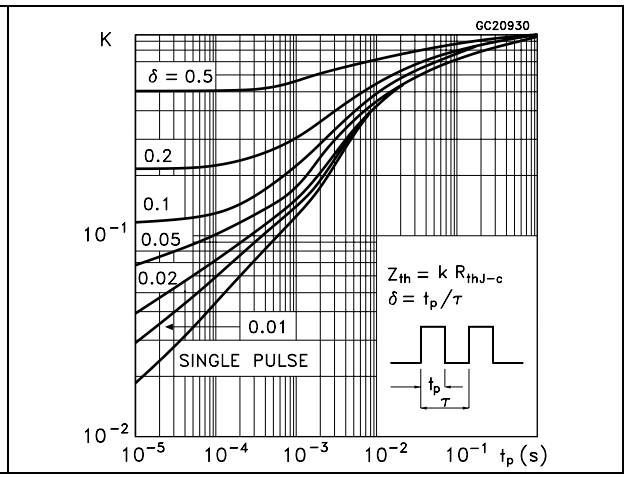


Figure 4. Safe operating area for TO-220FP

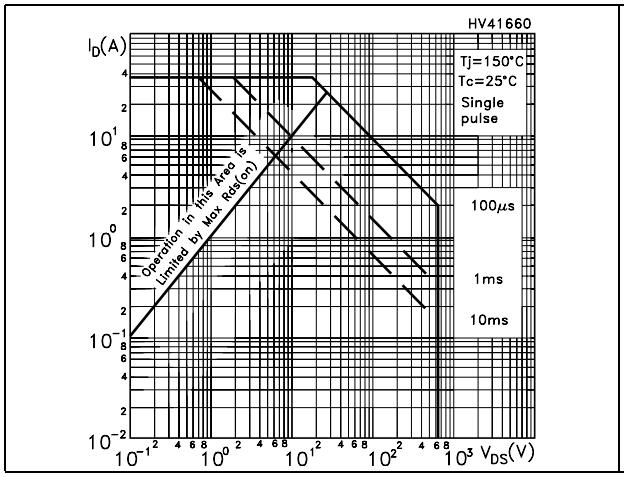


Figure 5. Thermal impedance for TO-220FP

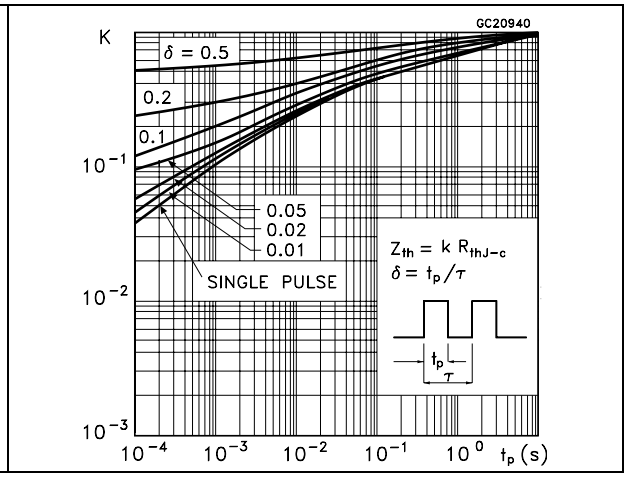


Figure 6. Safe operating area for DPAK/IPAK

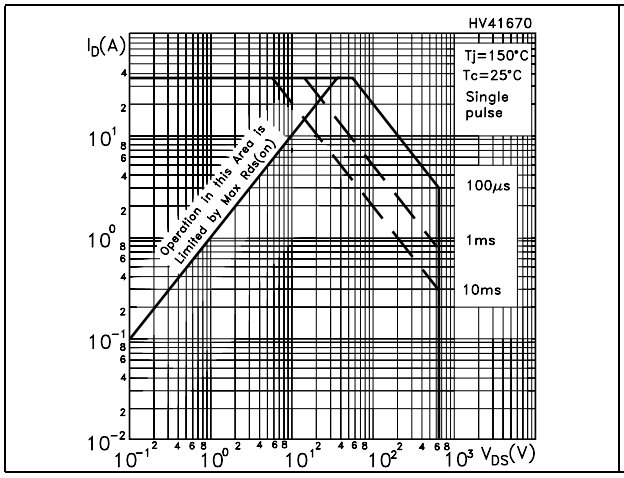


Figure 7. Thermal impedance for DPAK/IPAK

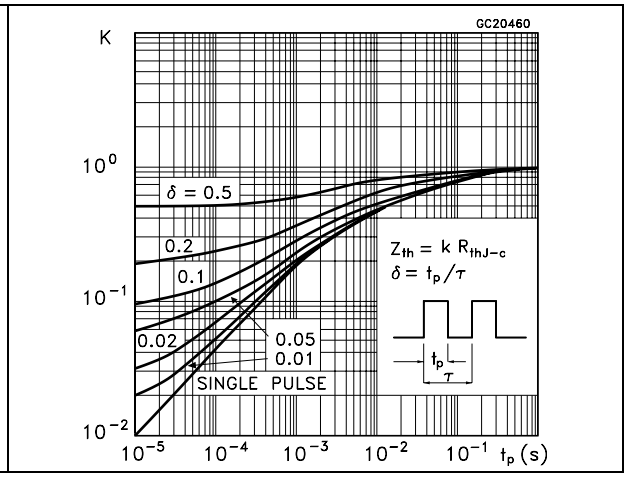


Figure 8. Output characteristics

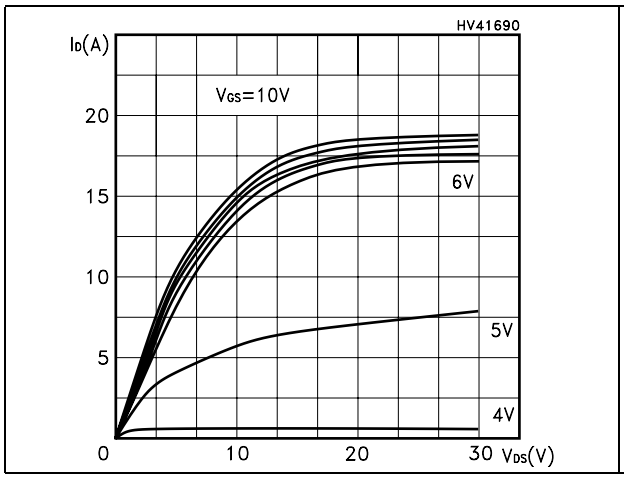


Figure 9. Transfer characteristics

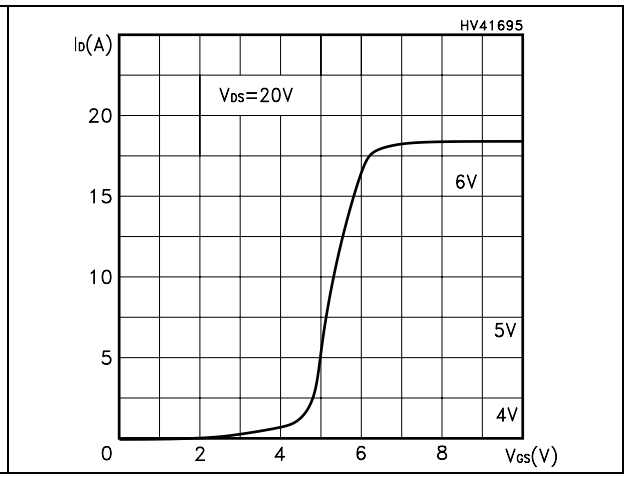


Figure 10. Transconductance

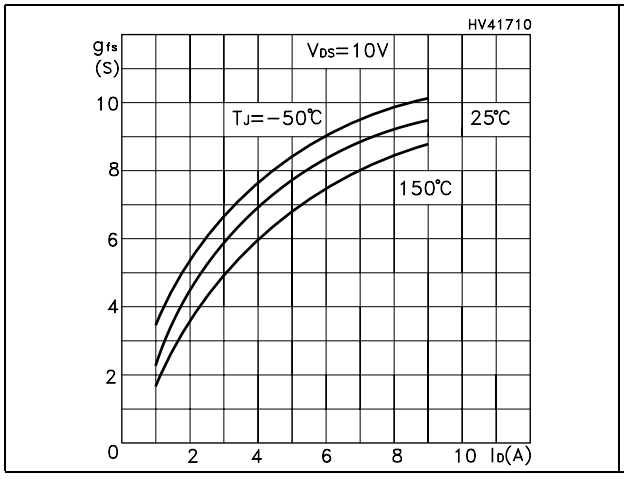


Figure 11. Static drain-source on resistance

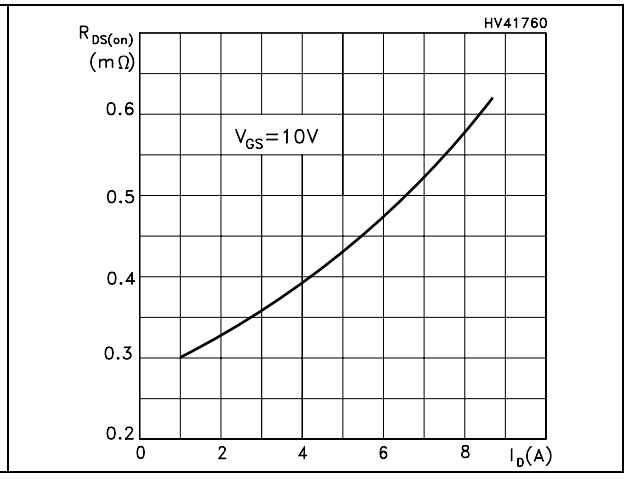


Figure 12. Gate charge vs gate source voltage

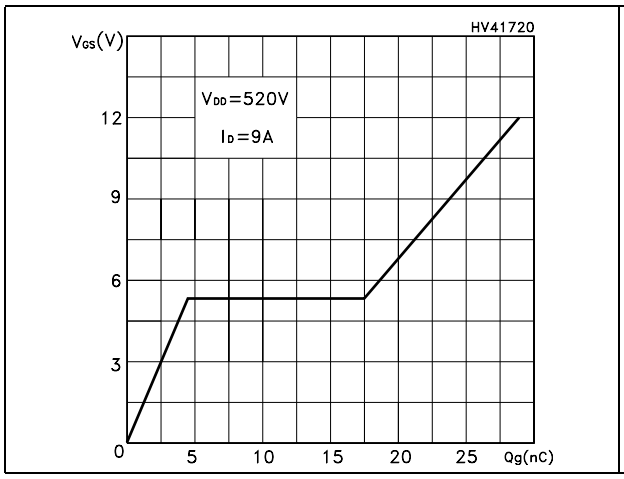


Figure 13. Capacitance variations

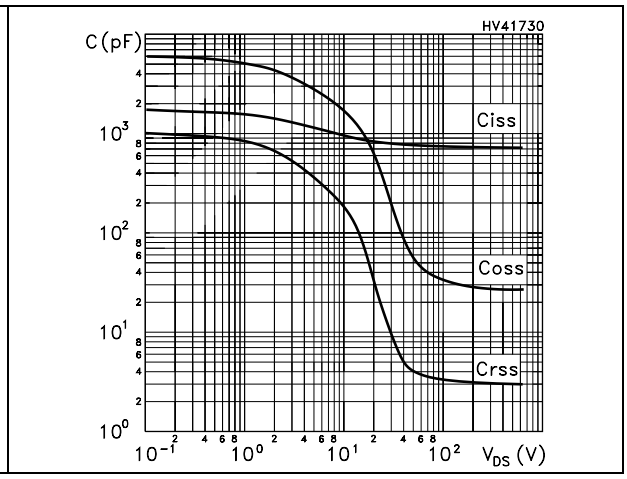


Figure 14. Normalized gate threshold voltage vs temperature

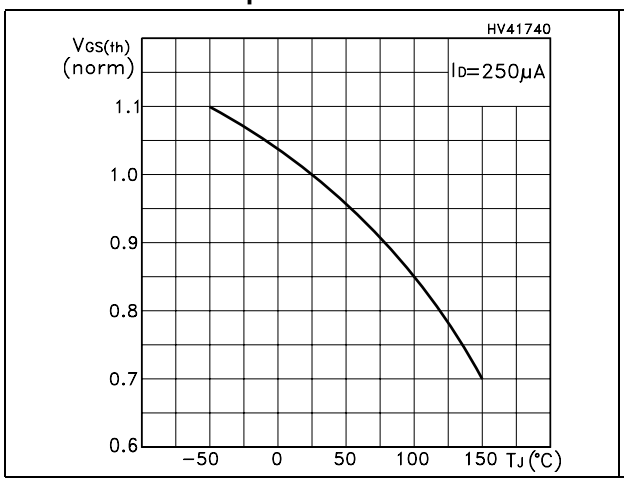


Figure 15. Normalized on resistance vs temperature

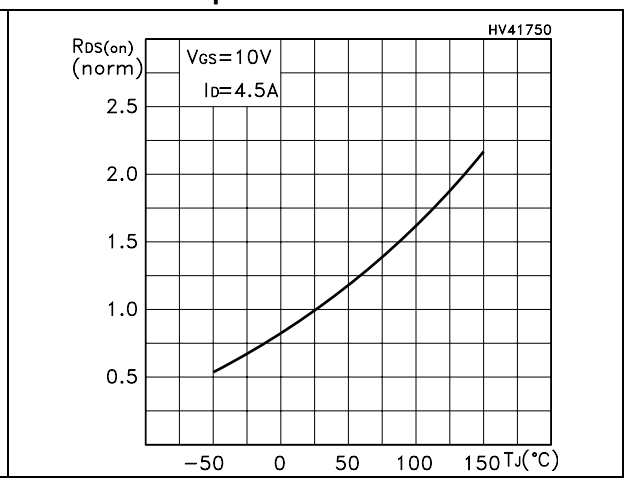


Figure 16. Source-drain diode forward characteristics

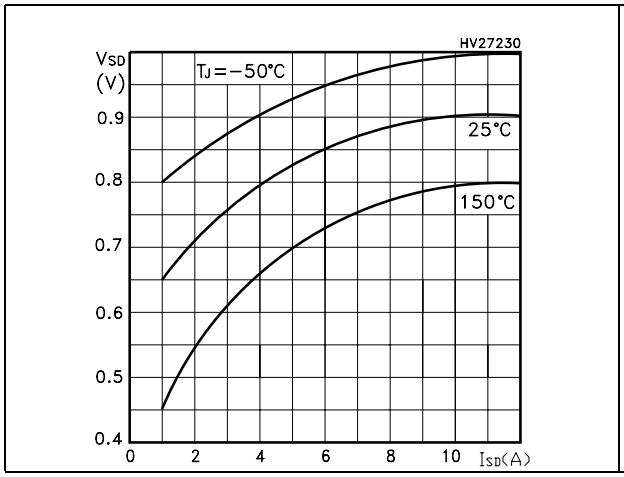
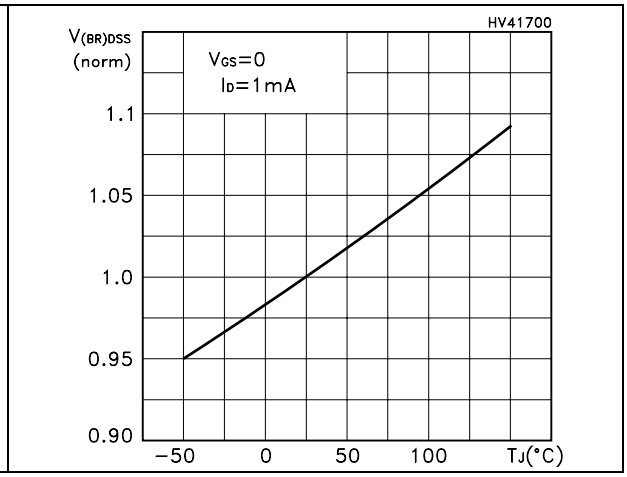


Figure 17. Normalized BV_{DSS} vs temperature



3 Test circuit

Figure 18. Switching times test circuit for resistive load

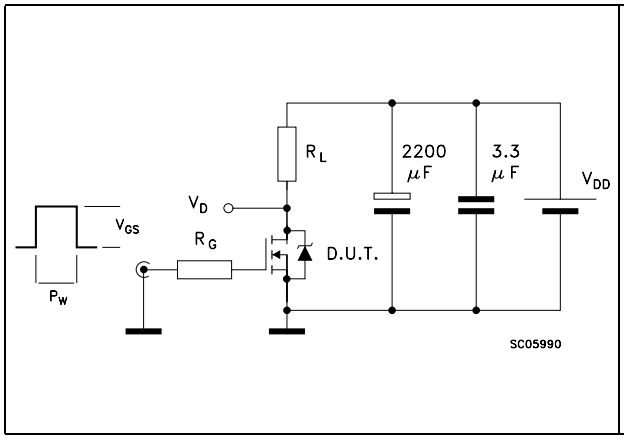


Figure 19. Gate charge test circuit

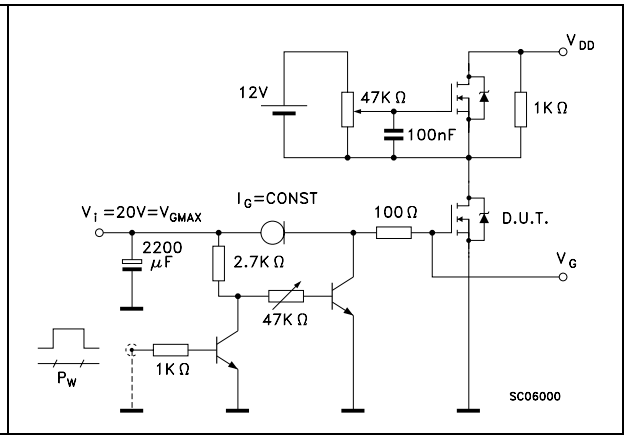


Figure 20. Test circuit for inductive load switching and diode recovery times

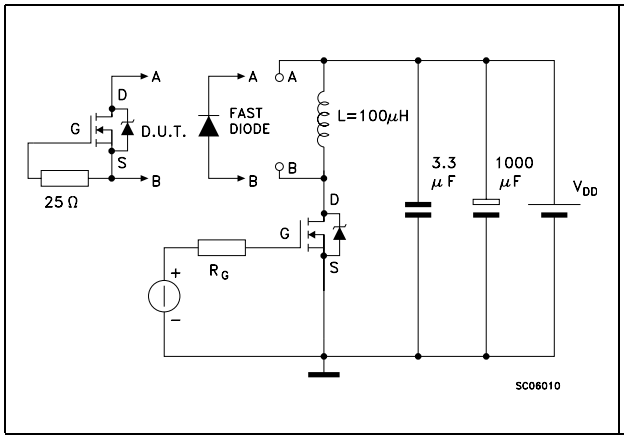


Figure 21. Unclamped inductive load test circuit

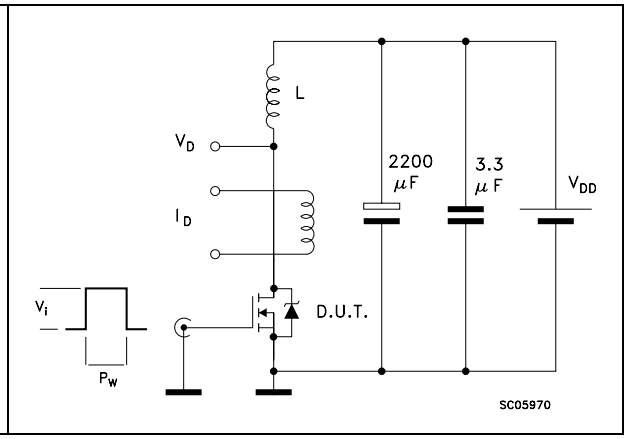


Figure 22. Unclamped inductive waveform

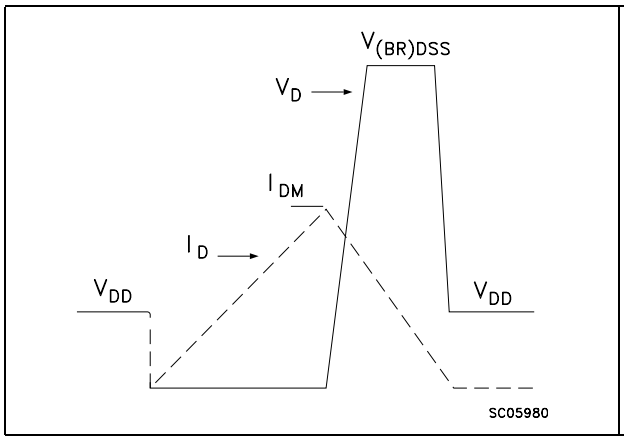
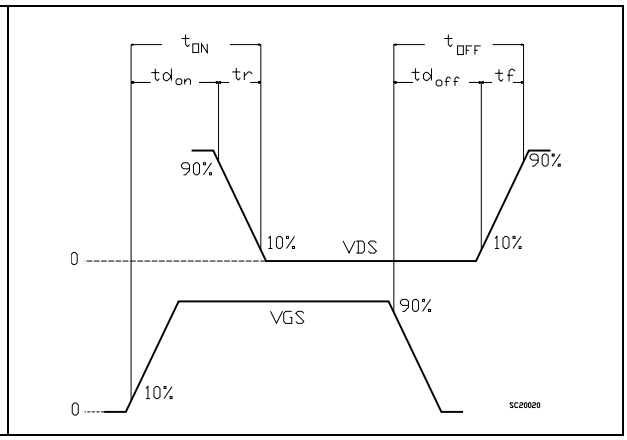


Figure 23. Switching time waveform

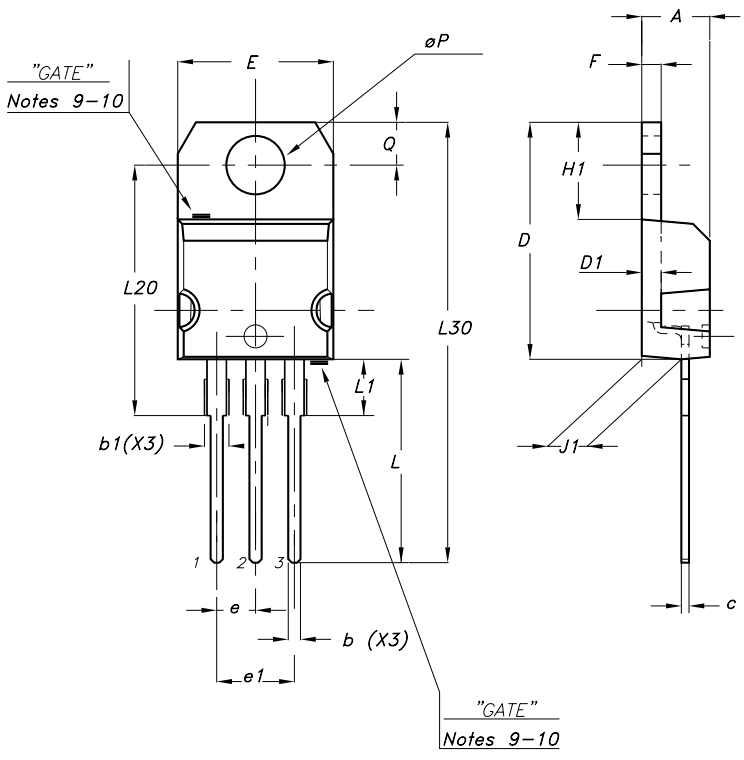


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: *www.st.com*

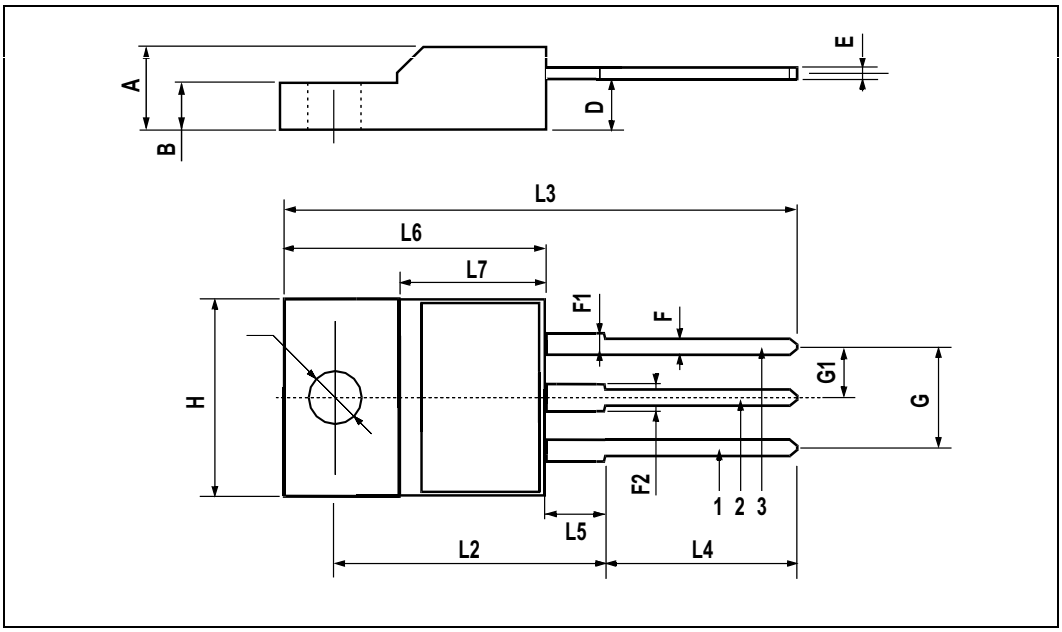
TO-220 mechanical data

Dim	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.14		1.70	0.044		0.066
c	0.48		0.70	0.019		0.027
D	15.25		15.75	0.6		0.62
D1		1.27			0.050	
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.051
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
∅P	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



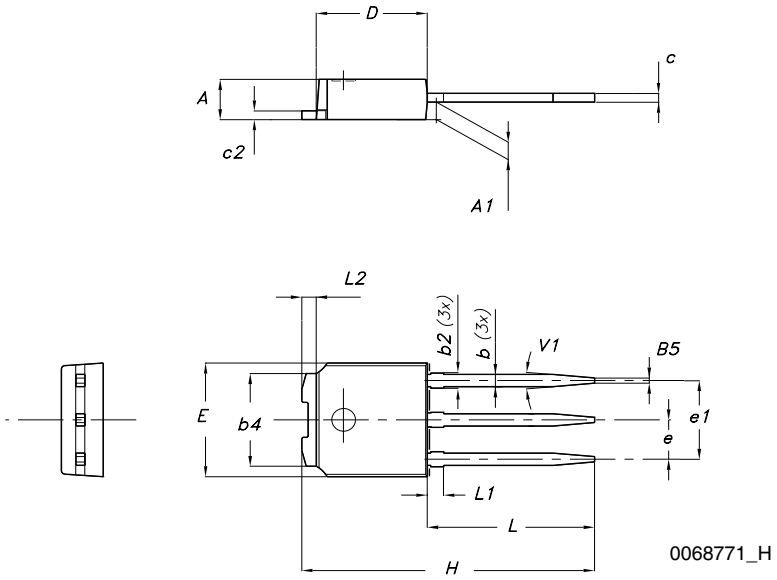
TO-220FP MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.45		0.7	0.017		0.027
F	0.75		1	0.030		0.039
F1	1.15		1.7	0.045		0.067
F2	1.15		1.7	0.045		0.067
G	4.95		5.2	0.195		0.204
G1	2.4		2.7	0.094		0.106
H	10		10.4	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.8		10.6	.0385		0.417
L5	2.9		3.6	0.114		0.141
L6	15.9		16.4	0.626		0.645
L7	9		9.3	0.354		0.366
Ø	3		3.2	0.118		0.126



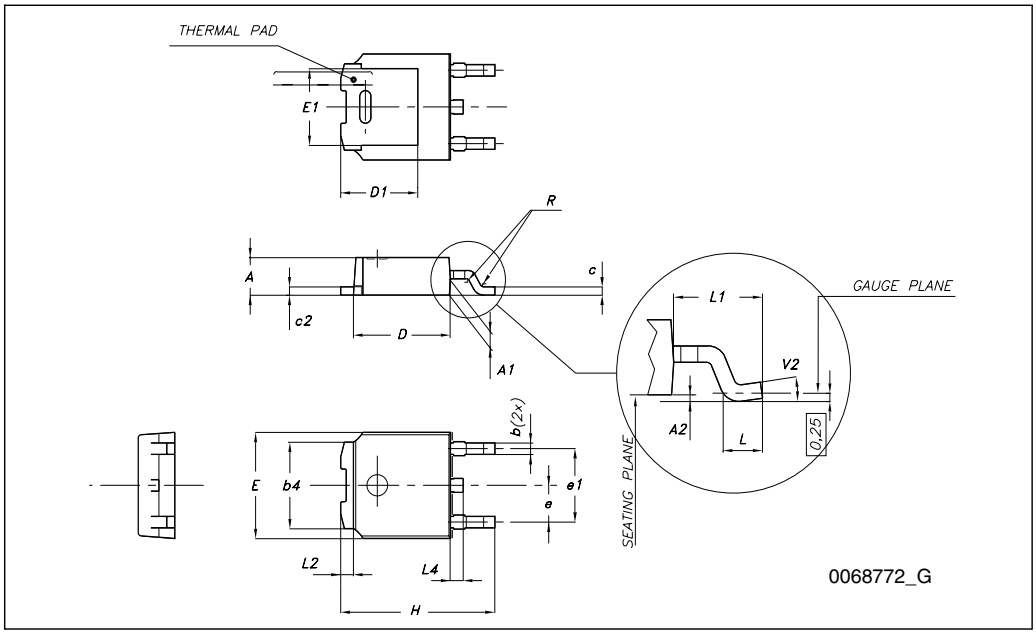
TO-251 (IPAK) mechanical data

DIM.	mm.		
	min.	typ	max.
A	2.20		2.40
A1	0.90		1.10
b	0.64		0.90
b2			0.95
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
E	6.40		6.60
e		2.28	
e1	4.40		4.60
H		16.10	
L	9.00		9.40
(L1)	0.80		1.20
L2		0.80	
V1		10 °	



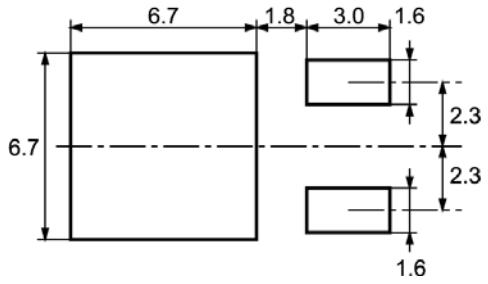
TO-252 (DPAK) mechanical data

DIM.	mm.		
	min.	typ	max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1		
L1		2.80	
L2		0.80	
L4	0.60		1
R		0.20	
V2	0 °		8 °



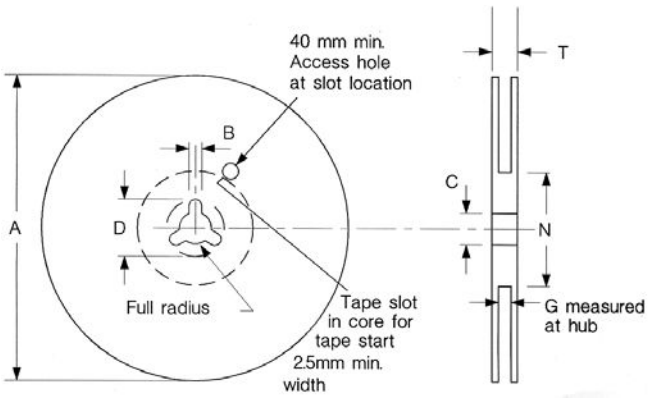
5 Package mechanical data

DPAK FOOTPRINT



All dimensions are in millimeters

TAPE AND REEL SHIPMENT



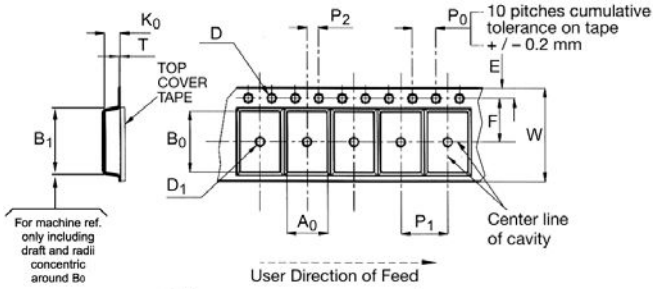
REEL MECHANICAL DATA

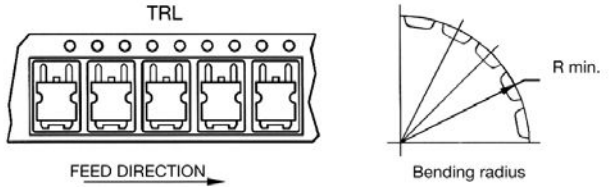
DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0.795	
G	16.4	18.4	0.645	0.724
N	50		1.968	
T		22.4		0.881

BASE QTY	BULK QTY
2500	2500

TAPE MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	6.8	7	0.267	0.275
B0	10.4	10.6	0.409	0.417
B1		12.1		0.476
D	1.5	1.6	0.059	0.063
D1	1.5		0.059	
E	1.65	1.85	0.065	0.073
F	7.4	7.6	0.291	0.299
K0	2.55	2.75	0.100	0.108
P0	3.9	4.1	0.153	0.161
P1	7.9	8.1	0.311	0.319
P2	1.9	2.1	0.075	0.082
R	40		1.574	
W	15.7	16.3	0.618	0.641





6 Revision history

Table 9. Document revision history

Date	Revision	Changes
26-Oct-2007	1	Initial release.
07-Feb-2008	2	Document status promoted from preliminary data to datasheet.
14-Oct-2008	3	*Table 4: Avalanche characteristics* has been corrected.