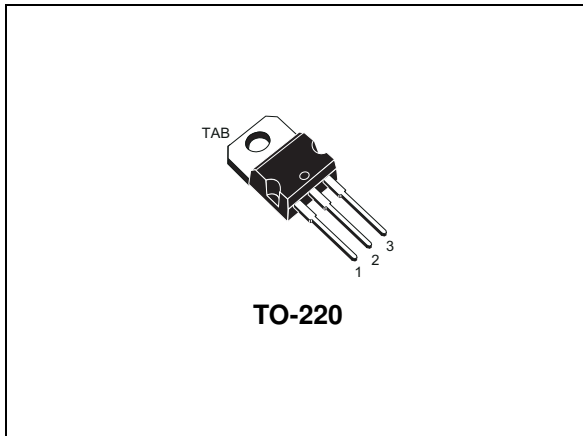
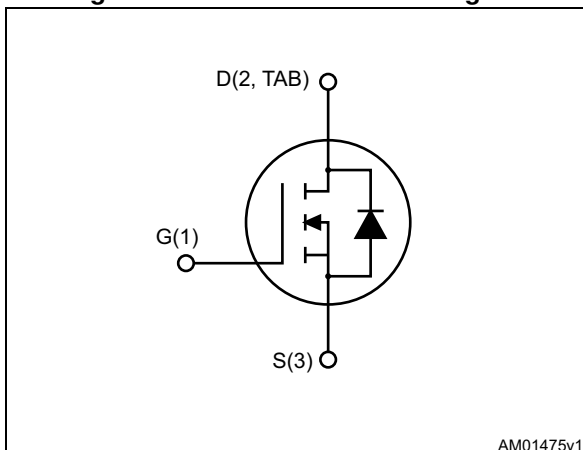


## N-channel 68 V, 0.0055 $\Omega$ typ., 110 A, STripFET™ F6 Power MOSFET in a TO-220 package

Datasheet - production data



**Figure 1. Internal schematic diagram**



### Features

Order code	$V_{DS}$	$R_{DS(on)max.}$	$I_D$	$P_{TOT}$
STP110N7F6	68 V	0.0065 $\Omega$	110 A	176 W

- Very low on-resistance
- Very low gate charge
- High avalanche ruggedness
- Low gate drive power loss

### Applications

- Switching applications

### Description

This device is an N-channel Power MOSFET developed using the STripFET™ F6 technology with a new trench gate structure. The resulting Power MOSFET exhibits very low  $R_{DS(on)}$  in all packages.

**Table 1. Device summary**

Order code	Marking	Package	Packing
STP110N7F6	110N7F6	TO-220	Tube

# Contents

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	68	V
$V_{GS}$	Gate- source voltage	$\pm 20$	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	110	A
	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	80	A
$I_{DM}^{(1)}$	Drain current (pulsed) $T_C = 25\text{ }^\circ\text{C}$	440	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	176	W
$E_{AS}^{(2)}$	Single pulse avalanche energy	185	mJ
$T_J$	Operating junction temperature range	-55 to 175	$^\circ\text{C}$
$T_{stg}$	Storage temperature range		$^\circ\text{C}$

1. Pulse width is limited by safe operating area

2. Starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $I_D = 35\text{ A}$ ,  $V_{DD} = 50\text{ V}$

**Table 3. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max.	0.85	$^\circ\text{C/W}$
$R_{thj-amb}$	Thermal resistance junction-ambient max.	62.5	$^\circ\text{C/W}$

## 2 Electrical characteristics

( $T_C = 25\text{ °C}$  unless otherwise specified)

**Table 4. On/off-states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0, I_D = 1\text{ mA}$	68			V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0, V_{DS} = 68\text{ V}$			1	$\mu\text{A}$
		$V_{GS} = 0, V_{DS} = 68\text{ V}, T_C = 125\text{ °C}$ (1)			100	$\mu\text{A}$
$I_{GSS}$	Gate-body leakage current	$V_{DS} = 0, V_{GS} = +20\text{ V}$			100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2		4	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}, I_D = 55\text{ A}$		0.0055	0.0065	$\Omega$

1. Defined by design, not subject to production test.

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 25\text{ V}, f = 1\text{ MHz}, V_{GS} = 0$	-	5850	-	pF
$C_{oss}$	Output capacitance			340		pF
$C_{riss}$	Reverse transfer capacitance			240		pF
$Q_g$	Total gate charge	$V_{DD} = 34\text{ V}, I_D = 110\text{ A}, V_{GS} = 10\text{ V}$ (see <a href="#">Figure 14</a> )	-	100	-	nC
$Q_{gs}$	Gate-source charge			32		nC
$Q_{gd}$	Gate-drain charge			19		nC

**Table 6. Switching times**

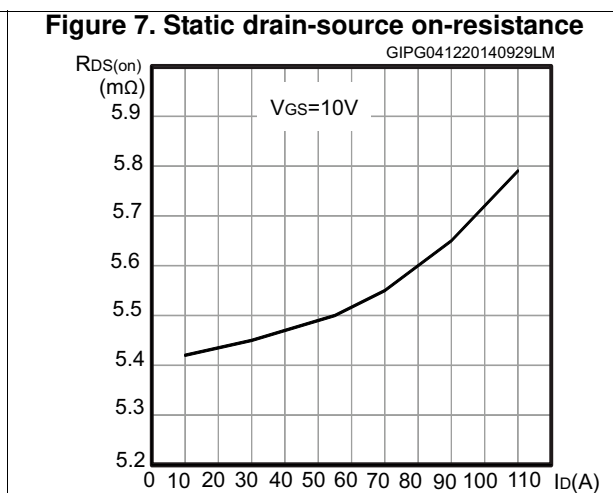
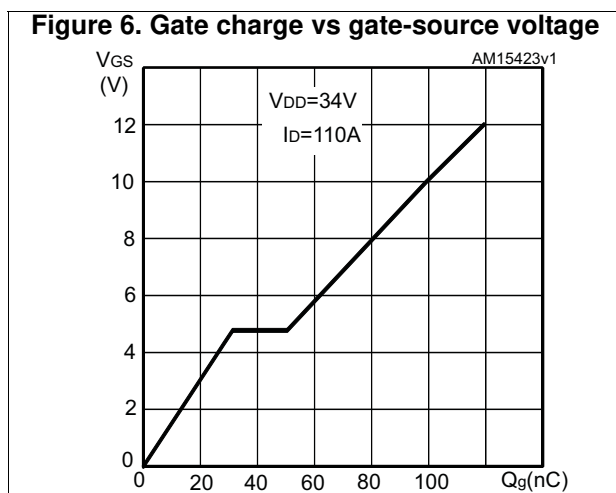
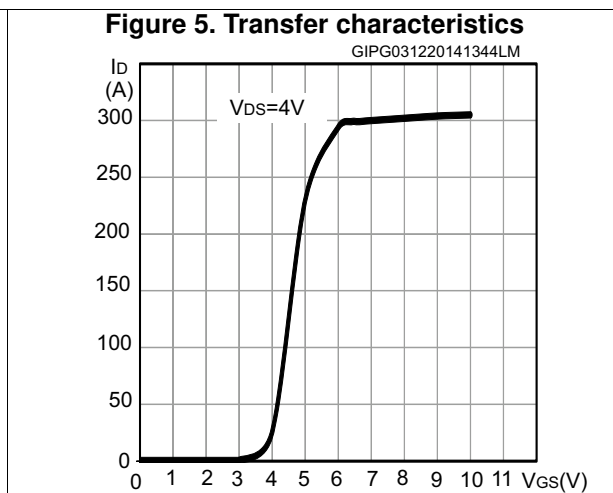
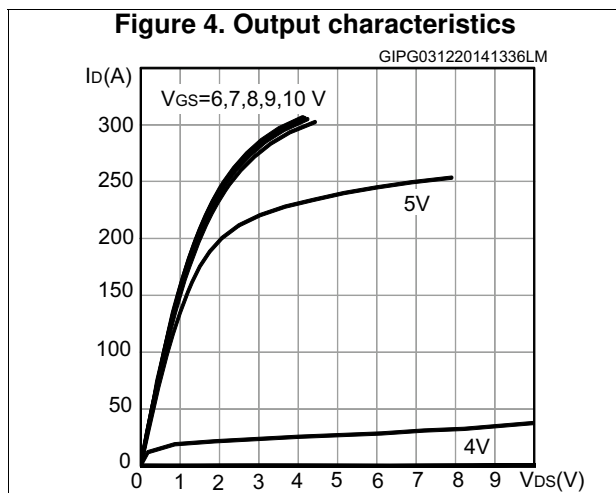
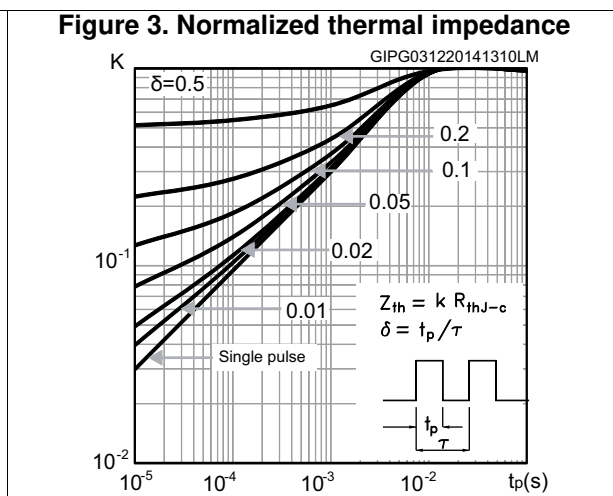
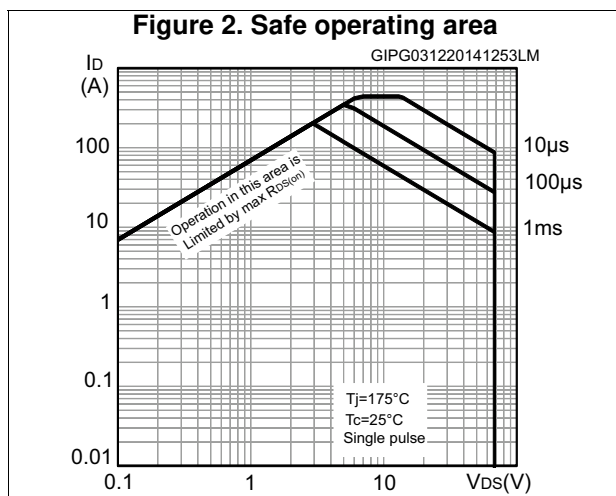
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 34\text{ V}, I_D = 55\text{ A}, R_G = 4.7\text{ }\Omega, V_{GS} = 10\text{ V}$ (see <a href="#">Figure 13</a> )	-	23	-	ns
$t_r$	Rise time			29		ns
$t_{d(off)}$	Turn-off delay time			103		ns
$t_f$	Fall time			23		ns

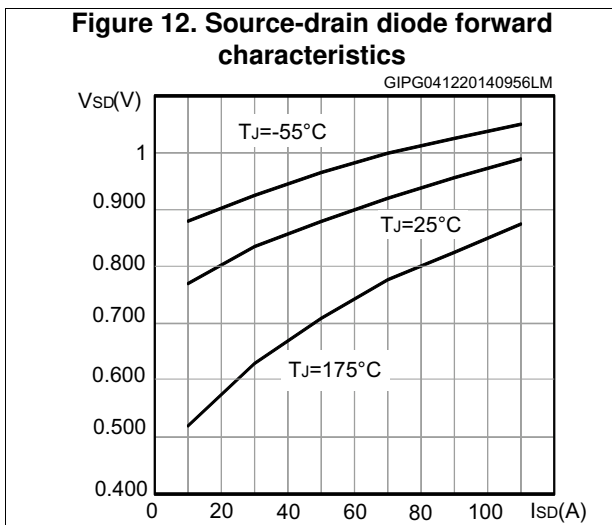
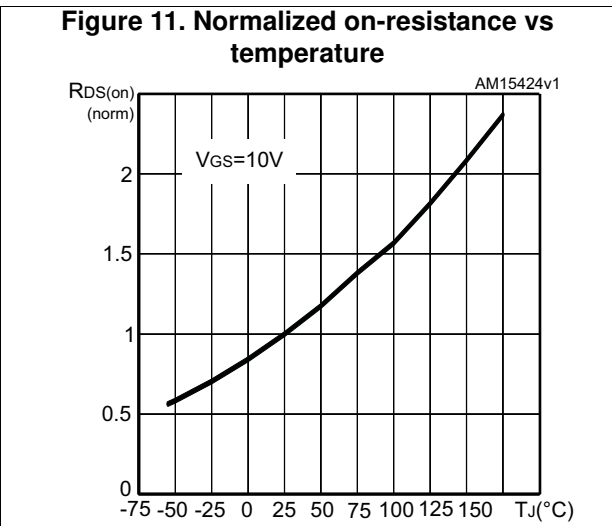
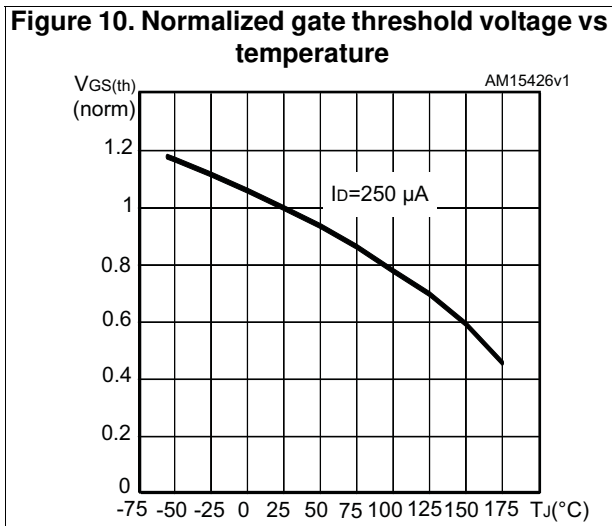
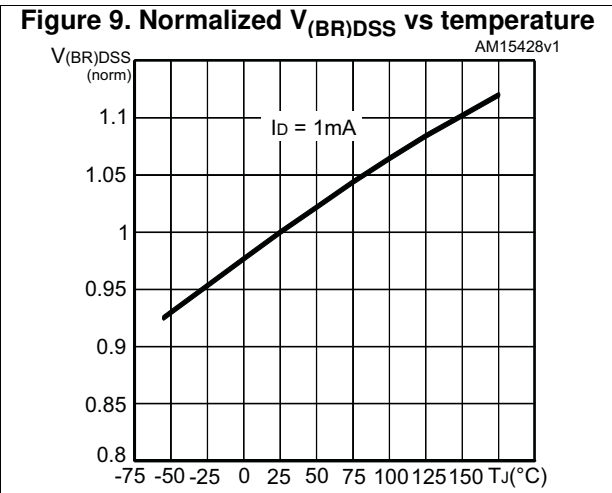
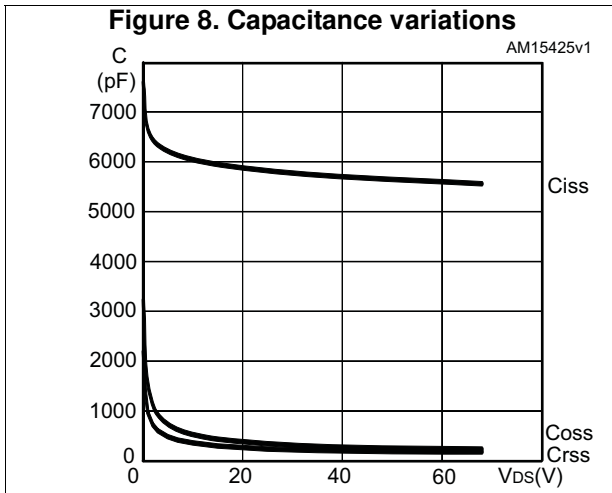
Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{SD}^{(1)}$	Forward on voltage	$I_{SD} = 110 \text{ A}$ , $V_{GS} = 0$	-		1.2	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 110 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 54 \text{ V}$ , (see <a href="#">Figure 15</a> )		31		ns
$Q_{rr}$	Reverse recovery charge			39		nC
$I_{RRM}$	Reverse recovery current			2.6		A

1. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)





### 3 Test circuits

Figure 13. Switching times test circuit for resistive load

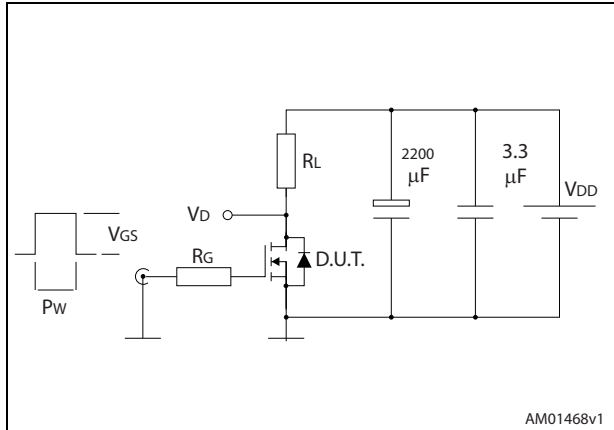


Figure 14. Gate charge test circuit

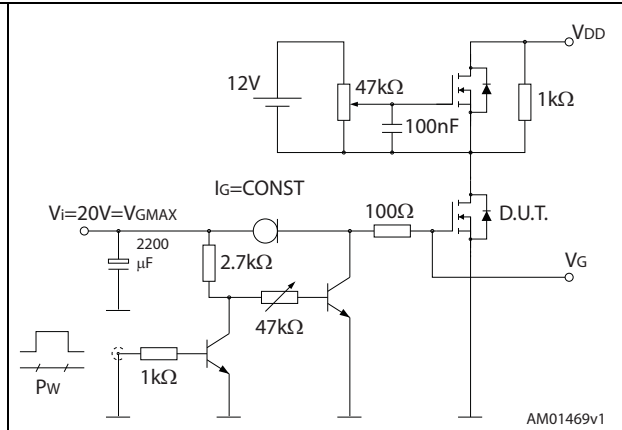


Figure 15. Test circuit for inductive load switching and diode recovery times

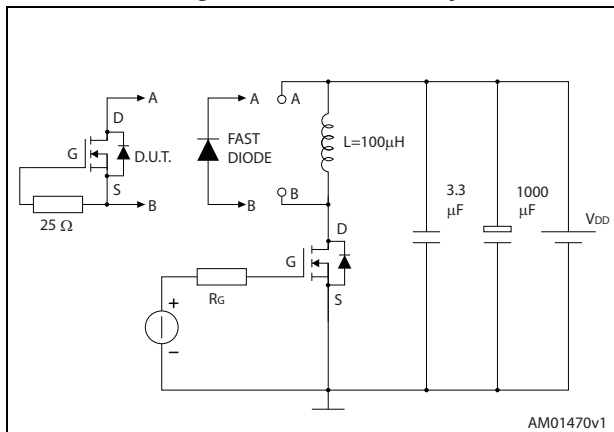


Figure 16. Unclamped inductive load test circuit

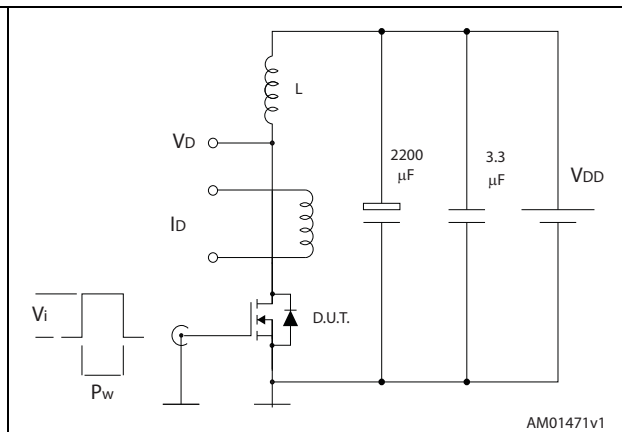


Figure 17. Unclamped inductive waveform

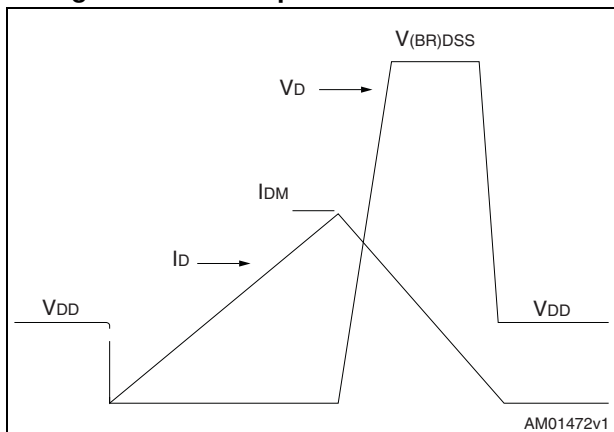
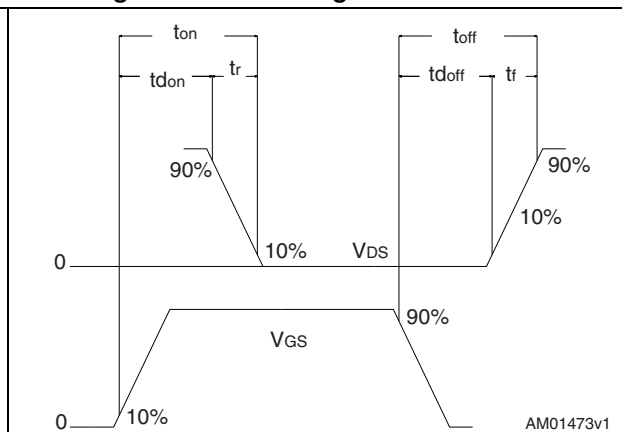


Figure 18. Switching time waveform





## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

### 4.1 TO-220 package information

Figure 19. TO-220 type A package outline

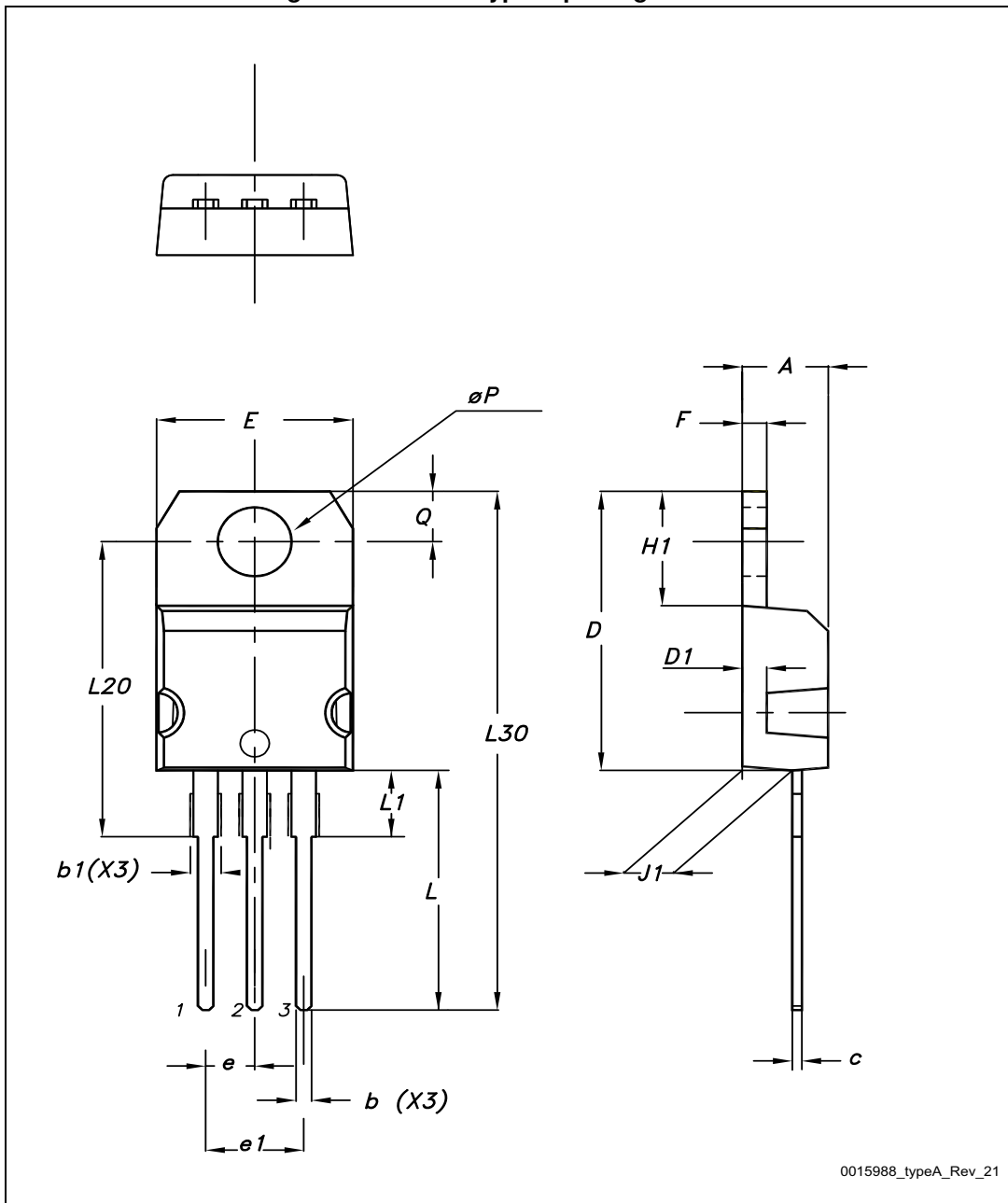


Table 8. TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95

## 5 Revision history

**Table 9. Document revision history**

Date	Revision	Changes
04-Dec-2014	1	First release.
30-Mar-2015	2	Document status promoted from preliminary to production data.
13-Oct-2016	3	Updated <a href="#">Figure 11: Normalized on-resistance vs temperature</a> and <a href="#">Section 4.1: TO-220 package information</a> . Minor text changes.

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