



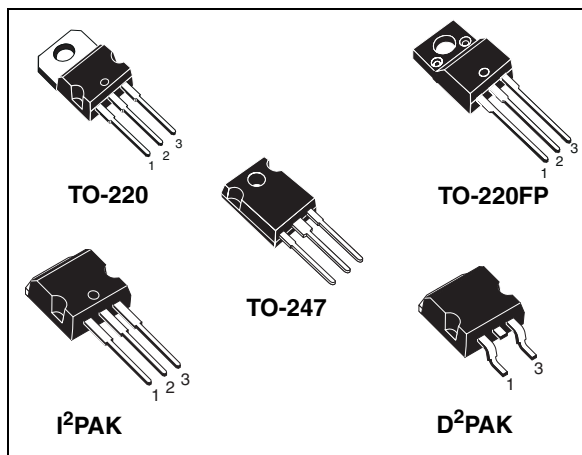
# STP14NK50Z - STP14NK50ZFP STB14NK50Z-STB14NK50Z-1-STW14NK50Z

N-channel 500V - 0.34Ω - 14A TO-220/FP/D<sup>2</sup>PAK/I<sup>2</sup>PAK/TO-247  
Zener-protected SuperMESH™ Power MOSFET

## General features

Type	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>	P <sub>w</sub>
STP14NK50Z	500V	<0.38Ω	14A	150W
STP14NK50ZFP	500V	<0.38Ω	14A	35W
STB14NK50Z	500V	<0.38Ω	14A	150W
STB14NK50Z-1	500V	<0.38Ω	14A	150W
STW14NK50Z	500V	<0.38Ω	14A	150W

- Extremely high dv/dt capability
- 100% avalanche tested
- Gate charge minimized
- Very low intrinsic capacitances
- Very good manufacturing repeatability



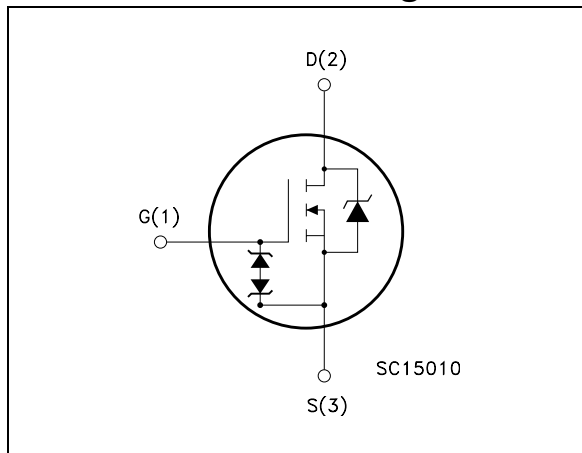
## Description

The SuperMESH™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications. Such series complements ST full range of high voltage MOSFETs including revolutionary MDmesh™ products.

## Applications

- Switching application

## Internal schematic diagram



## Order codes

Part number	Marking	Package	Packaging
STP14NK50Z	P14NK50Z	TO-220	Tube
STP14NK50ZFP	P14NK50ZFP	TO-220FP	Tube
STB14NK50ZT4	B14NK50Z	D <sup>2</sup> PAK	Tape & reel
STB14NK50Z-1	B14NK50Z	I <sup>2</sup> PAK	Tube
STW14NK50Z	W14NK50Z	TO-247	Tube

## Contents

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# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value			Unit
		TO-220 I <sup>2</sup> PAK/D <sup>2</sup> PAK	TO-220FP	TO-247	
V <sub>DS</sub>	Drain-source voltage (V <sub>GS</sub> = 0)	500			V
V <sub>DGR</sub>	Drain-gate voltage (R <sub>GS</sub> = 20KΩ)	500			V
V <sub>GS</sub>	Gate-source voltage	± 30			V
I <sub>D</sub>	Drain current (continuous) at T <sub>C</sub> = 25°C	14	14 <sup>(1)</sup>	14	A
I <sub>D</sub>	Drain current (continuous) at T <sub>C</sub> =100°C	7.6	7.6 <sup>(1)</sup>	7.6	A
I <sub>DM</sub> <sup>(2)</sup>	Drain current (pulsed)	48	48 <sup>(1)</sup>	48	A
P <sub>TOT</sub>	Total dissipation at T <sub>C</sub> = 25°C	150	35	150	W
	Derating factor	1.20	0.28	1.20	W/°C
Vesd(G-S)	G-S ESD (HBM C=100pF, R=1.5kΩ)	4000			KV
dv/dt <sup>(3)</sup>	Peak diode recovery voltage slope	4.5			V/ns
V <sub>ISO</sub>	Insulation withstand voltage (DC)	--	2500		V
T <sub>J</sub> T <sub>stg</sub>	Operating junction temperature Storage temperature	-55 to 150			°C

1. Limited only by maximum temperature allowed
2. Pulse width limited by safe operating area
3. I<sub>SD</sub> ≤ 3A, di/dt ≤ 200A/μs, V<sub>DD</sub> ≤ V<sub>(BR)DSS</sub>, T<sub>J</sub> ≤ T<sub>JMAX</sub>

**Table 2. Thermal data**

Symbol	Parameter	Value				Unit
		TO-220 I <sup>2</sup> PAK	D <sup>2</sup> PAK	TO-220FP	TO-247	
R <sub>thj-case</sub>	Thermal resistance junction-case Max	0.83		3.6	0.83	°C/ W
R <sub>thj-pcb</sub>	Thermal resistance junction-pcb Max (1)		60			°C/ W
R <sub>thj-a</sub>	Thermal resistance junction-ambient Max	62.5			50	°C/ W
T <sub>I</sub>	Maximum lead temperature for soldering purpose	300				°C

1. When mounted on minimum footprint

**Table 3. Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AR}$	Avalanche current, repetitive or not-repetitive (pulse width limited by Tj Max)	12	A
$E_{AS}$	Single pulse avalanche energy (starting Tj=25°C, Id=Iar, Vdd=50V)	400	mJ

**Table 4. Gate-source zener diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$BV_{GSO}$	Gate-source breakdown voltage	Igs=±1mA (Open Drain)	30			V

## 1.1 Protection features og gate-to-source zener diodes

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device’s ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device’s integrity. These integrated Zener diodes thus avoid the usage of external components.

## 2 Electrical characteristics

(T<sub>CASE</sub>=25°C unless otherwise specified)

**Table 5. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source breakdown voltage	I <sub>D</sub> = 1mA, V <sub>GS</sub> = 0	500			V
I <sub>DSS</sub>	Zero gate voltage drain current (V <sub>GS</sub> = 0)	V <sub>DS</sub> = Max rating, V <sub>DS</sub> = Max rating, T <sub>C</sub> = 125°C			1 50	μA μA
I <sub>GSS</sub>	Gate body leakage current (V <sub>DS</sub> = 0)	V <sub>GS</sub> = ±20V			±10	nA
V <sub>GS(th)</sub>	Gate threshold voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 100μA	3	3.75	4.5	V
R <sub>DS(on)</sub>	Static drain-source on resistance	V <sub>GS</sub> = 10V, I <sub>D</sub> = 6A		0.34	0.38	Ω

**Table 6. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g <sub>fs</sub> <sup>(1)</sup>	Forward transconductance	V <sub>DS</sub> = 8V, I <sub>D</sub> = 6A		12		S
C <sub>iSS</sub> C <sub>oss</sub> C <sub>rSS</sub>	Input capacitance Output capacitance Reverse transfer capacitance	V <sub>DS</sub> = 25V, f = 1 MHz, V <sub>GS</sub> = 0		2000 238 55		pF pF pF
C <sub>oss eq</sub> <sup>(2)</sup>	Equivalent output capacitance	V <sub>GS</sub> = 0, V <sub>DS</sub> = 0V to 400V		150		pF
Q <sub>g</sub> Q <sub>gs</sub> Q <sub>gd</sub>	Total gate charge Gate-source charge Gate-drain charge	V <sub>DD</sub> = 400V, I <sub>D</sub> = 12A V <sub>GS</sub> = 10V		69 12 31	92	nC nC nC

1. Pulsed: pulse duration=300μs, duty cycle 1.5%

2. C<sub>oss eq</sub> is defined as a constant equivalent capacitance giving the same charging time as C<sub>oss</sub> when V<sub>DS</sub> increases from 0 to 80% V<sub>DSS</sub>

**Table 7. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t <sub>d(on)</sub> t <sub>r</sub>	Turn-on delay time Rise time	V <sub>DD</sub> = 250 V, I <sub>D</sub> = 6A, R <sub>G</sub> = 4.7Ω, V <sub>GS</sub> = 10V (see Figure 19)		24 16		ns ns

**Table 7. Switching times**

$t_{d(off)}$	Turn-off delay time	$V_{DD}=250V, I_D=6A,$ $R_G=4.7\Omega, V_{GS}=10V$ (see Figure 19)		54		ns
$t_f$	Fall time			12		ns
$t_{r(Voff)}$	Off-voltage rise time	$V_{DD}=400V, I_D=12A,$ $R_G=4.7\Omega, V_{GS}=10V$ (see Figure 21)		9.5		ns
$t_f$	Fall time			9		ns
$t_c$	Cross-over time			20		ns

**Table 8. Source drain diode**

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
$I_{SD}$	Source-drain current				12	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				48	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD}=12A, V_{GS}=0$			1.6	V
$t_{rr}$	Reverse recovery time	$I_{SD}=12A,$ $di/dt = 100A/\mu s,$ $V_{DD}=35V, T_J=150^\circ C$ (see Figure 21)		470		ns
$Q_{rr}$	Reverse recovery charge			3.1		$\mu C$
$I_{RRM}$	Reverse recovery current			13.2		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300 $\mu s$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

Figure 2. Thermal impedance

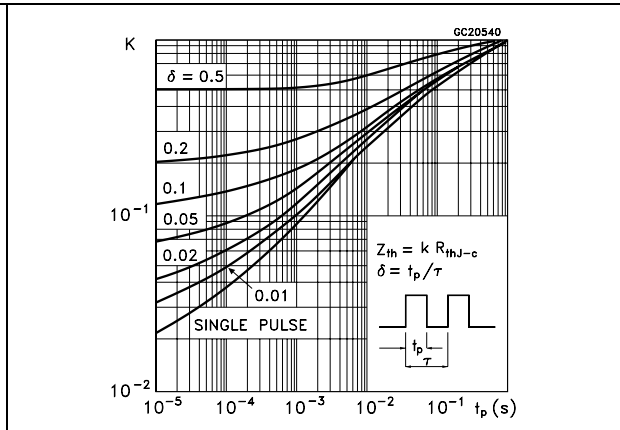
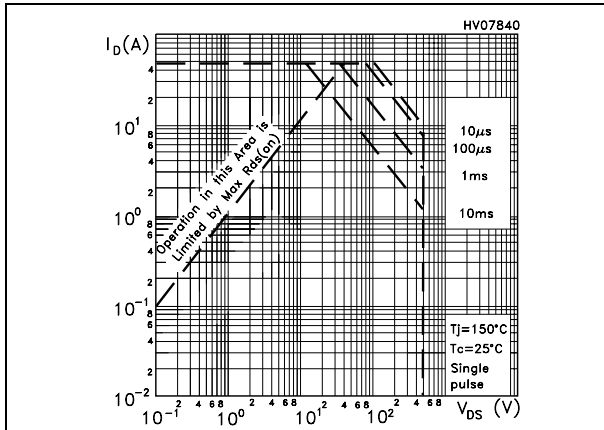


Figure 3. Safe operating area for TO-220FP

Figure 4. Thermal impedance for TO-220FP

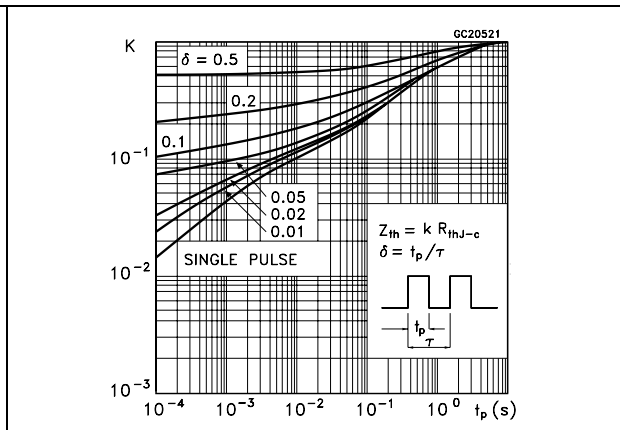
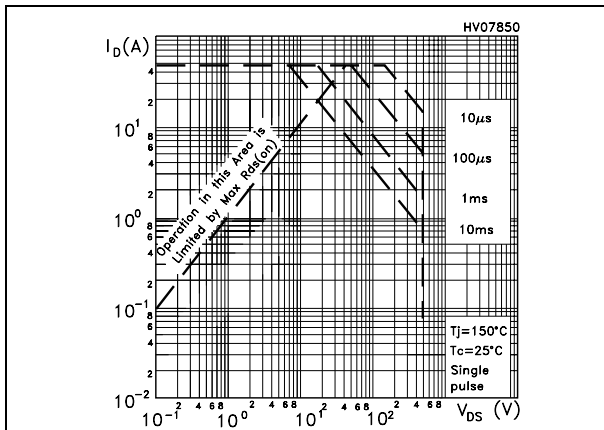


Figure 5. Safe operating area for TO-247

Figure 6. Thermal impedance for TO-247

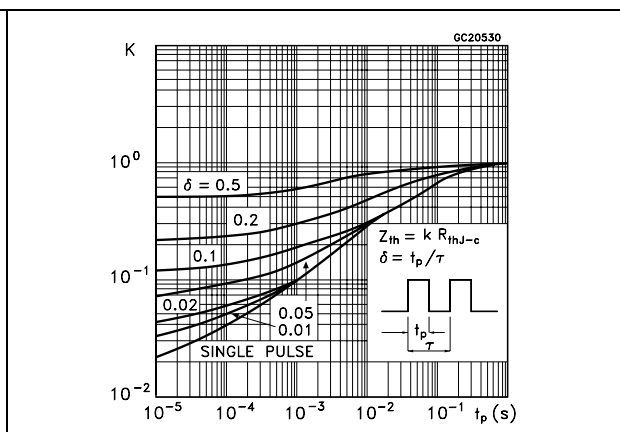
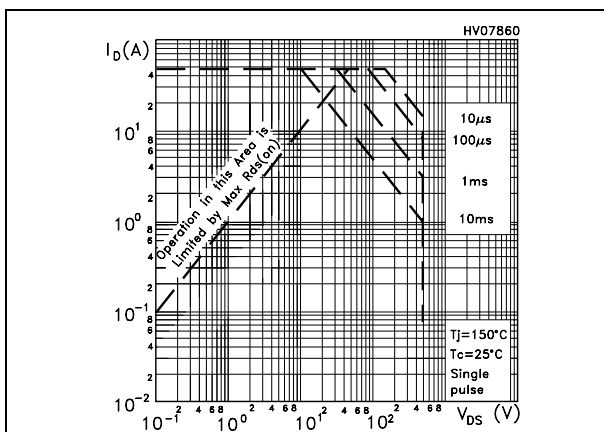


Figure 7. Output characteristics

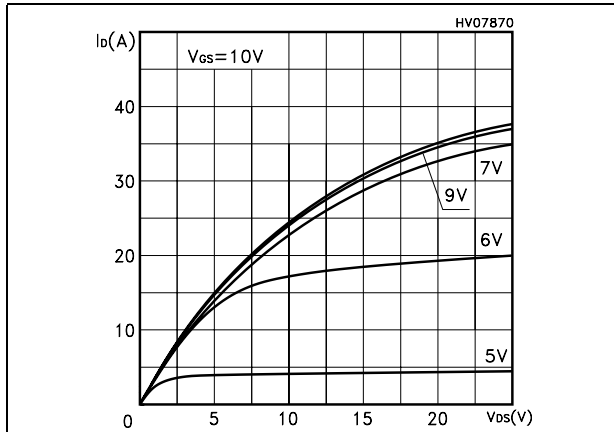


Figure 8. Transfer characteristics

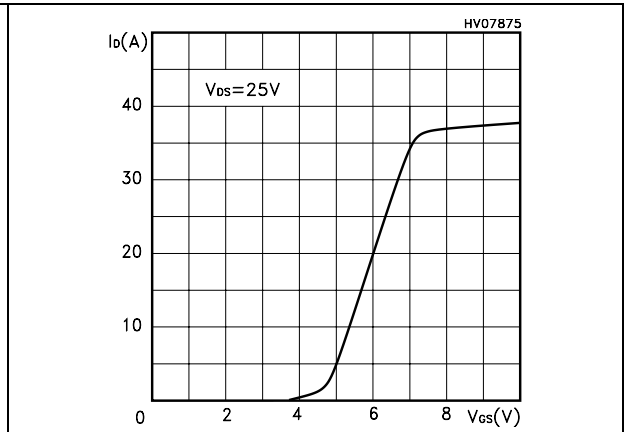


Figure 9. Transconductance

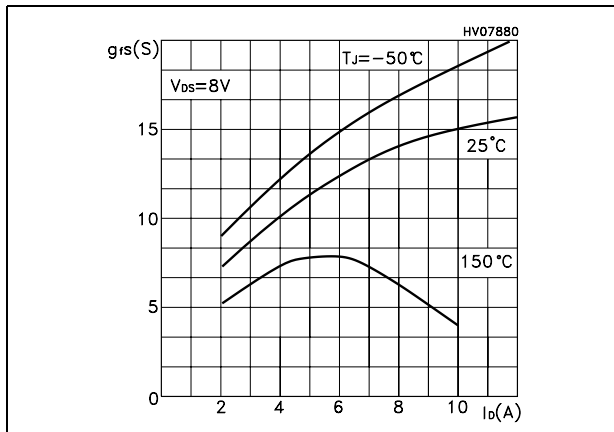


Figure 10. Static drain-source on resistance

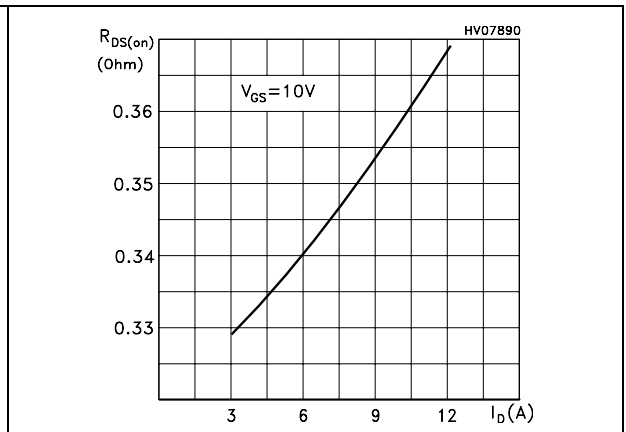


Figure 11. Gate charge vs gate-source voltage

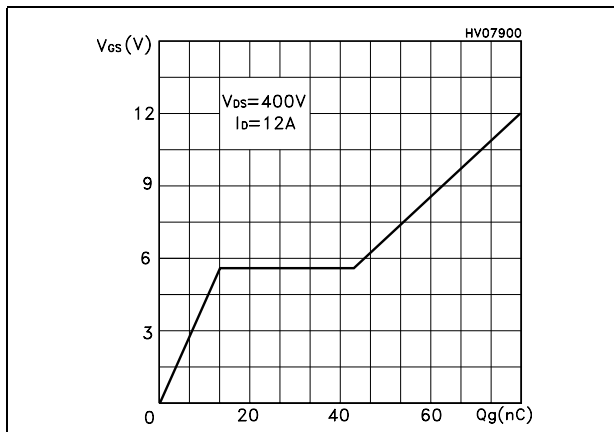


Figure 12. Capacitance variations

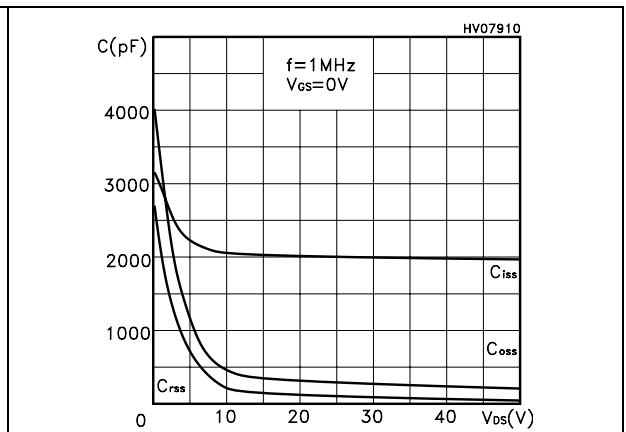




Figure 13. Normalized gate threshold voltage vs temperature

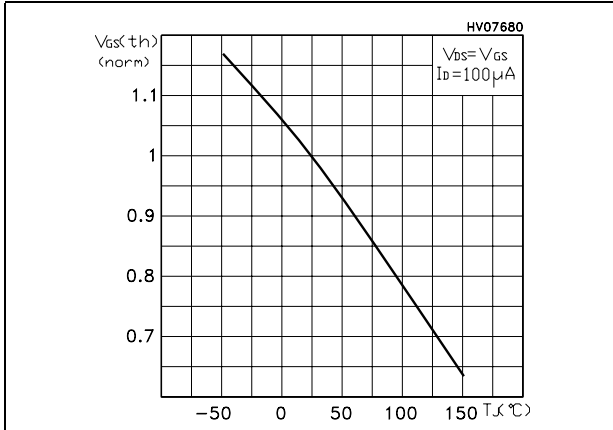


Figure 14. Normalized on resistance vs temperature

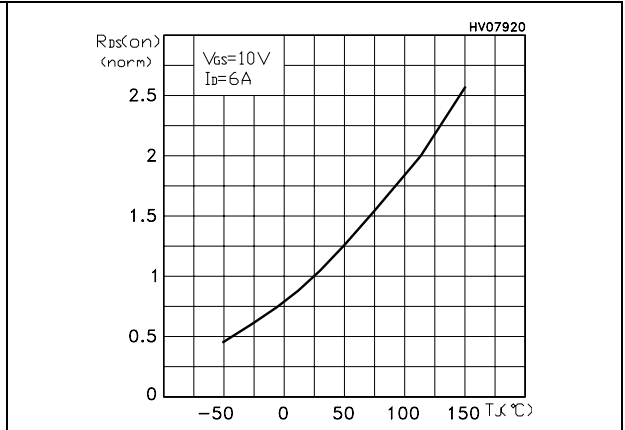


Figure 15. Source-drain diode forward characteristics

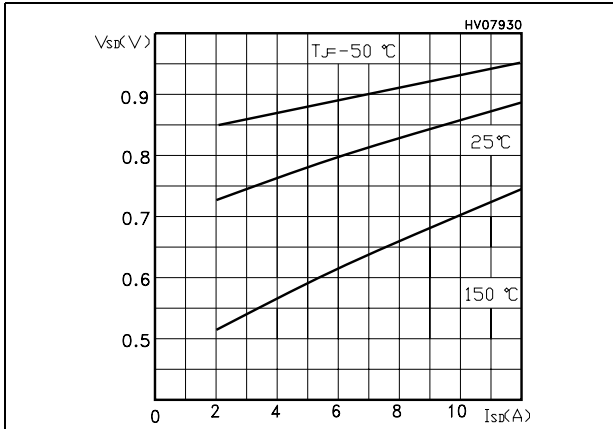


Figure 16. Normalized BV<sub>DSS</sub> vs temperature

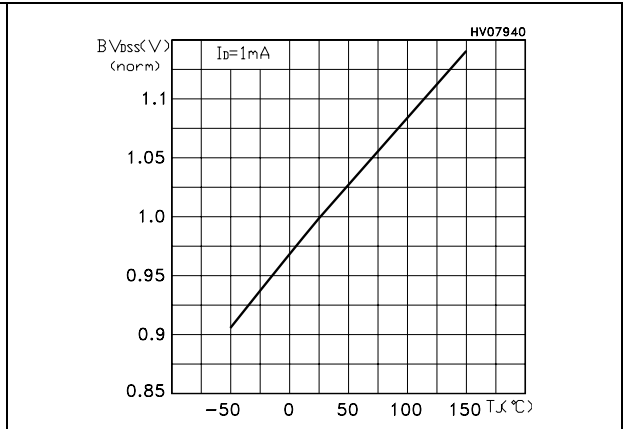


Figure 17. Normalized BV<sub>gs0</sub> vs temperature

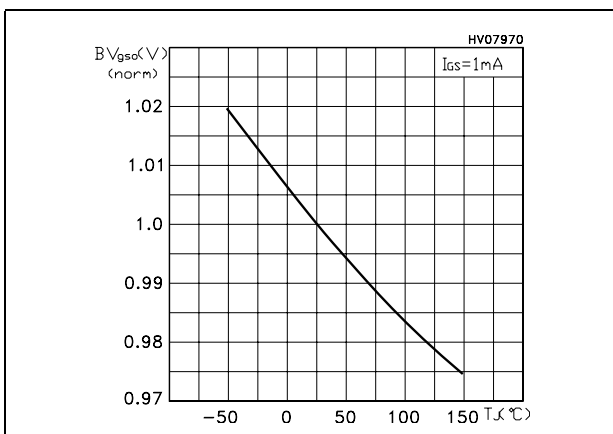
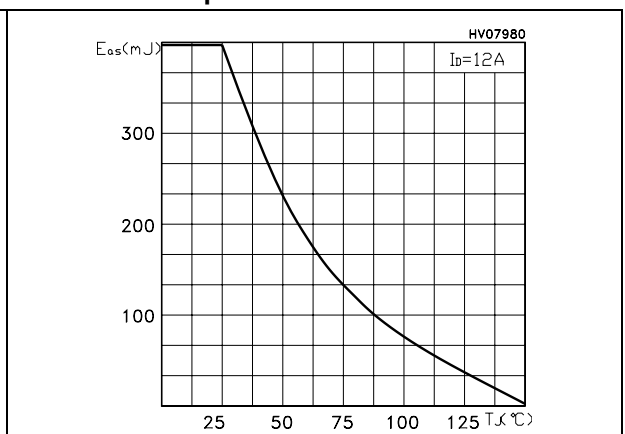


Figure 18. Maximum avalanche energy vs temperature



### 3 Test circuit

Figure 19. Switching times test circuit for resistive load

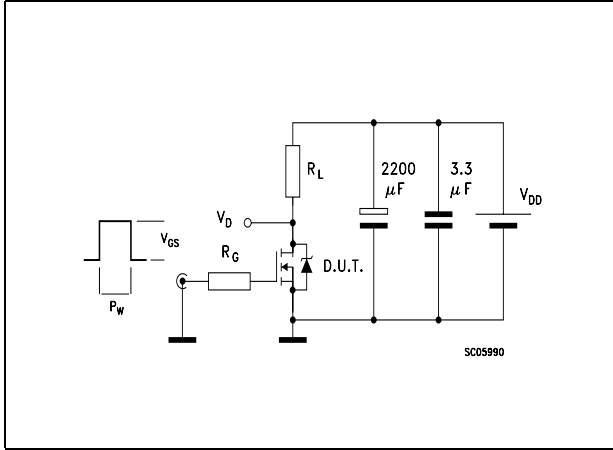


Figure 20. Gate charge test circuit

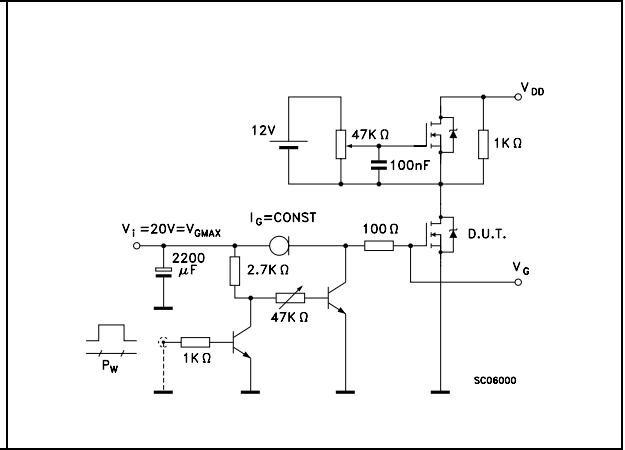


Figure 21. Test circuit for inductive load switching and diode recovery times

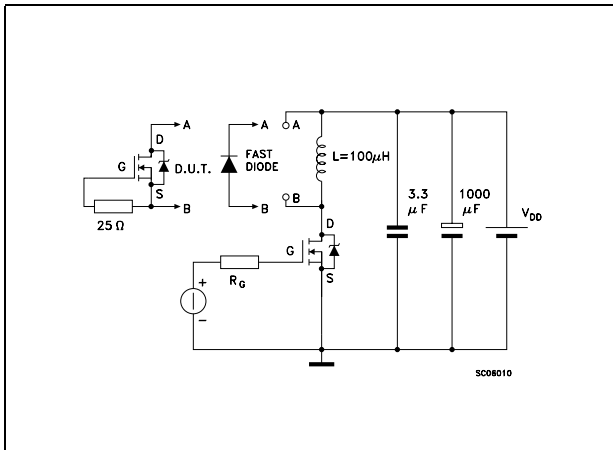


Figure 22. Unclamped Inductive load test circuit

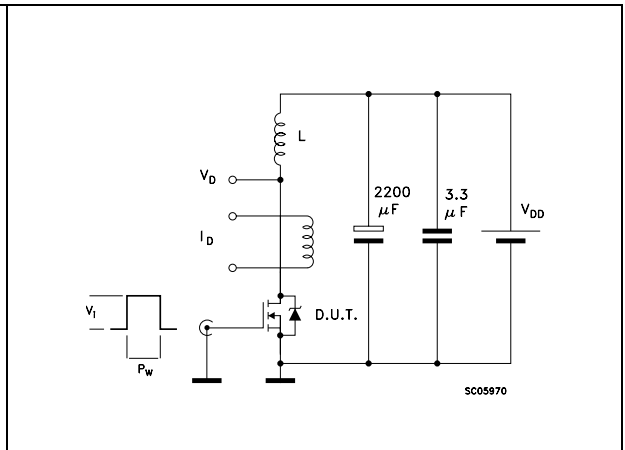


Figure 23. Unclamped inductive waveform

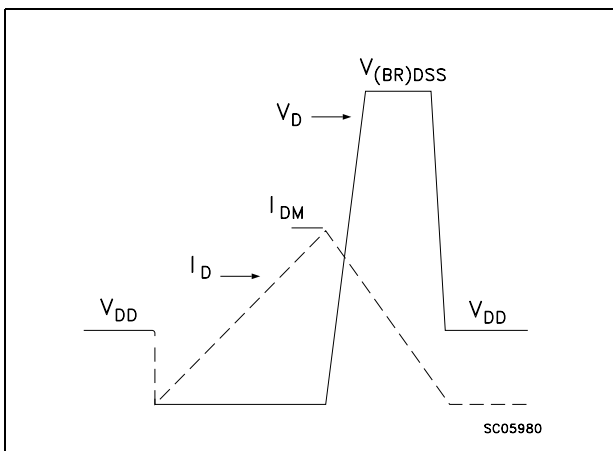
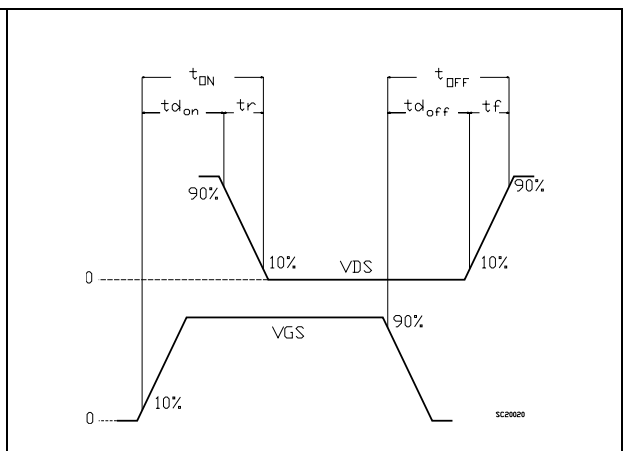


Figure 24. Switching time waveform

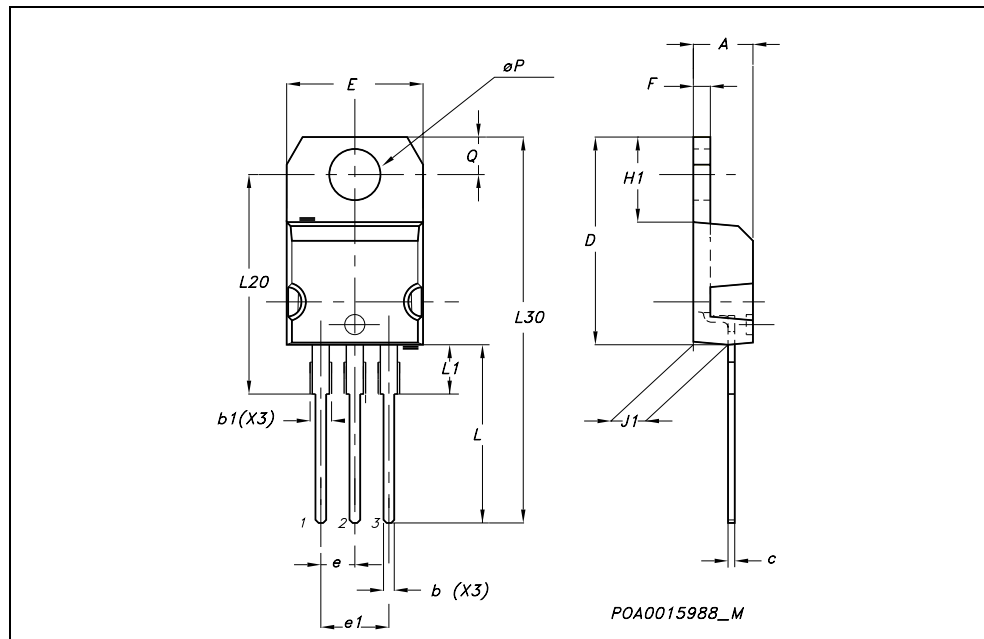


## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)

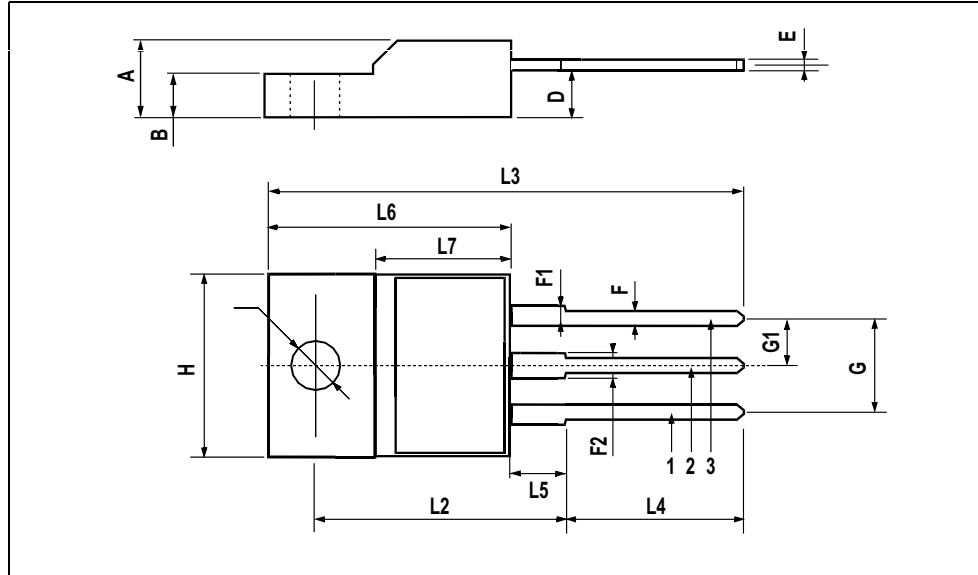
**TO-220 MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.15		1.70	0.045		0.066
c	0.49		0.70	0.019		0.027
D	15.25		15.75	0.60		0.620
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.052
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
øP	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



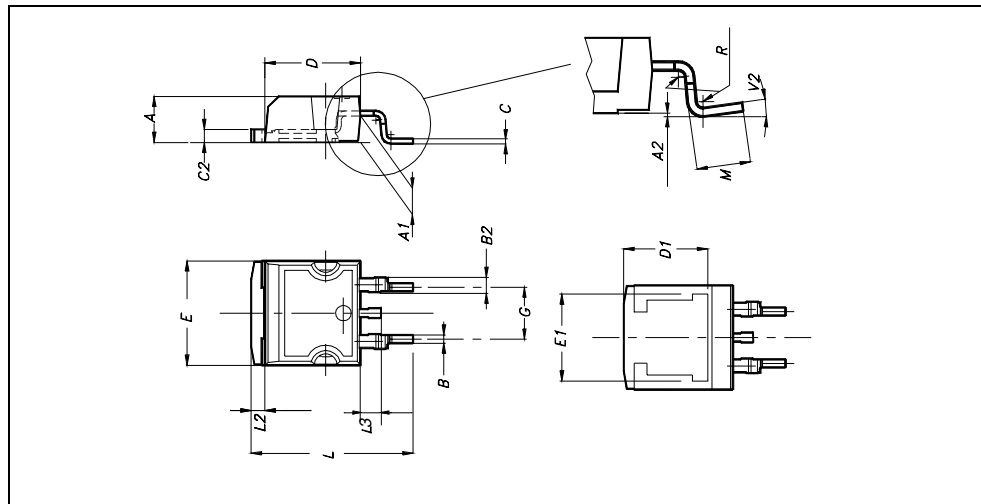
**TO-220FP MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.45		0.7	0.017		0.027
F	0.75		1	0.030		0.039
F1	1.15		1.7	0.045		0.067
F2	1.15		1.7	0.045		0.067
G	4.95		5.2	0.195		0.204
G1	2.4		2.7	0.094		0.106
H	10		10.4	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.8		10.6	.0385		0.417
L5	2.9		3.6	0.114		0.141
L6	15.9		16.4	0.626		0.645
L7	9		9.3	0.354		0.366
Ø	3		3.2	0.118		0.126



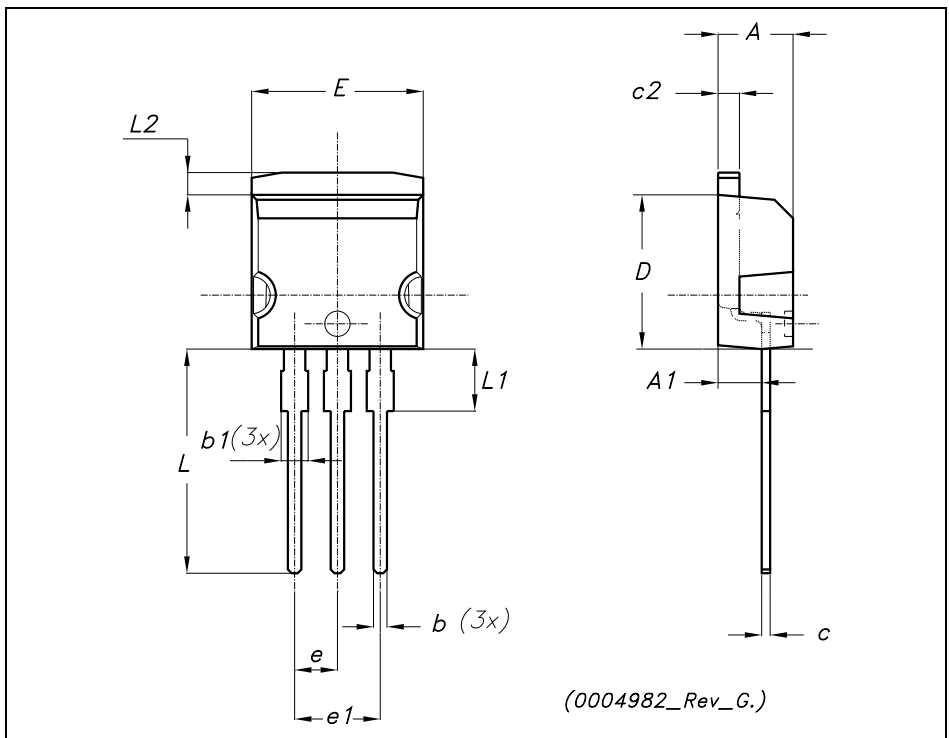
**D<sup>2</sup>PAK MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
A2	0.03		0.23	0.001		0.009
B	0.7		0.93	0.027		0.036
B2	1.14		1.7	0.044		0.067
C	0.45		0.6	0.017		0.023
C2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
D1		8			0.315	
E	10		10.4	0.393		
E1		8.5			0.334	
G	4.88		5.28	0.192		0.208
L	15		15.85	0.590		0.625
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.068
M	2.4		3.2	0.094		0.126
R		0.4			0.015	
V2	0°		4°			



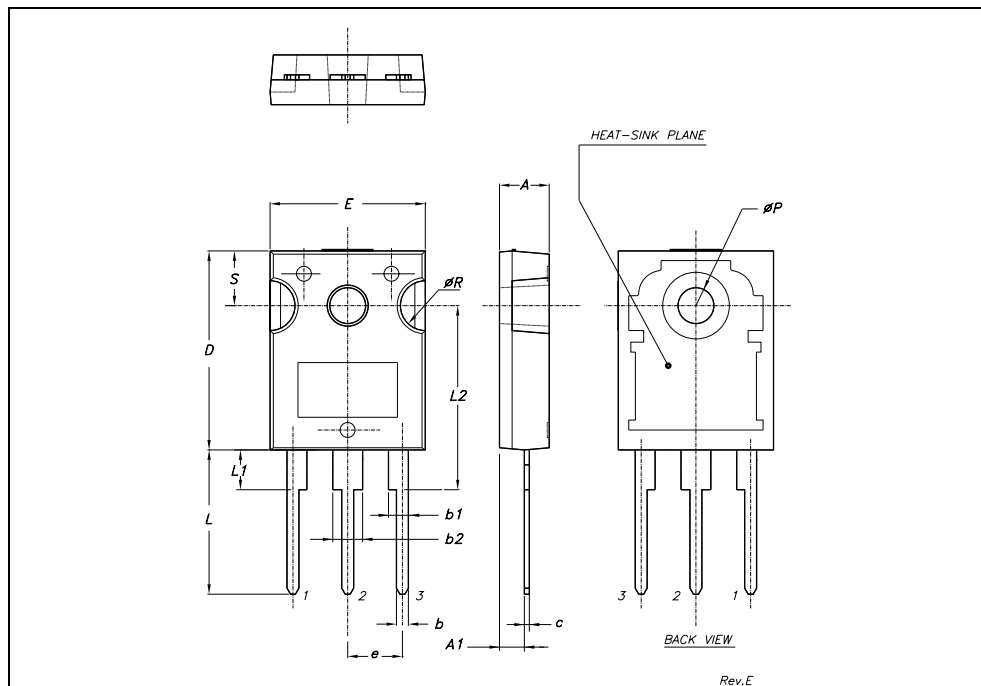
**TO-262 (I<sup>2</sup>PAK) MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
A1	2.40		2.72	0.094		0.107
b	0.61		0.88	0.024		0.034
b1	1.14		1.70	0.044		0.066
c	0.49		0.70	0.019		0.027
c2	1.23		1.32	0.048		0.052
D	8.95		9.35	0.352		0.368
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
E	10		10.40	0.393		0.410
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L2	1.27		1.40	0.050		0.055



**TO-247 MECHANICAL DATA**

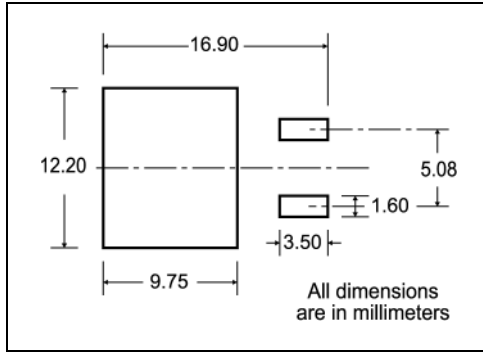
DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.85		5.15	0.19		0.20
A1	2.20		2.60	0.086		0.102
b	1.0		1.40	0.039		0.055
b1	2.0		2.40	0.079		0.094
b2	3.0		3.40	0.118		0.134
c	0.40		0.80	0.015		0.03
D	19.85		20.15	0.781		0.793
E	15.45		15.75	0.608		0.620
e		5.45			0.214	
L	14.20		14.80	0.560		0.582
L1	3.70		4.30	0.14		0.17
L2		18.50			0.728	
øP	3.55		3.65	0.140		0.143
øR	4.50		5.50	0.177		0.216
S		5.50			0.216	





## 5 Packaging mechanical data

### D<sup>2</sup>PAK FOOTPRINT



### TAPE AND REEL SHIPMENT

**TAPE MECHANICAL DATA**

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	10.5	10.7	0.413	0.421
B0	15.7	15.9	0.618	0.626
D	1.5	1.6	0.059	0.063
D1	1.59	1.61	0.062	0.063
E	1.65	1.85	0.065	0.073
F	11.4	11.6	0.449	0.456
K0	4.8	5.0	0.189	0.197
P0	3.9	4.1	0.153	0.161
P1	11.9	12.1	0.468	0.476
P2	1.9	2.1	0.075	0.082
R	50		1.574	
T	0.25	0.35	0.0098	0.0137
W	23.7	24.3	0.933	0.956

**REEL MECHANICAL DATA**

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0.795	
G	24.4	26.4	0.960	1.039
N	100		3.937	
T		30.4		1.197

BASE QTY	BULK QTY
1000	1000

\* on sales type

## 6 Revision history

**Table 9. Revision history**

Date	Revision	Changes
21-Jun-2004	2	Complete version with curves
26-Jul-2006	3	New template, no content change

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