STP16NK65Z
STB16NK65Z-S

N-CHANNEL 650V - 0.38Ω - 13A TO-220 / I²SPAK
Zener - Protected SuperMESH™ MOSFET

Table 1: General Features

TYPE	V_{DSS}	$R_{DS(on)}$	I_D	Pw
STP16NK65Z	650 V	< 0.50 Ω	13 A	190 W
STB16NK65Z-S	650 V	< 0.50 Ω	13 A	190 W

- TYPICAL R_{DS}(on) = 0.38Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- GATE CHARGE MINIMIZED
- VERY LOW INTRINSIC CAPACITANCES
- VERY GOOD MANUFACTURING REPEATIBILITY

DESCRIPTION

The SuperMESH™ series is obtained through an extreme optimization of ST's well established stripbased PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications. Such series complements ST full range of high voltage MOSFETs including revolutionary MDmesh™ products.

APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- IDEAL FOR OFF-LINE POWER SUPPLIES

Figure 1: Package

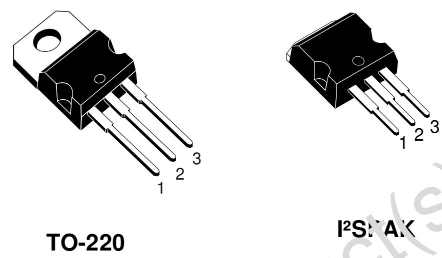


Figure 2: Internal Schematic Diagram

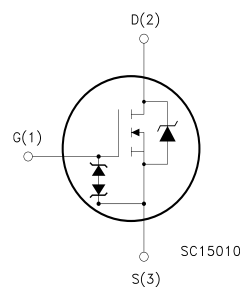


Table 2: Order Codes

SALES TYPE	MARKING	PACKAGE	PACKAGING
STP16NK65Z	P16NK65Z	TO-220	TUBE
STB16NK65Z-S	B16NK65Z	I²SPAK	TUBE

Rev. 3

Table 3: Absolute Maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage (V_{GS} = 0)	650	V
V_{DGR}	Drain-gate Voltage (R_{GS} = 20 kΩ)	650	V
V_{GS}	Gate- source Voltage	± 30	V
I_D	Drain Current (continuous) at T_C = 25°C	13	A
I_D	Drain Current (continuous) at T_C = 100°C	8.19	A
I_{DM} (*)	Drain Current (pulsed)	52	A
P_{TOT}	Total Dissipation at T_C = 25°C	190	W
	Derating Factor	1.51	W/°C
$V_{ESD(G-S)}$	Gate source EDS (HBM-C=100pF, R=1.5kΩ)	6000	V
dv/dt (1)	Peak Diode Recovery voltage slope	4.5	V/ns
T_j T_{stg}	Operating Junction Temperature Storage Temperature	-55 to 150	°C

(*) Pulse width limited by safe operating area
(1) $I_{SD} \leq 13$ A, di/dt ≤ 200 A/µs, $V_{DD} \leq V_{(BR)DSS}$, $T_j \leq T_{JMAX}$

Table 4: Thermal Data

Rthj-case	Thermal Resistance Junction-case Max	0.66	°C/W
Rthj-amb	Thermal Resistance Junction-ambient Max	62.5	°C/W
T_l	Maximum Lead Temperature For Soldering Purpose	300	°C

Table 5: Avalanche Characteristics

Symbol	Parameter	Max. Value	Unit
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max)	13	A
E_{AS}	Single Pulse Avalanche Energy (starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	350	mJ

Table 6: Gate-Source Zener Diode

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
BV_{GSO}	Gate-Source Breakdown Voltage	Igs=± 1mA (Open Drain)	30			V

PROTECTION FEATURES OF GATE-TO-SOURCE ZENER DIODES

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied fromgate to source. In this respect the Zener voltage ia appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

ELECTRICAL CHARACTERISTICS (T_{CASE} =25°C UNLESS OTHERWISE SPECIFIED)

Table 7: On/Off

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D = 1 mA, V_{GS} = 0	650			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating, T_C = 125 °C			1 50	µA µA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS} = ± 20 V			±10	µA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 100 µA	3	3.75	4.5	V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS} = 10V, I_D = 6.5 A		0.38	0.50	Ω

Table 8: Dynamic

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward Transconductance	V_{DS} = 15 V, I_D = 6.5 A		12		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0		2750 275 60		pF pF pF
$C_{oss\ eq.}$ (*)	Equivalent Output Capacitance	V_{GS} = 0V, V_{DS} = 6.5 V to 520 V		188		pF
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on Delay Time Rise Time Turn-off Delay Time Fall Time	V_{DD} = 325 V, I_D = 6.5 A R_G = 4.7Ω V_{GS} = 10 V (see Figure 17)		25 25 68 17		ns ns ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V_{DD} = 520 V, I_D = 13 A, V_{GS} = 10 V (see Figure 20)		89 18 45		nC nC nC

Table 9: Source Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (2)	Source-drain Current Source-drain Current (pulsed)				13 52	A A
V_{SD} (1)	Forward On Voltage	I_{SD} = 13 A, V_{GS} = 0			1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD} = 13 A, di/dt = 100 A/µs, V_{DD} = 100 V, T_j = 25°C (see Figure 18)		500 5.2 21		ns µC A
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD} = 13 A, di/dt = 100 A/µs, V_{DD} = 100 V, T_j = 150°C (see Figure 18)		615 7 22.5		ns µC A

(1) Pulsed: Pulse duration = 300µs, duty cycle 1.5%
(2) Pulse width limited by safe operating area
(*) $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Figure 3: Safe Operating Area

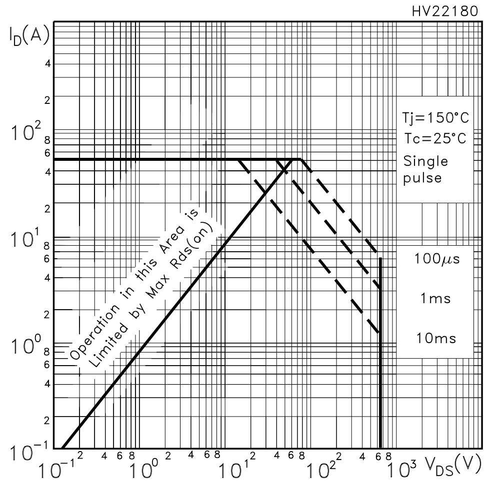


Figure 6: Thermal Impedance

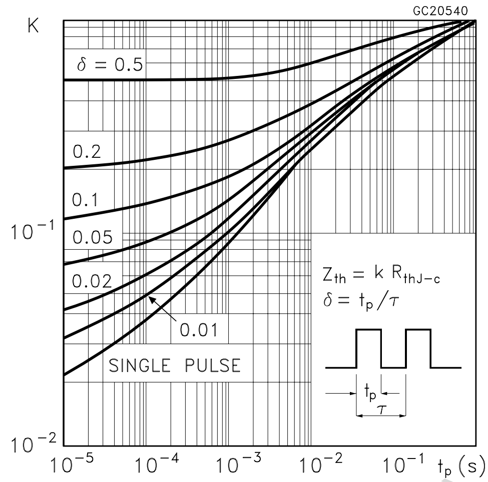


Figure 4: Output Characteristics

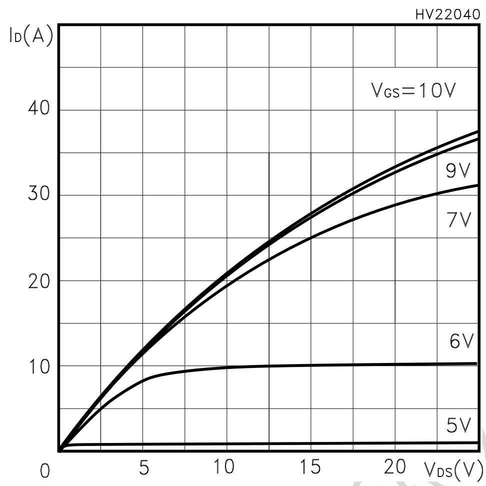


Figure 7: Transfer Characteristics

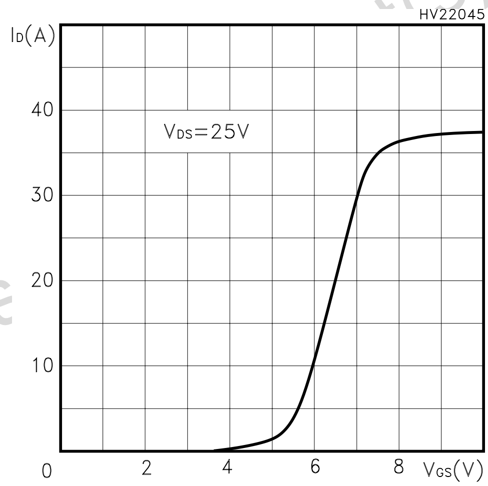


Figure 5: Transconductance

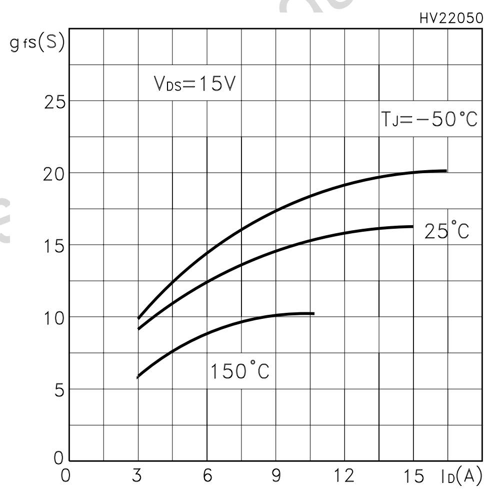


Figure 8: Static Drain-source On Resistance

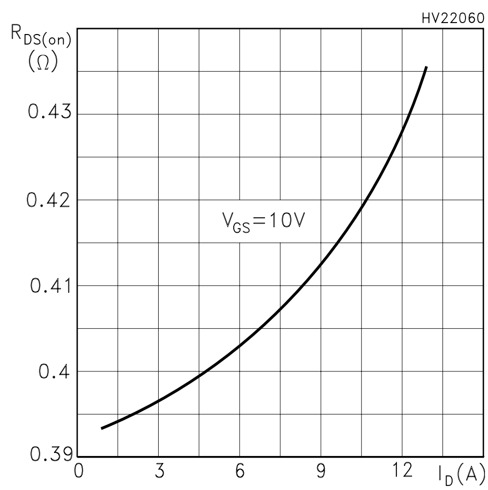


Figure 9: Gate Charge vs Gate-source Voltage

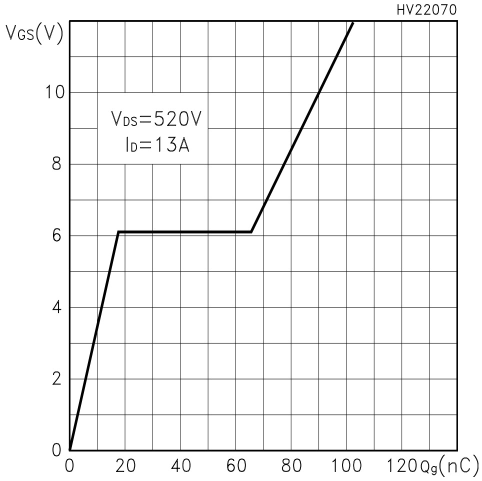


Figure 10: Normalized Gate Thereshold Voltage vs Temperature

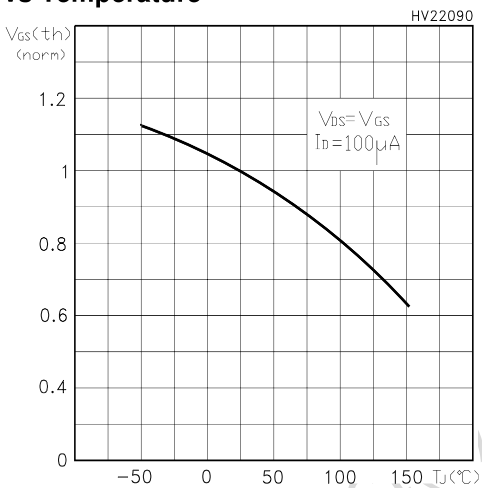


Figure 11: Dource-Drain Diode Forward Characteristics

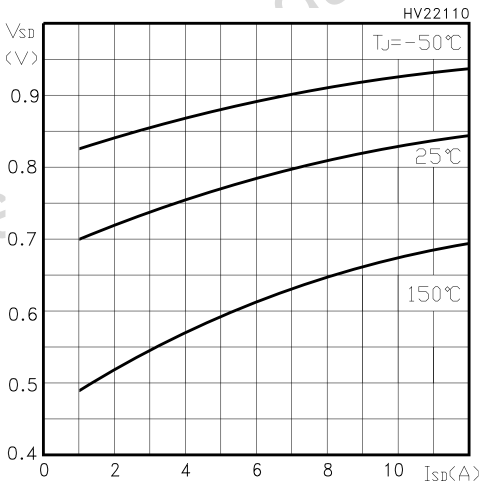


Figure 12: Capacitance Variations

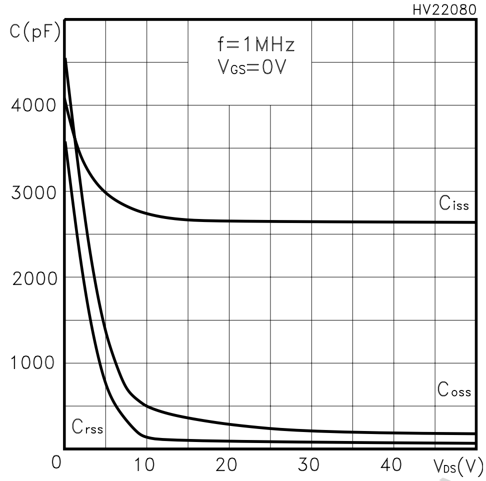


Figure 13: Normalized On Resistance vs Temperature

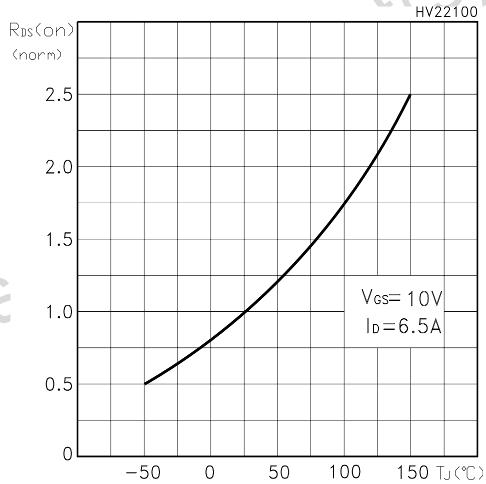


Figure 14: Normalized BVdss vs Temperature

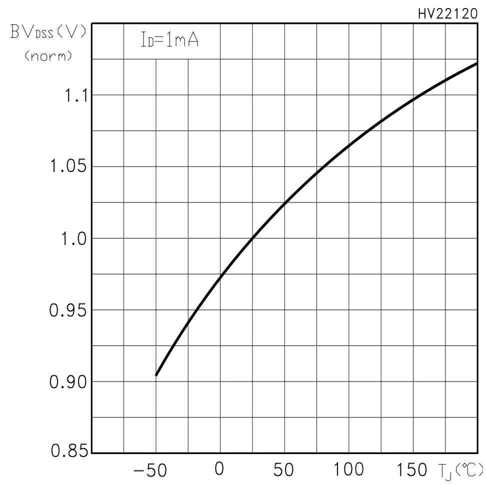


Figure 15: Avalanche Energy vs Starting Tj
j

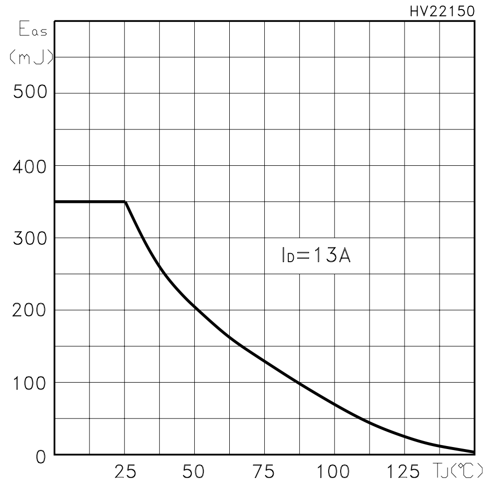


Figure 16: Unclamped Inductive Load Test Circuit

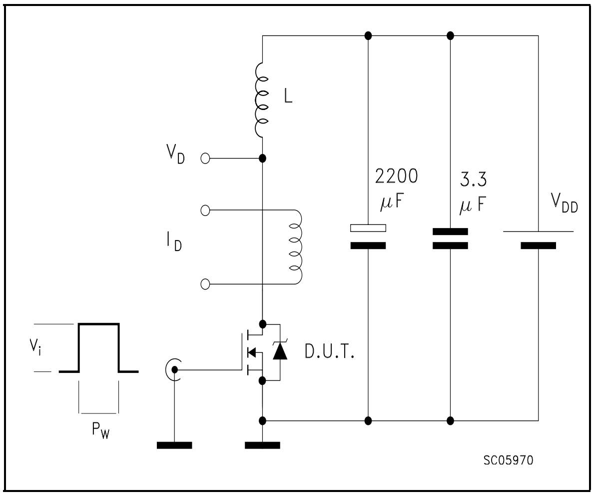


Figure 17: Switching Times Test Circuit For Resistive Load

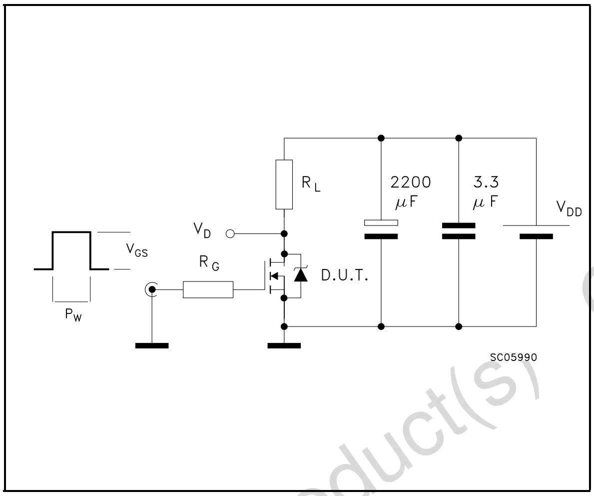


Figure 18: Test Circuit For Inductive Load Switching and Diode Recovery Times

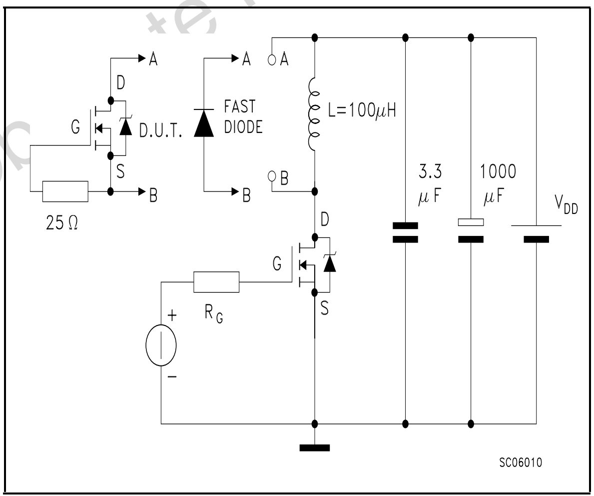


Figure 19: Unclamped Inductive Wafeform

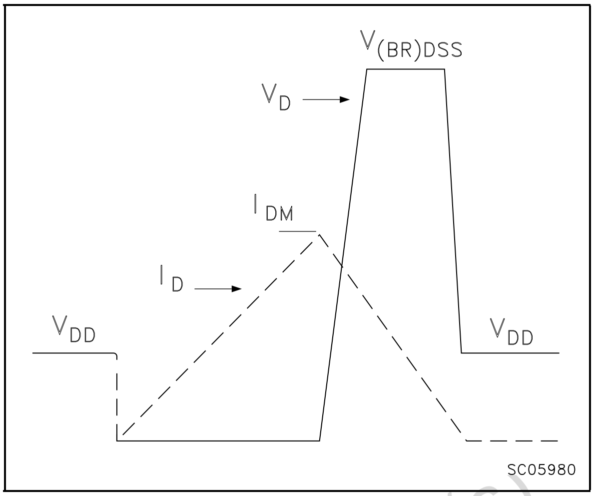
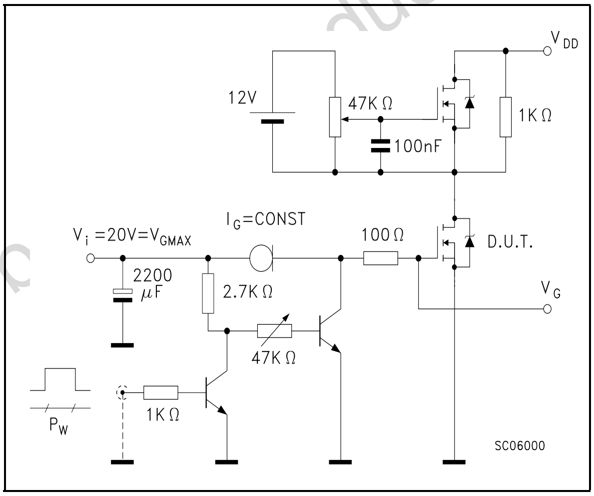


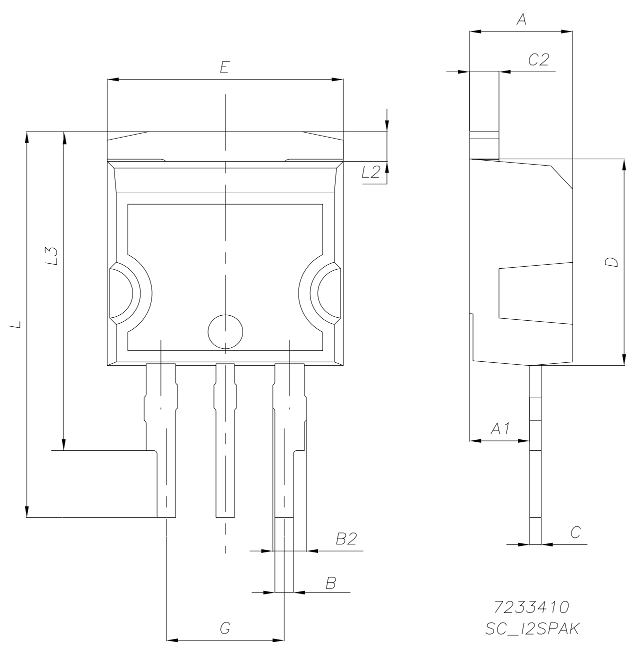
Figure 20: Gate Charge Test Circuit



In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

I^2SPAK MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
A1	2.49		2.69	0.098		0.106
B	0.70		0.93	0.027		0.037
B2	1.14		1.70	0.045		0.067
C	0.45		0.60	0.018		0.024
C2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
E	10.00		10.40	0.394		0.409
G	4.88		5.28	0.192		0.208
L	16.7		17.5	0.657		0.689
L2	1.27		1.4	0.05		0.055
L3	13.82		14.42	0.544		0.568



TO-220 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.15		1.70	0.045		0.066
c	0.49		0.70	0.019		0.027
D	15.25		15.75	0.60		0.620
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.052
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
øP	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116

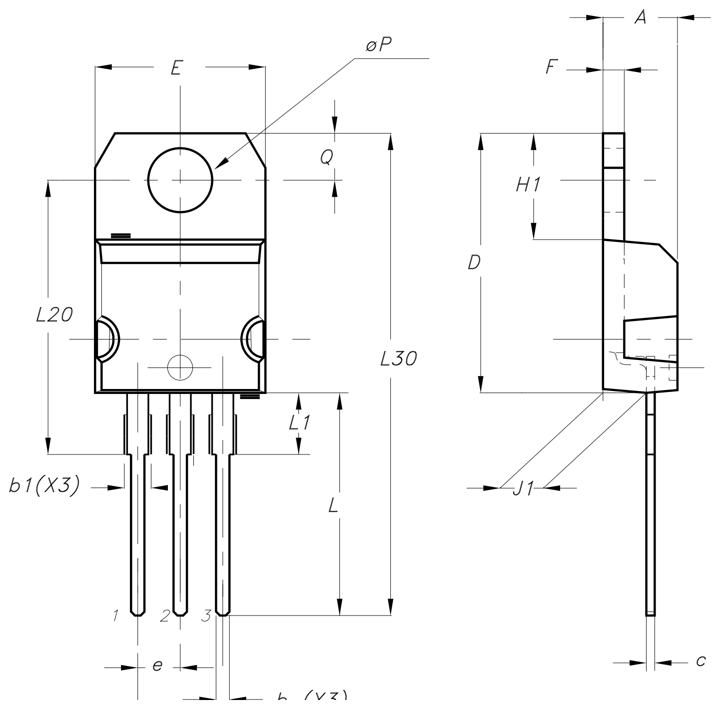


Table 10: Revision History

Date	Revision	Description of Changes
06-Aug-2004	1	First Release.
02-Sep-2004	2	Complete Version
06-Sep-2005	3	Inserted Ecopack indication