



# STB21N65M5, STF21N65M5 STI21N65M5, STP21N65M5, STW21N65M5

N-channel 650 V, 0.150  $\Omega$ , 17 A MDmesh™ V Power MOSFET  
D<sup>2</sup>PAK, TO-220FP, TO-220, I<sup>2</sup>PAK, TO-247

## Features

Order codes	V <sub>DSS</sub> @ T <sub>Jmax</sub>	R <sub>DS(on)</sub> max	I <sub>D</sub>	P <sub>W</sub>
STB21N65M5	710 V	< 0.179 $\Omega$	17 A	125 W
STF21N65M5			17 A <sup>(1)</sup>	30 W
STI21N65M5			17 A	125 W
STP21N65M5				
STW21N65M5				

1. Limited only by maximum temperature allowed

- Worldwide best R<sub>DS(on)</sub> \* area
- Higher V<sub>DSS</sub> rating
- High dv/dt capability
- Excellent switching performance
- 100% avalanche tested

## Application

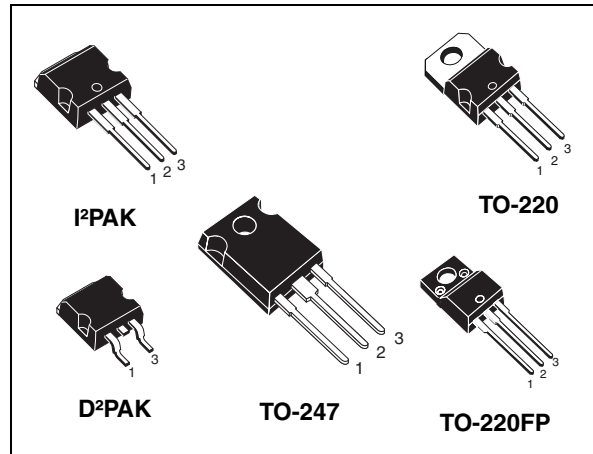
Switching applications

## Description

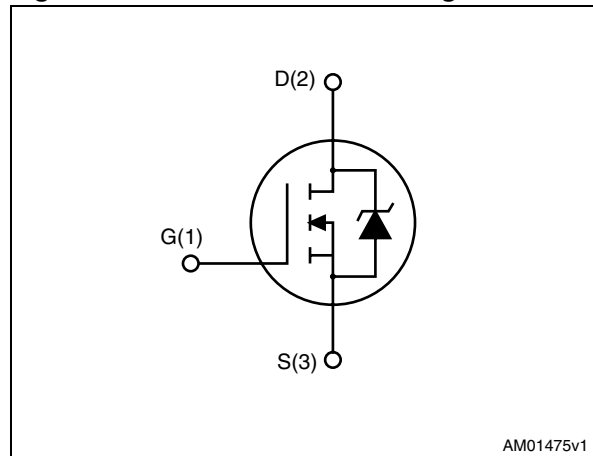
These devices are N-channel MDmesh™ V Power MOSFETs based on an innovative proprietary vertical process technology, which is combined with STMicroelectronics' well-known PowerMESH™ horizontal layout structure. The resulting product has extremely low on-resistance, which is unmatched among silicon-based Power MOSFETs, making it especially suitable for applications which require superior power density and outstanding efficiency.

**Table 1. Device summary**

Order codes	Marking	Package	Packaging
STB21N65M5	21N65M5	D <sup>2</sup> PAK	Tape and reel
STF21N65M5		TO-220FP	Tube
STI21N65M5		I <sup>2</sup> PAK	Tube
STP21N65M5		TO-220	Tube
STW21N65M5		TO-247	Tube



**Figure 1. Internal schematic diagram**



AM01475v1

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value		Unit
		TO-220, I <sup>2</sup> PAK, D <sup>2</sup> PAK, TO-247	TO-220FP	
V <sub>GS</sub>	Gate-source voltage	± 25		V
I <sub>D</sub>	Drain current (continuous) at T <sub>C</sub> = 25 °C	17	17 <sup>(1)</sup>	A
I <sub>D</sub>	Drain current (continuous) at T <sub>C</sub> = 100 °C	10.7	10.7 <sup>(1)</sup>	A
I <sub>DM</sub> <sup>(2)</sup>	Drain current (pulsed)	68	68 <sup>(1)</sup>	A
P <sub>TOT</sub>	Total dissipation at T <sub>C</sub> = 25 °C	125	30	W
I <sub>AR</sub>	Avalanche current, repetitive or not-repetitive (pulse width limited by T <sub>j</sub> max)	5		A
E <sub>AS</sub>	Single pulse avalanche energy (starting T <sub>j</sub> = 25 °C, I <sub>D</sub> = I <sub>AR</sub> , V <sub>DD</sub> = 50 V)	400		mJ
dv/dt <sup>(3)</sup>	Peak diode recovery voltage slope	15		V/ns
V <sub>ISO</sub>	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s; T <sub>C</sub> = 25 °C)	2500		V
T <sub>stg</sub>	Storage temperature	- 55 to 150		°C
T <sub>j</sub>	Max. operating junction temperature	150		°C

1. Limited only by maximum temperature allowed.
2. Pulse width limited by safe operating area.
3. I<sub>SD</sub> ≤ 17 A, di/dt ≤ 400 A/μs; V<sub>Peak</sub> < V<sub>(BR)DSS</sub>; V<sub>DD</sub> = 400 V.

**Table 3. Thermal data**

Symbol	Parameter	Value					Unit
		D <sup>2</sup> PAK	I <sup>2</sup> PAK	TO-220	TO-247	TO-220FP	
R <sub>thj-case</sub>	Thermal resistance junction-case max	1			4.17	°C/W	
R <sub>thj-amb</sub>	Thermal resistance junction-ambient max		62.5	50	62.5	°C/W	
R <sub>thj-pcb</sub>	Thermal resistance junction-pcb max	30				°C/W	
T <sub>l</sub>	Maximum lead temperature for soldering purpose	300				°C	

## 2 Electrical characteristics

( $T_C = 25\text{ °C}$  unless otherwise specified)

**Table 4. On /off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}, V_{GS} = 0$	650			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = \text{Max rating}$ $V_{DS} = \text{Max rating}, T_C = 125\text{ °C}$			1 100	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate-body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 25\text{ V}$			100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}, I_D = 8.5\text{ A}$		0.150	0.179	$\Omega$

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 100\text{ V}, f = 1\text{ MHz},$ $V_{GS} = 0$	-	1950	-	pF
$C_{oss}$	Output capacitance			46		
$C_{rss}$	Reverse transfer capacitance			3		
$C_{o(tr)}^{(1)}$	Equivalent capacitance time related	$V_{DS} = 0\text{ to }520\text{ V}, V_{GS} = 0$	-	133	-	pF
$C_{o(er)}^{(2)}$	Equivalent capacitance energy related			44		
$R_G$	Intrinsic gate resistance	$f = 1\text{ MHz open drain}$	-	2.5	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 520\text{ V}, I_D = 8.5\text{ A},$ $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 20</a> )	-	50	-	nC
$Q_{gs}$	Gate-source charge			13		
$Q_{gd}$	Gate-drain charge			23		

1.  $C_{oss\text{ eq.}}$  time related is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$ .

2.  $C_{oss\text{ eq.}}$  energy related is defined as a constant equivalent capacitance giving the same stored energy as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$ .

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_d$ (v)	Voltage delay time	$V_{DD} = 400\text{ V}$ , $I_D = 11\text{ A}$ ,		37		ns
$t_r$ (v)	Voltage rise time	$R_G = 4.7\ \Omega$ , $V_{GS} = 10\text{ V}$		10		ns
$t_f$ (i)	Current fall time	(see <a href="#">Figure 21</a> )	-	12	-	ns
$t_c$ (off)	Crossing time	(see <a href="#">Figure 24</a> )		24		ns

**Table 7. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current				17	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		68	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 17\text{ A}$ , $V_{GS} = 0$	-		1.5	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 17\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$		294		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 100\text{ V}$ (see <a href="#">Figure 21</a> )	-	4		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current			28		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 17\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$		340		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 100\text{ V}$ , $T_j = 150\text{ }^\circ\text{C}$	-	5		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current	(see <a href="#">Figure 21</a> )		29		A

1. Pulse width limited by safe operating area.

2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for TO-220, D<sup>2</sup>PAK, I<sup>2</sup>PAK

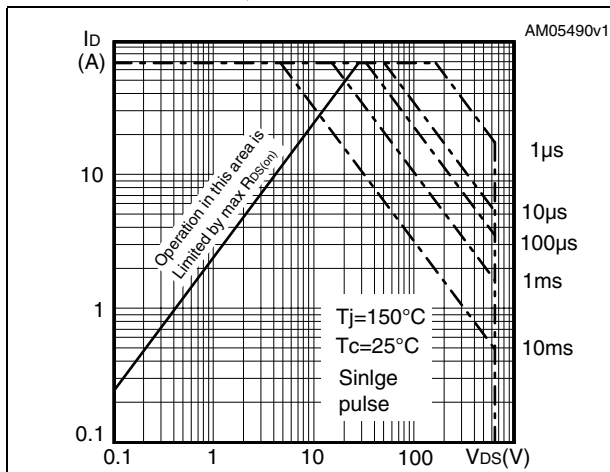


Figure 3. Thermal impedance for TO-220, D<sup>2</sup>PAK, I<sup>2</sup>PAK

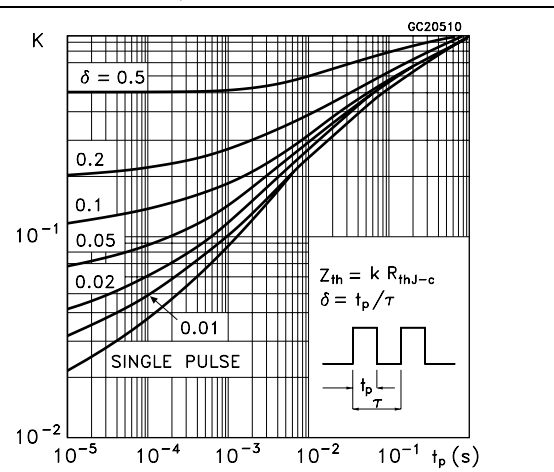


Figure 4. Safe operating area for TO-220FP

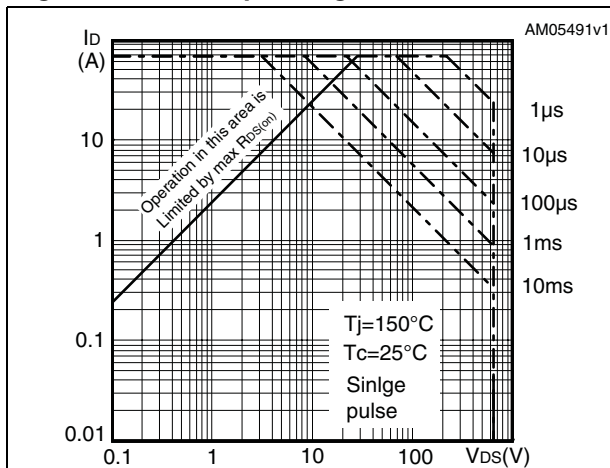


Figure 5. Thermal impedance for TO-220FP

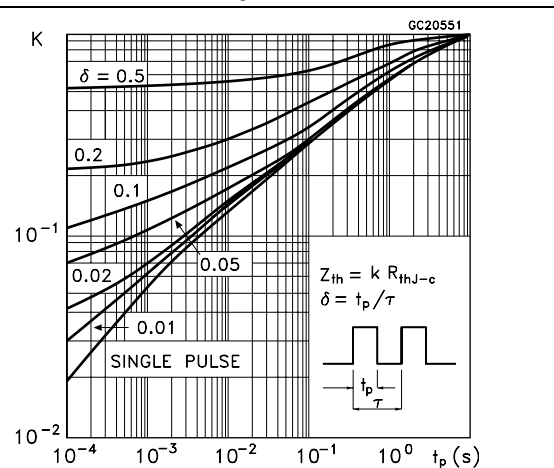


Figure 6. Safe operating area for TO-247

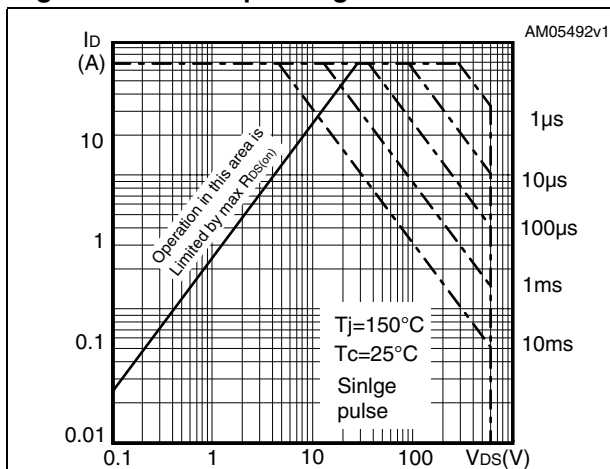


Figure 7. Thermal impedance for TO-247

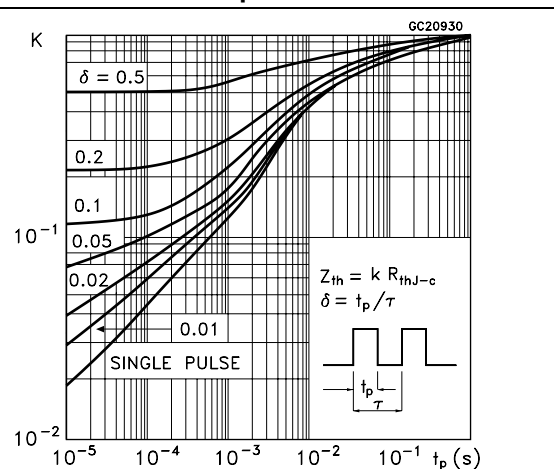


Figure 8. Output characteristics

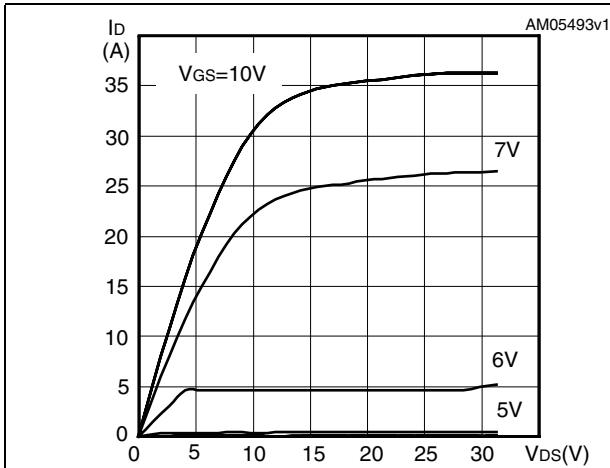


Figure 9. Transfer characteristics

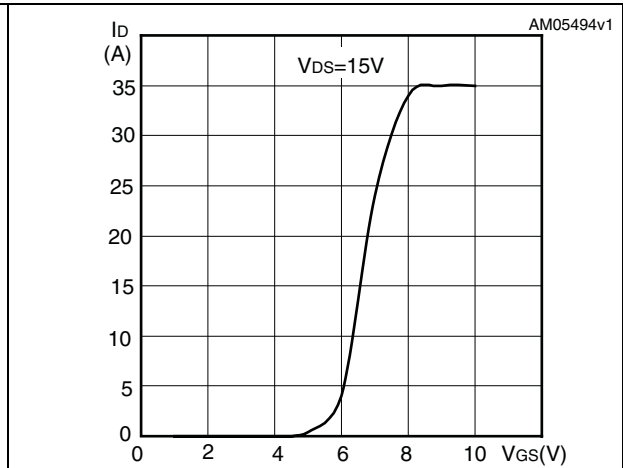


Figure 10. Gate charge vs gate-source voltage

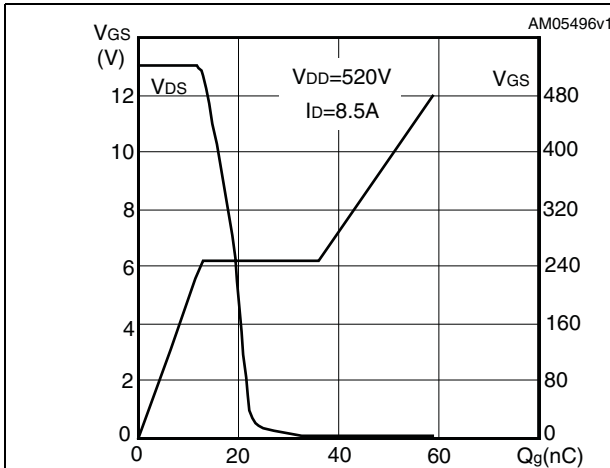


Figure 11. Static drain-source on resistance

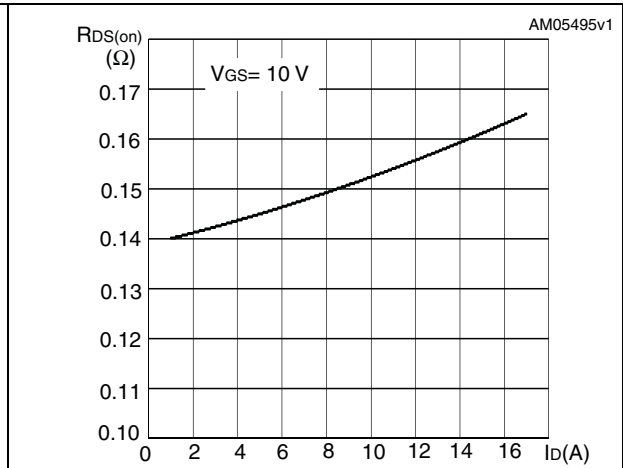


Figure 12. Capacitance variations

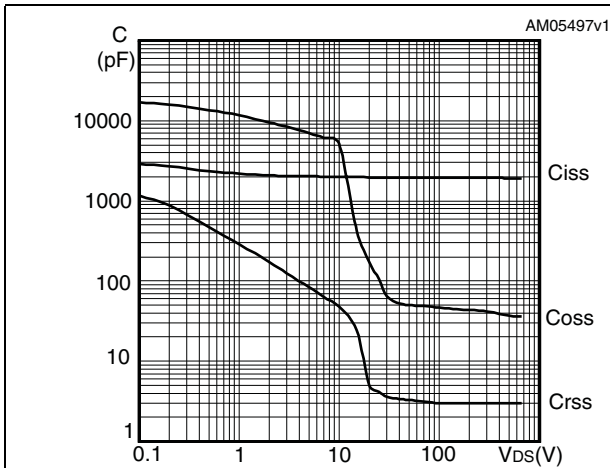


Figure 13. Output capacitance stored energy

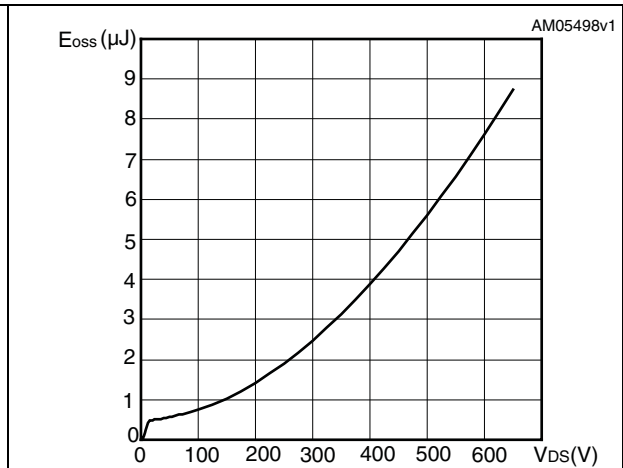


Figure 14. Normalized gate threshold voltage vs temperature

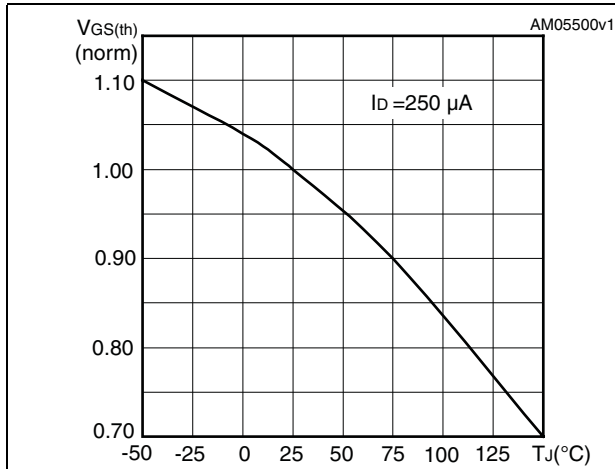


Figure 15. Normalized on resistance vs temperature

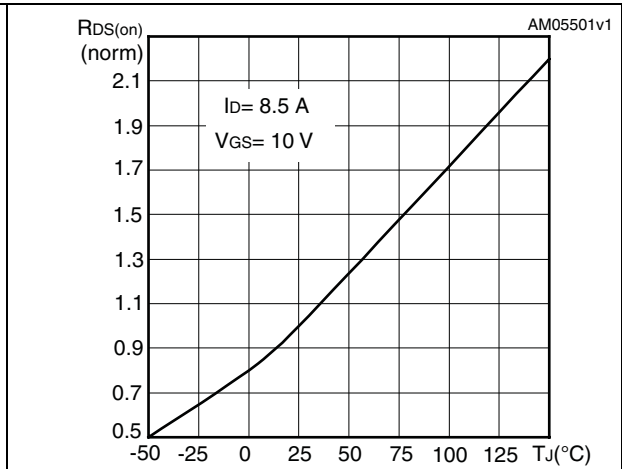


Figure 16. Source-drain diode forward characteristics

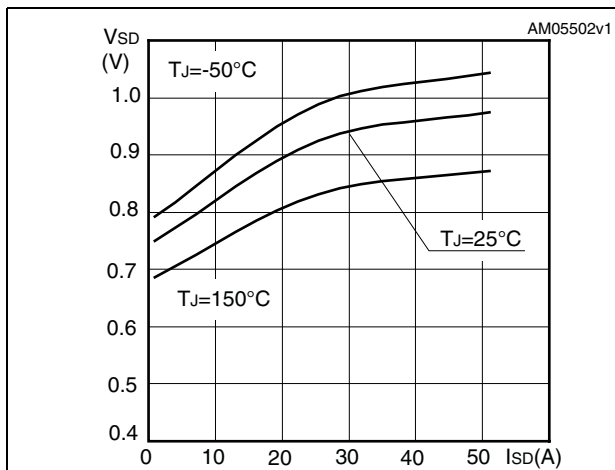


Figure 17. Normalized BV<sub>DSS</sub> vs temperature

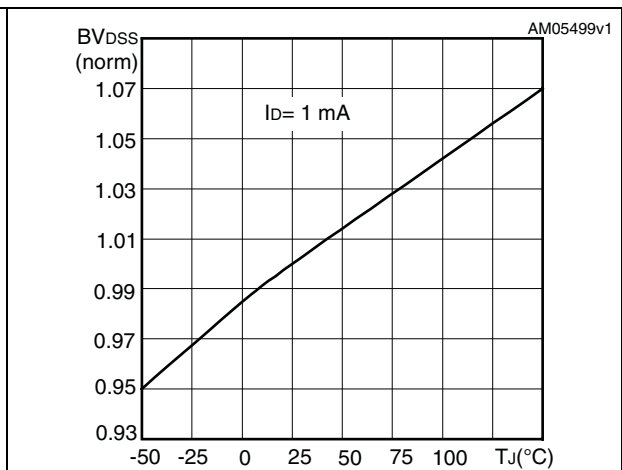
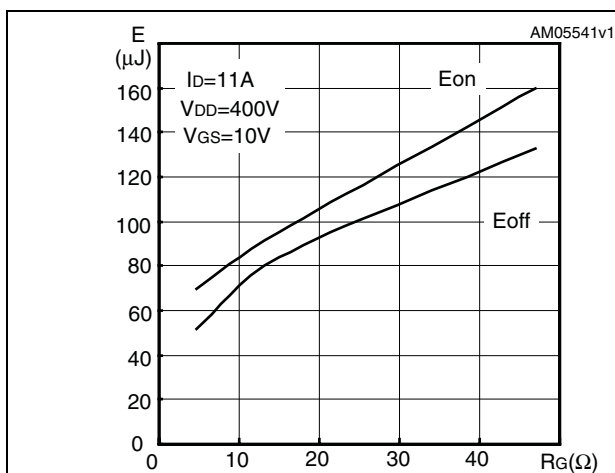


Figure 18. Switching losses vs gate resistance (1)

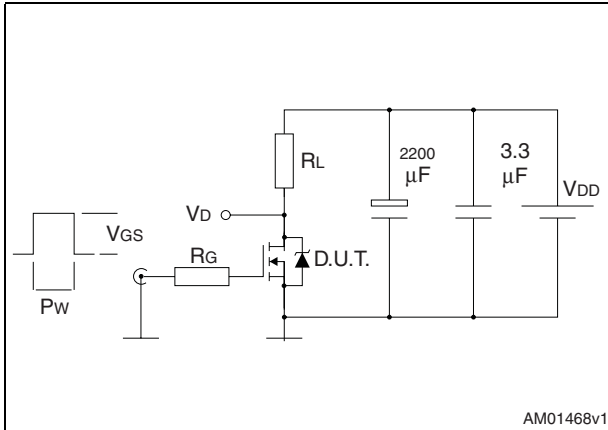


1. Eon including reverse recovery of a SiC diode.

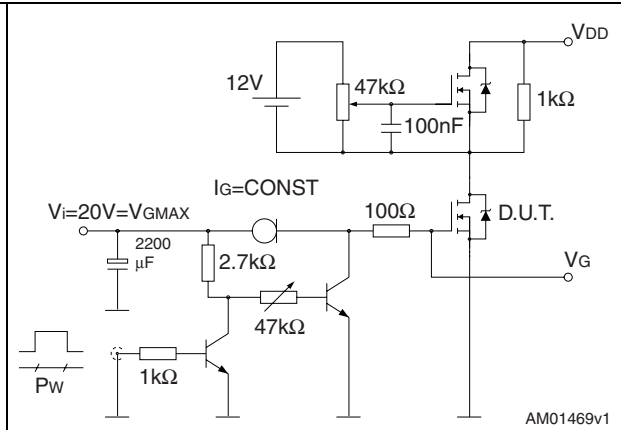


### 3 Test circuits

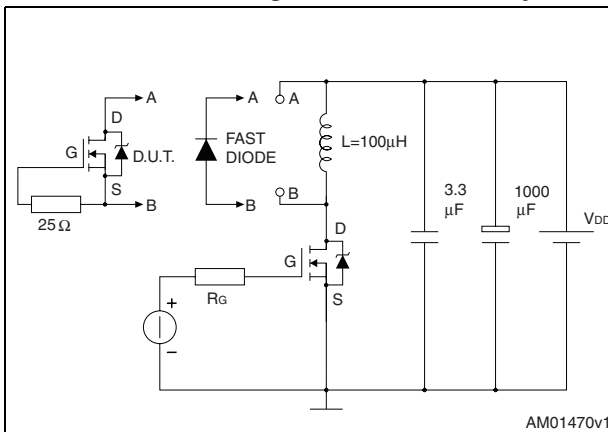
**Figure 19. Switching times test circuit for resistive load**



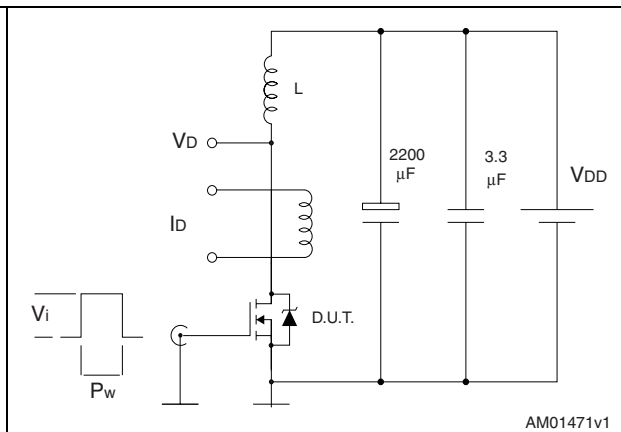
**Figure 20. Gate charge test circuit**



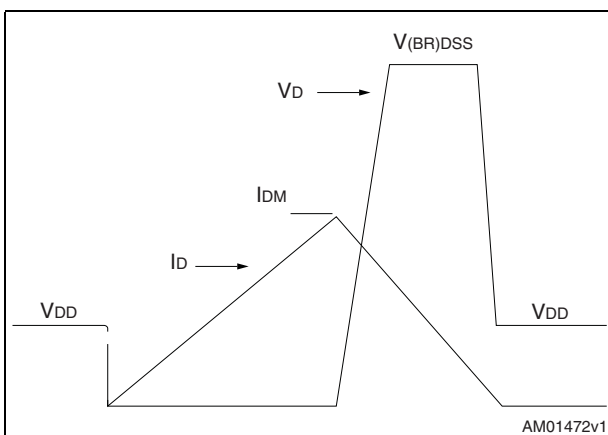
**Figure 21. Test circuit for inductive load switching and diode recovery times**



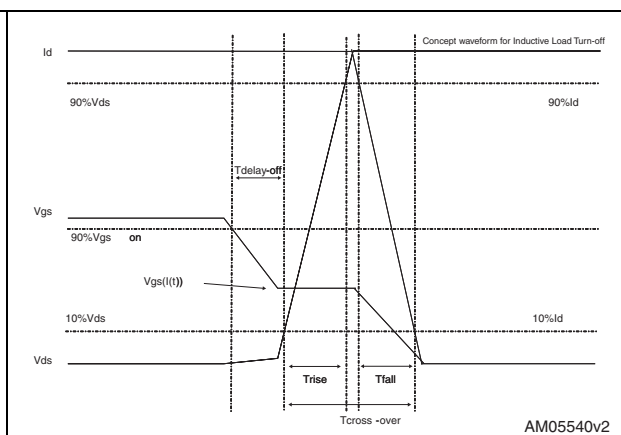
**Figure 22. Unclamped inductive load test circuit**



**Figure 23. Unclamped inductive waveform**



**Figure 24. Switching time waveform**



## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

Table 8. TO-220FP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

Figure 25. TO-220FP drawing mechanical data

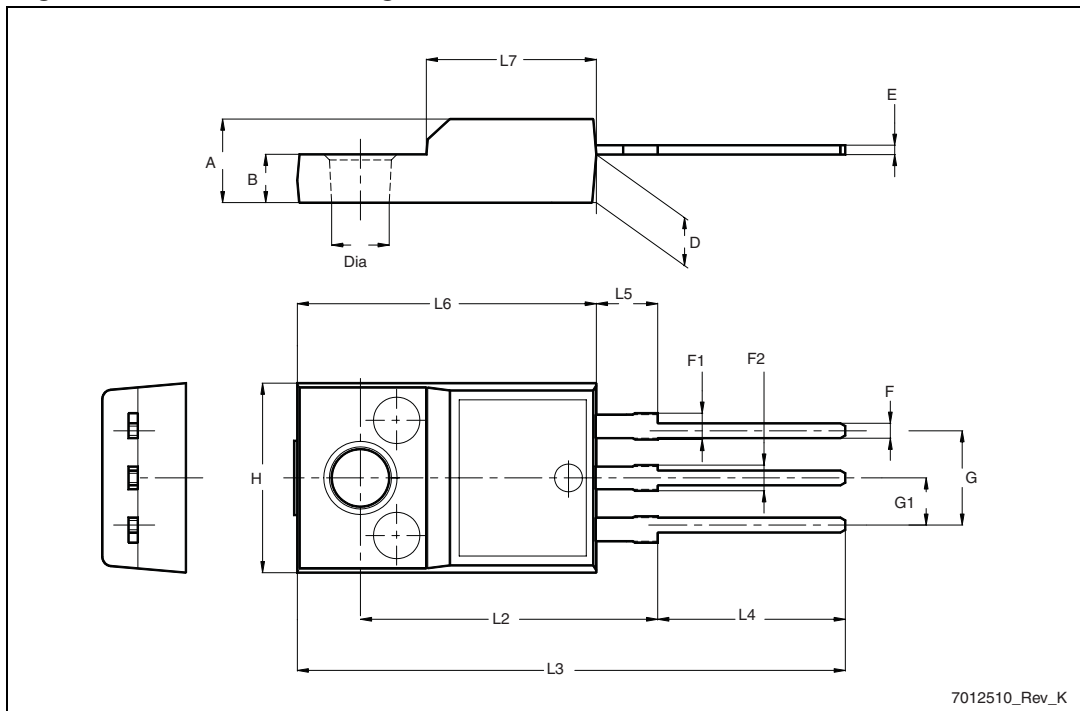
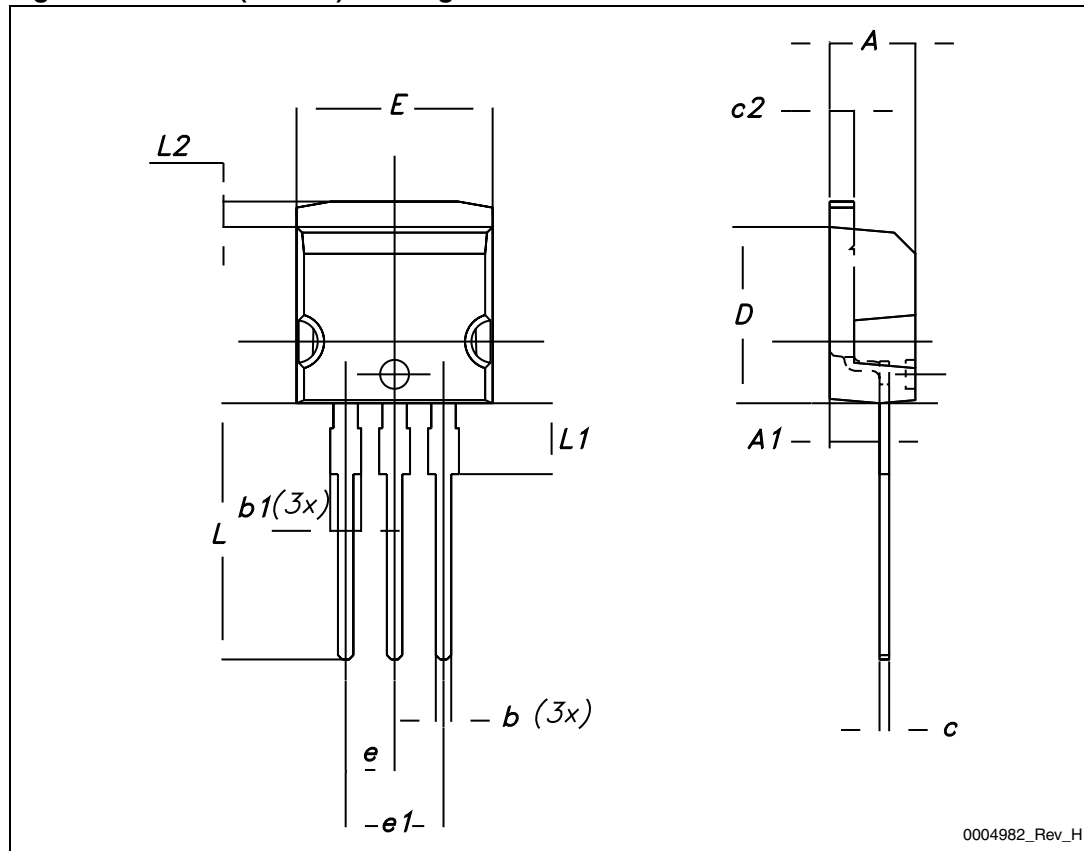


Table 9. I<sup>2</sup>PAK (TO-262) mechanical data

DIM.	mm.		
	min.	typ	max.
A	4.40		4.60
A1	2.40		2.72
b	0.61		0.88
b1	1.14		1.70
c	0.49		0.70
c2	1.23		1.32
D	8.95		9.35
e	2.40		2.70
e1	4.95		5.15
E	10		10.40
L	13		14
L1	3.50		3.93
L2	1.27		1.40

Figure 26. I<sup>2</sup>PAK (TO-262) drawing



0004982\_Rev\_H

Table 10. TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
ØP	3.75		3.85
Q	2.65		2.95

Figure 27. TO-220 type A drawing

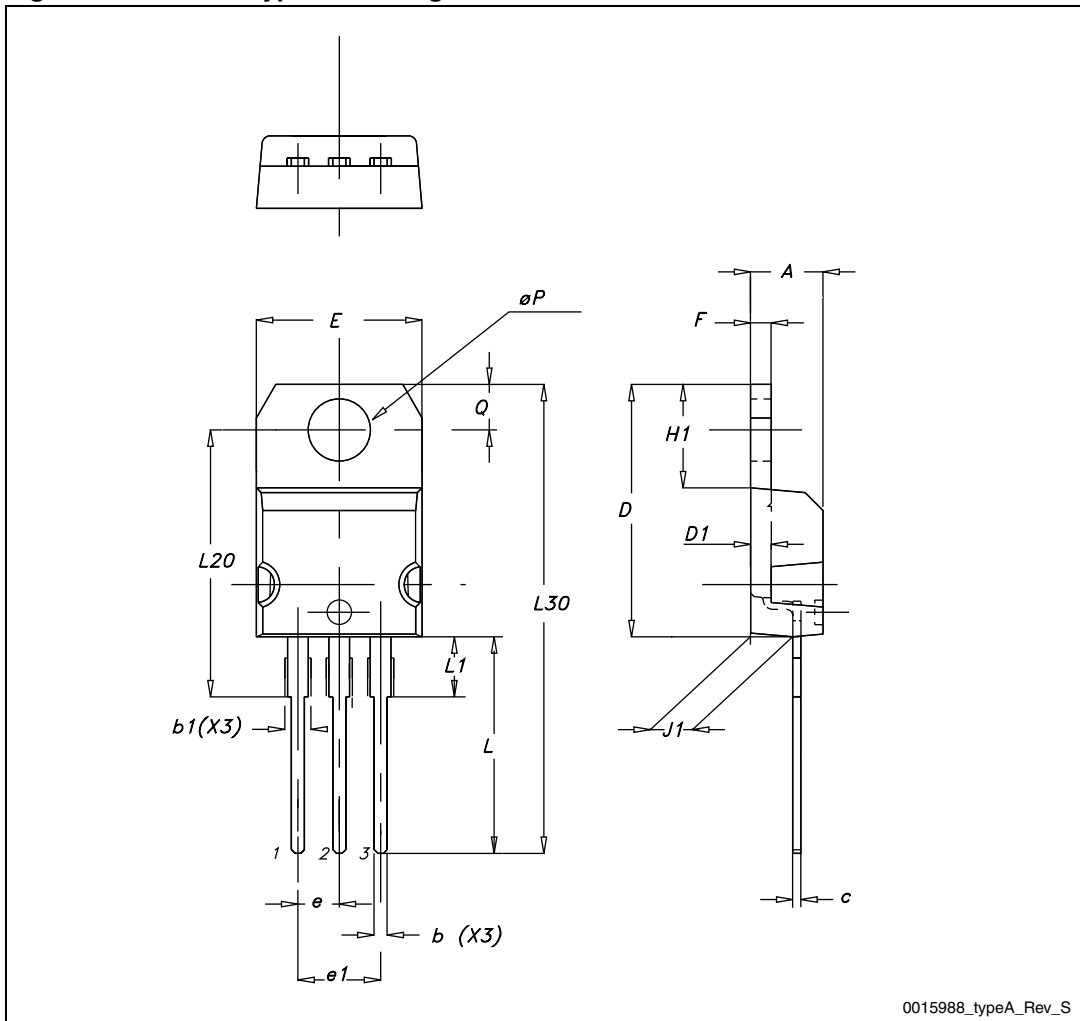
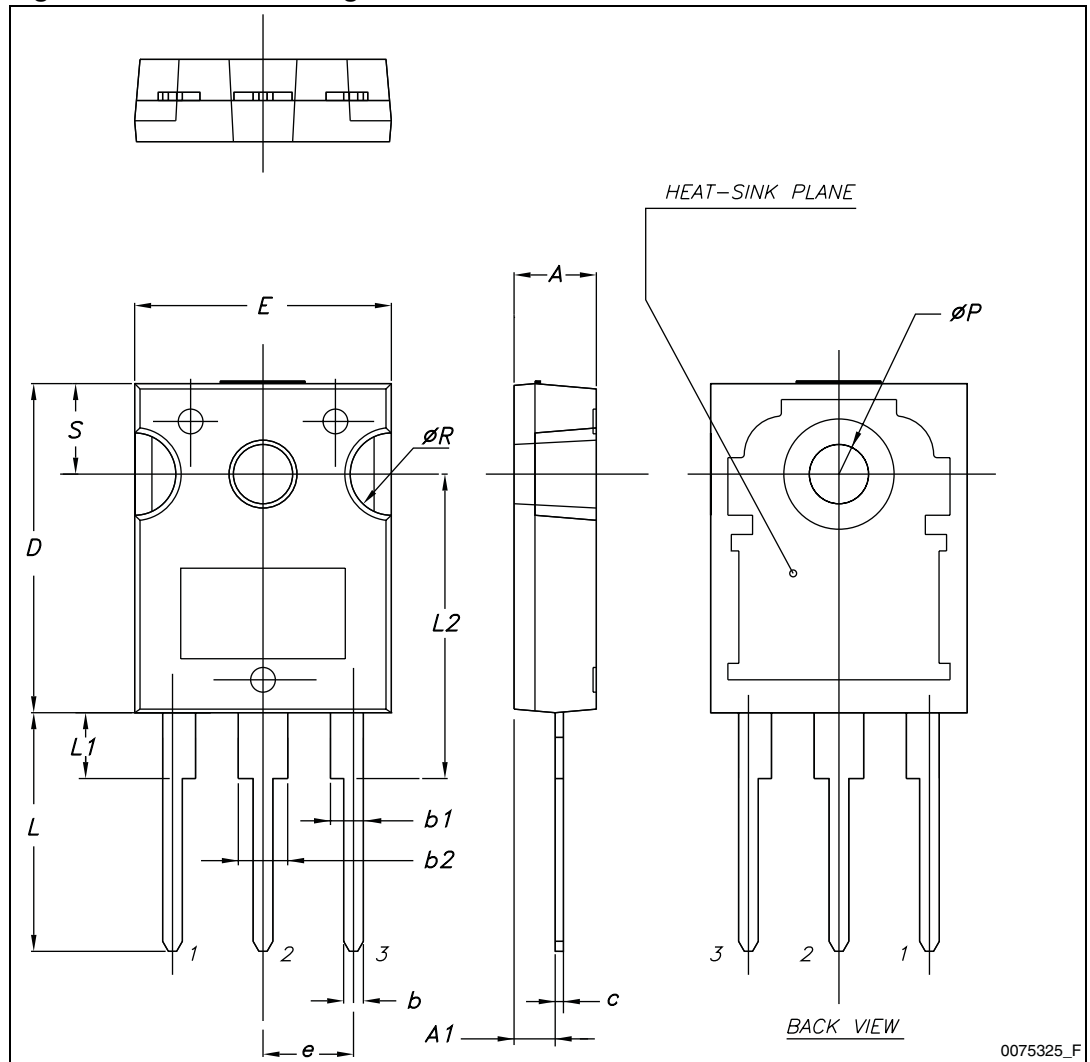


Table 11. TO-247 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e		5.45	
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S		5.50	

Figure 28. TO-247 drawing



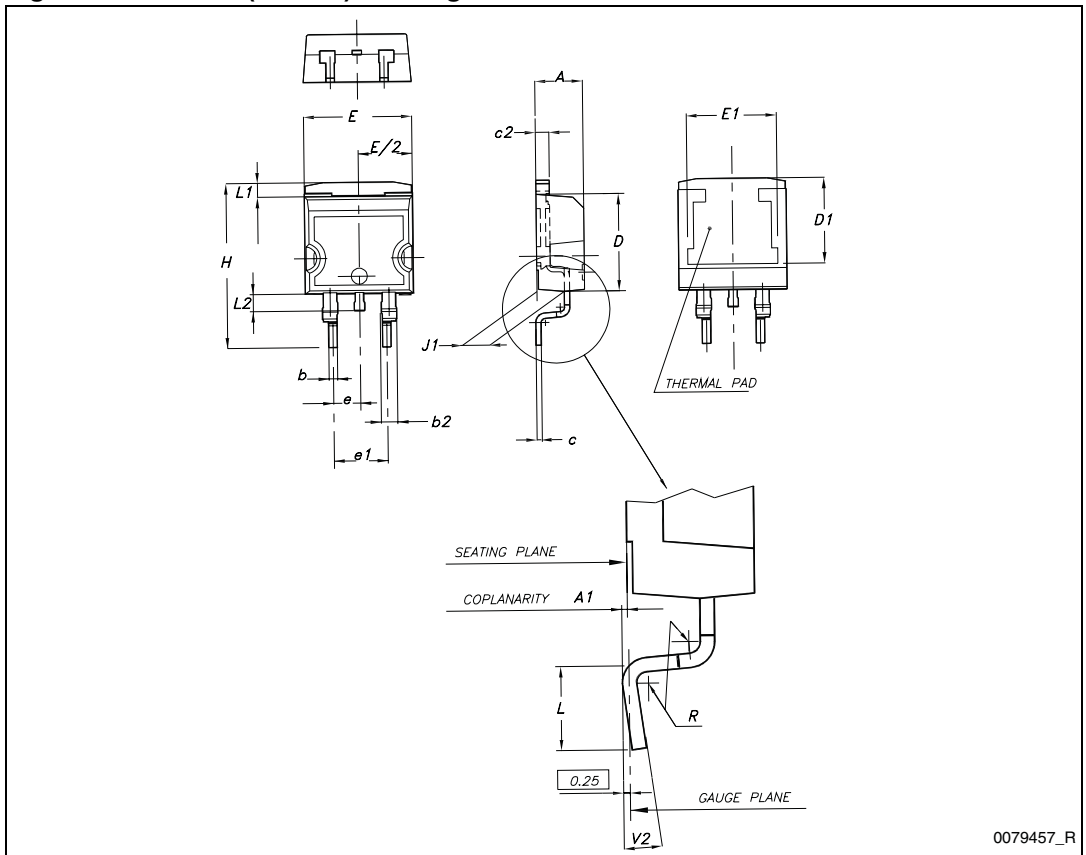
0075325\_F



Table 12. D<sup>2</sup>PAK (TO-263) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50		
E	10		10.40
E1	8.50		
e		2.54	
e1	4.88		5.28
H	15		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.4	
V2	0°		8°

Figure 29. D<sup>2</sup>PAK (TO-263) drawing

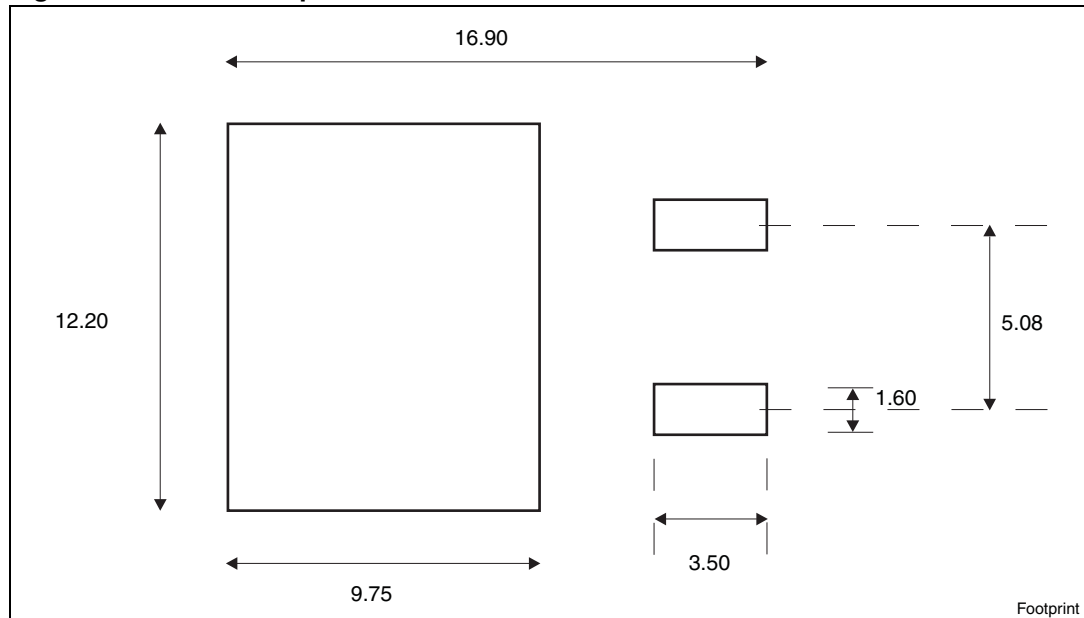


## 5 Packaging mechanical data

Table 13. D<sup>2</sup>PAK (TO-263) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base qty		1000
P2	1.9	2.1	Bulk qty		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

Figure 30. D<sup>2</sup>PAK footprint<sup>(a)</sup>



a. All dimension are in millimeters

Figure 31. Tape

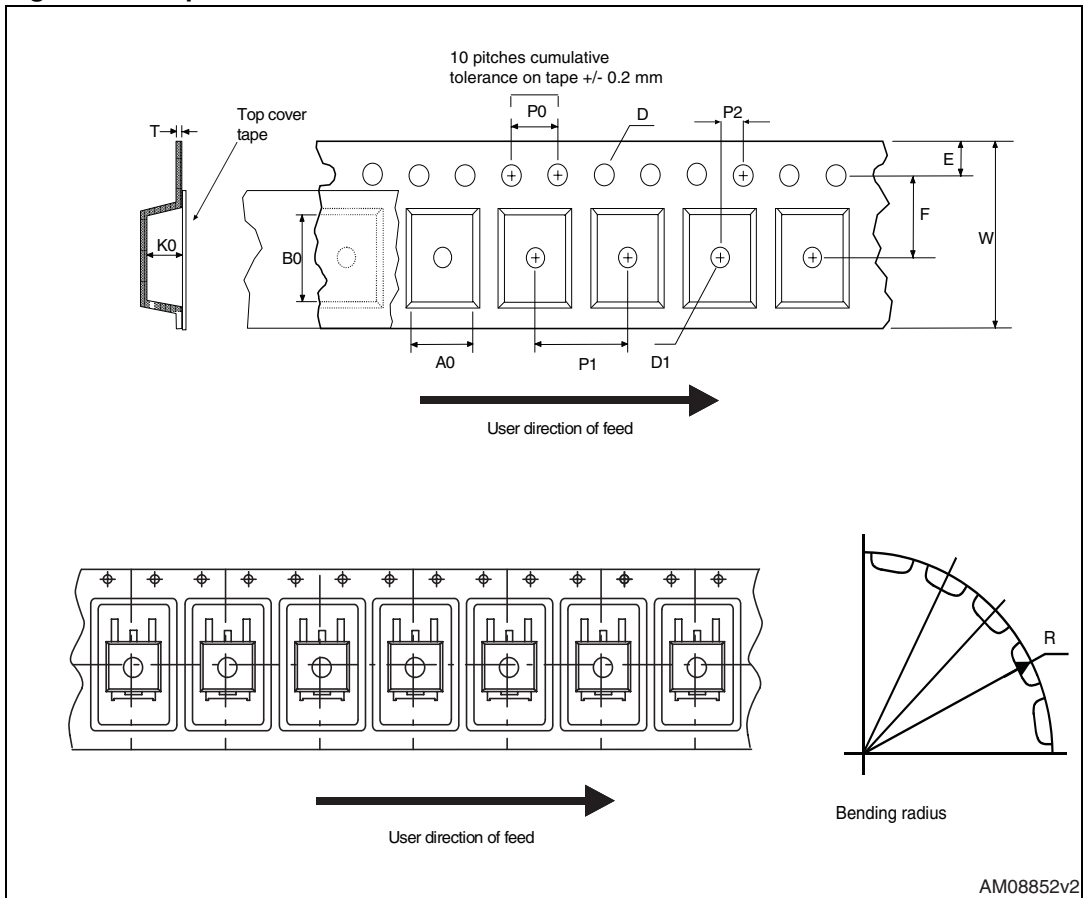
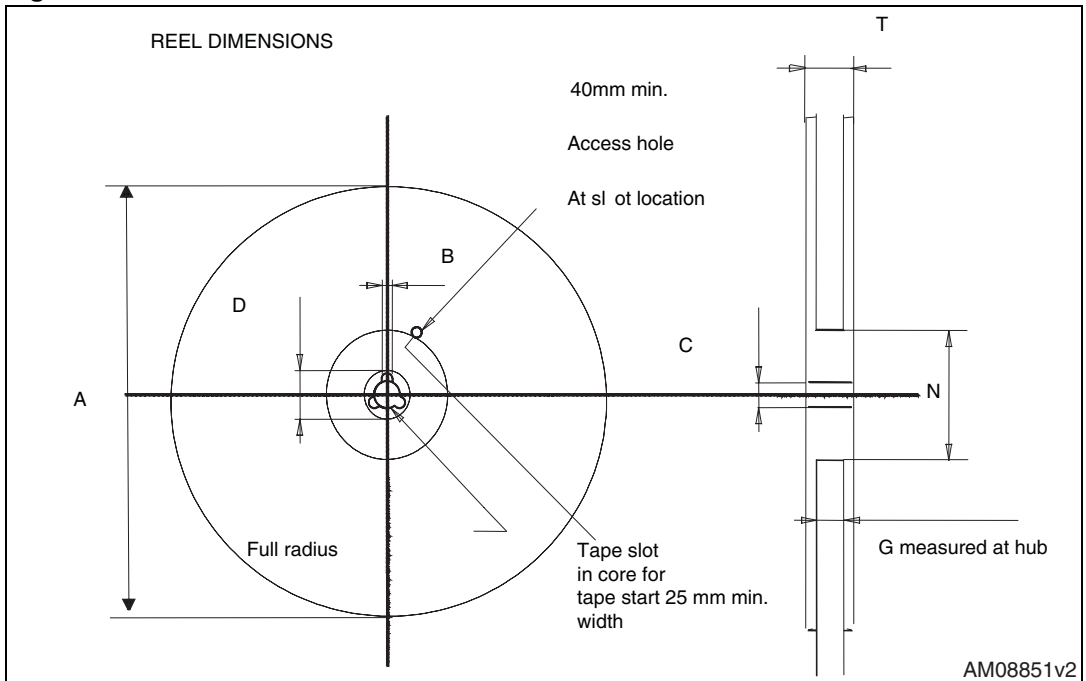


Figure 32. Reel



## 6 Revision history

**Table 14. Document revision history**

Date	Revision	Changes
24-Feb-2009	1	First release
27-Feb-2009	2	Corrected package information on first page.
11-Nov-2009	3	Document status promoted from preliminary data to datasheet.
11-May-2011	4	$R_{DS(on)}$ values have been updated (see <a href="#">Table 4: On /off states</a> and <a href="#">Figure 11: Static drain-source on resistance</a> ).

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