



# STP40NF10

N-channel 100 V, 0.025  $\Omega$ , 50 A TO-220  
low gate charge STripFET™ II Power MOSFET

## Features

Order code	V <sub>DSS</sub>	R <sub>DS(on)</sub> max.	I <sub>D</sub>
STP40NF10	100 V	< 0.028 $\Omega$	50 A

- Exceptional dv/dt capability
- Low gate charge
- 100% avalanche tested

## Application

Switching applications

## Description

This N-channel 100 V Power MOSFET is the latest development of STMicroelectronics unique "single feature size" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps allowing remarkable manufacturing reproducibility.

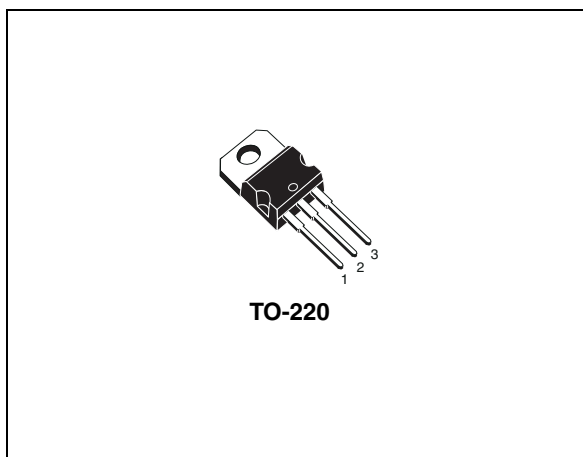


Figure 1. Internal schematic diagram

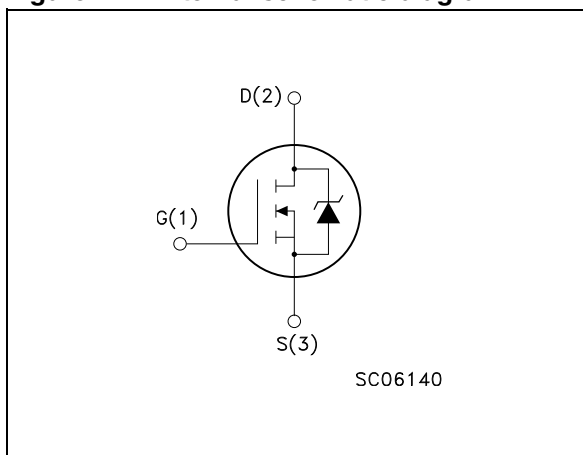


Table 1. Device summary

Order code	Marking	Package	Packaging
STP40NF10	P40NF10@	TO-220	Tube

# Contents

<b>1</b>	<b>Electrical ratings</b> .....	<b>3</b>
<b>2</b>	<b>Electrical characteristics</b> .....	<b>4</b>
	2.1 Electrical characteristics (curves) .....	6
<b>3</b>	<b>Test circuit</b> .....	<b>8</b>
<b>4</b>	<b>Package mechanical data</b> .....	<b>9</b>
<b>5</b>	<b>Revision history</b> .....	<b>11</b>

# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage ( $V_{GS} = 0$ )	100	V
$V_{GS}$	Gate- source voltage	$\pm 20$	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	50	A
$I_D$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	35	A
$I_{DM}^{(2)}$	Drain current (pulsed)	200	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	150	W
	Derating factor	1	W/ $^\circ\text{C}$
$dv/dt^{(3)}$	Peak diode recovery voltage slope	27	V/ns
$E_{AS}^{(4)}$	Single pulse avalanche energy	385	mJ
$T_{stg}$	Storage temperature	- 55 to 175	$^\circ\text{C}$
$T_j$	Max. operating junction temperature		

1. Limited by wire bonding
2. Pulse width limited by safe operating area
3.  $I_{SD} \leq 50\text{ A}$ ,  $di/dt \leq 600\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  $T_j \leq T_{JMAX}$ .
4. Starting  $T_j = 25\text{ }^\circ\text{C}$ ,  $I_D = 50\text{ A}$ ,  $V_{DD} = 25\text{ V}$

**Table 3. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	1	$^\circ\text{C}/\text{W}$
$R_{thj-a}$	Thermal resistance junction-ambient max	62.5	$^\circ\text{C}/\text{W}$
$T_l$	Maximum lead temperature for soldering purpose	300	$^\circ\text{C}$

## 2 Electrical characteristics

( $T_{CASE} = 25\text{ °C}$  unless otherwise specified)

**Table 4. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown voltage	$I_D = 250\ \mu\text{A}$ , $V_{GS} = 0$	100			V
$I_{DSS}$	Zero gate voltage Drain current ( $V_{GS} = 0$ )	$V_{DS} = \text{Max rating}$ $V_{DS} = \text{Max rating}$ , $T_C = 125\text{ °C}$			1 10	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate-body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20\ \text{V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\ \mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\ \text{V}$ , $I_D = 25\ \text{A}$		0.025	0.028	$\Omega$

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 15\ \text{V}$ , $I_D = 28\ \text{A}$	-	22		S
$C_{iss}$	Input capacitance	$V_{DS} = 25\ \text{V}$ , $f = 1\ \text{MHz}$ , $V_{GS} = 0$	-	2180		pF
$C_{oss}$	Output capacitance			298		pF
$C_{rss}$	Reverse transfer capacitance			83.7		pF
$Q_g$	Total gate charge	$V_{DD} = 50\ \text{V}$ , $I_D = 40\ \text{A}$ , $V_{GS} = 10\ \text{V}$ <i>(see Figure 15)</i>	-	46.5	62	nC
$Q_{gs}$	Gate-source charge			13.3		nC
$Q_{gd}$	Gate-drain charge			17.5	22.5	nC

1. Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5.

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 50\ \text{V}$ , $I_D = 25\ \text{A}$ $R_G = 4.7\ \Omega$ , $V_{GS} = 10\ \text{V}$ <i>(see Figure 14)</i>	-	21	-	ns
$t_r$	Rise time			46	-	ns
$t_{d(off)}$	Turn-off-delay time			54	-	ns
$t_f$	Fall time			13	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$I_{SD}$	Source-drain current		-		80	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		320	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 50A, V_{GS} = 0$	-		1.5	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 50A, V_{DD} = 25V$ $di/dt = 100A/\mu s,$ $T_j = 150^\circ C$ <i>(see Figure 16)</i>	-	80		ns
$Q_{rr}$	Reverse recovery charge			250		nC
$I_{RRM}$	Reverse recovery current			6.4		A

1. Pulse width limited by safe operating area.

2. Pulsed: Pulse duration = 300  $\mu s$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for TO-220

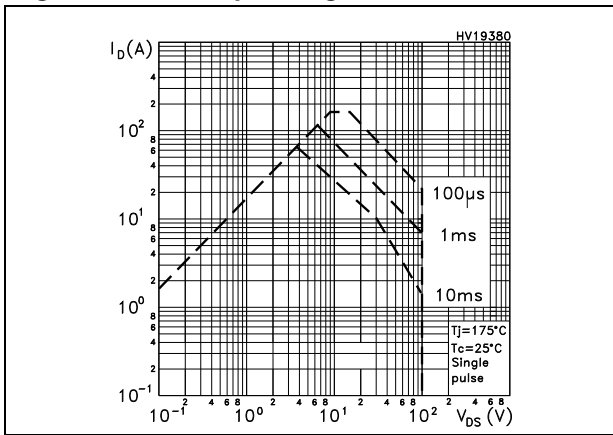


Figure 3. Thermal impedance for TO-220

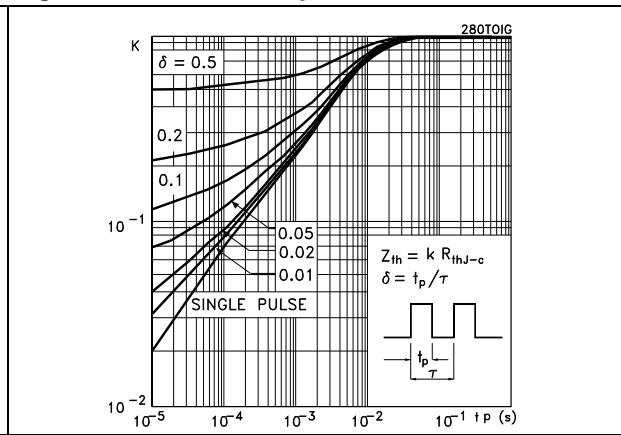


Figure 4. Output characteristics

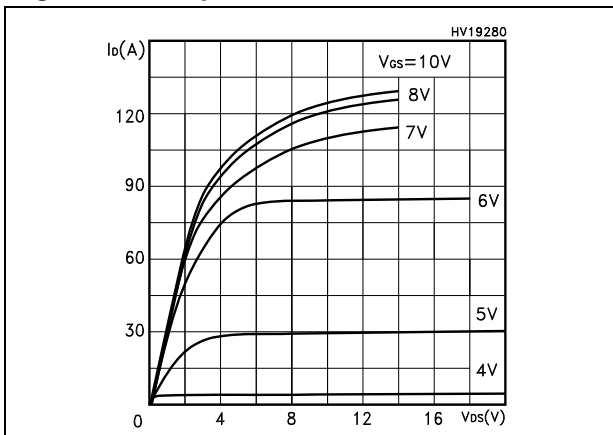


Figure 5. Transfer characteristics

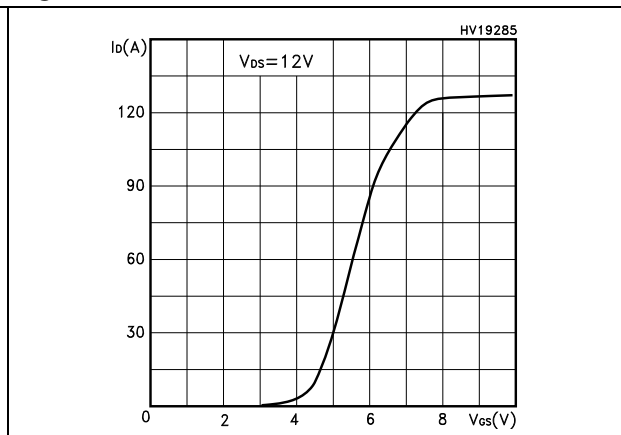


Figure 6. Transconductance

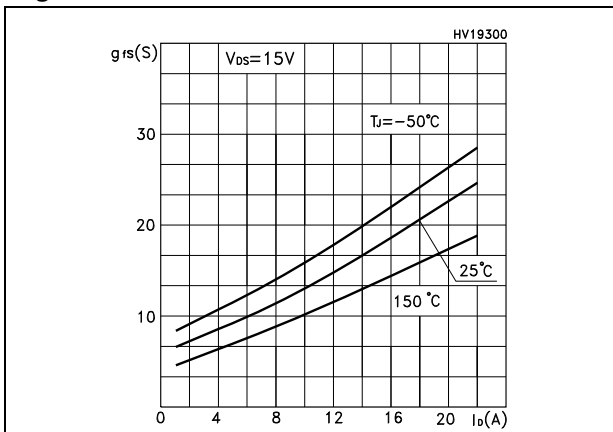


Figure 7. Static drain-source on resistance

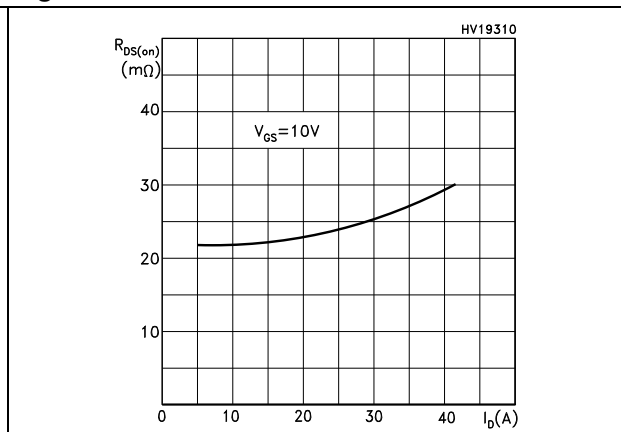


Figure 8. Gate charge vs. gate-source voltage Figure 9. Capacitance variations

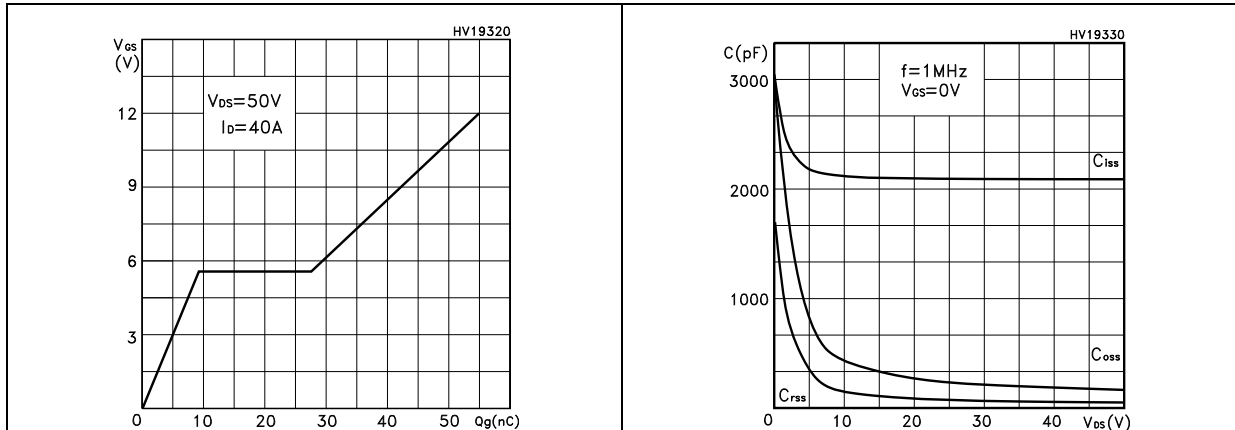


Figure 10. Normalized gate threshold voltage vs. temperature Figure 11. Normalized on resistance vs. temperature

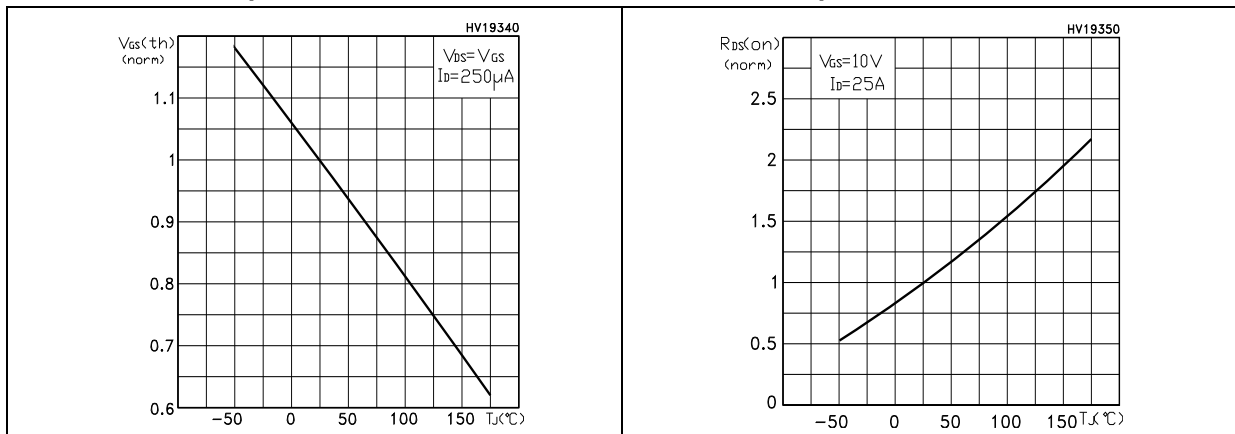
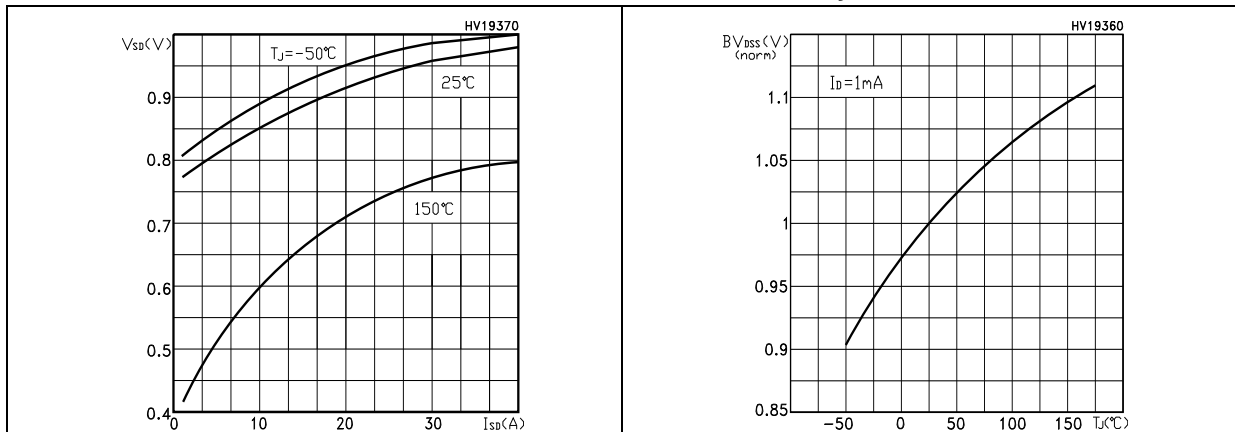
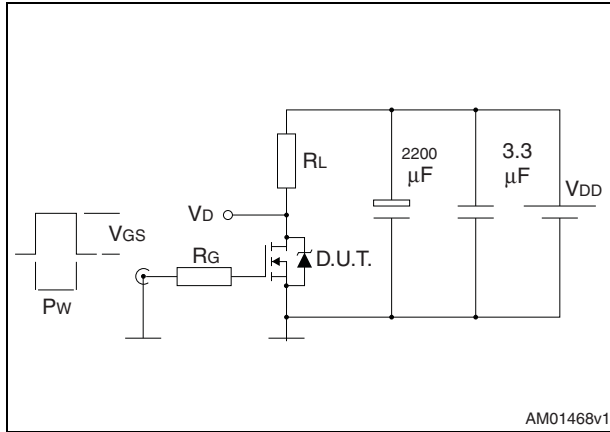


Figure 12. Source-drain diode forward characteristics Figure 13. Normalized breakdown voltage vs.  $T_j$



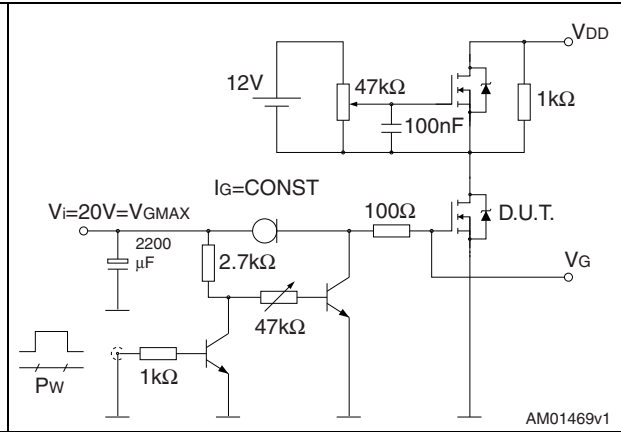
### 3 Test circuit

**Figure 14. Switching times test circuit for resistive load**



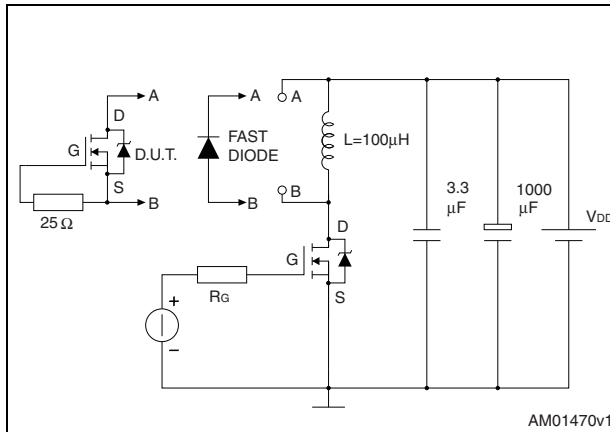
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**Figure 15. Gate charge test circuit**



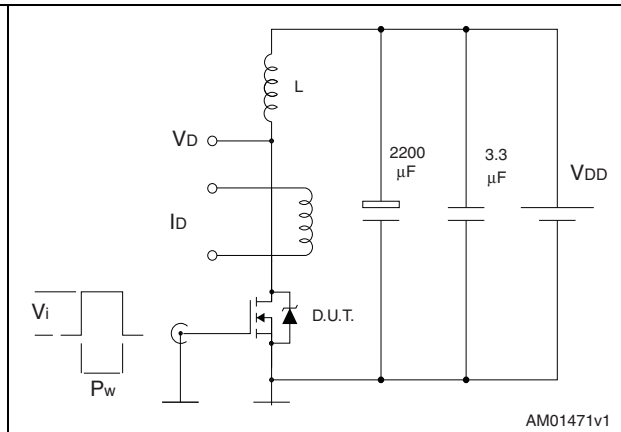
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**Figure 16. Test circuit for inductive load switching and diode recovery times**



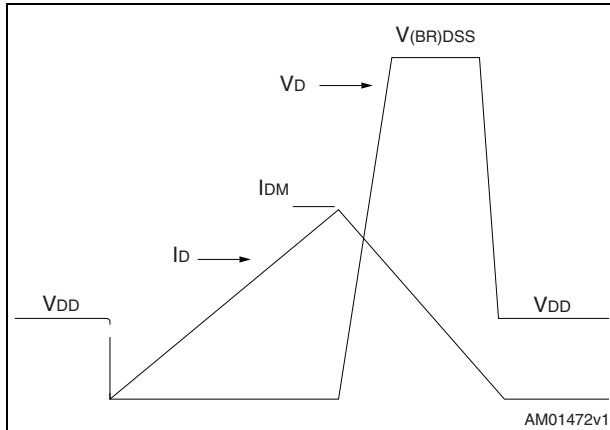
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**Figure 17. Unclamped Inductive load test circuit**



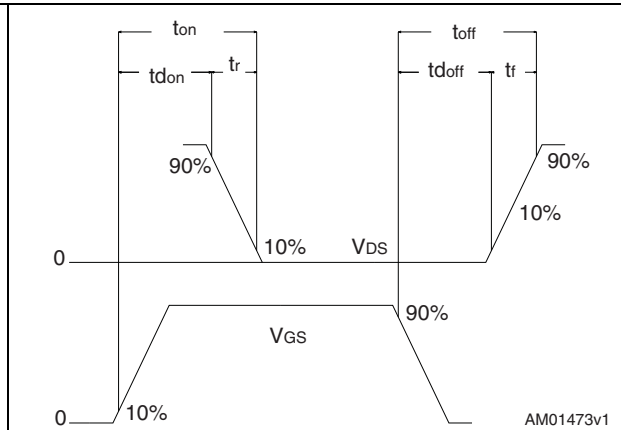
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**Figure 18. Unclamped inductive waveform**



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**Figure 19. Switching time waveform**



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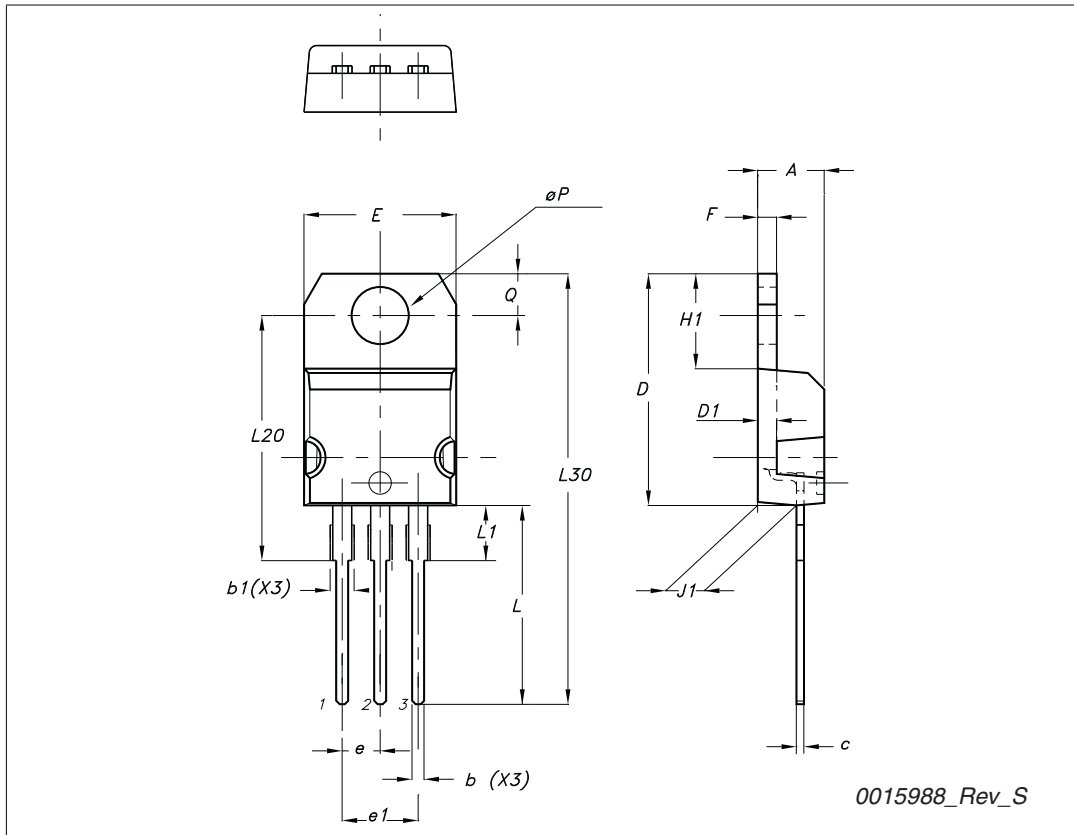


## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

TO-220 type A mechanical data

Dim	mm		
	Min	Typ	Max
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
∅P	3.75		3.85
Q	2.65		2.95



## 5 Revision history

**Table 8. Document revision history**

Date	Revision	Changes
16-Dec-2004	1	First version.
17-Aug-2006	2	The document has been reformatted.
31-Jan-2007	3	Typo mistake on <a href="#">Table 2</a> .
19-Sep-2007	4	Added DPAK.
10-Nov-2010	5	Removed DPAK.

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