



STB5N52K3, STD5N52K3, STF5N52K3 STP5N52K3, STU5N52K3

N-channel 525 V, 1.2 Ω , 4.4 A SuperMESH3™ Power MOSFET
D²PAK, DPAK, TO-220FP, TO-220, IPAK

Features

Order codes	V _{DSS}	R _{DS(on)} max	I _D	P _w
STB5N52K3	525 V	< 1.5 Ω	4.4 A	70 W
STD5N52K3				70 W
STF5N52K3				25 W
STP5N52K3				70 W
STU5N52K3				70 W

- 100% avalanche tested
- Extremely high dv/dt capability
- Gate charge minimized
- Very low intrinsic capacitance
- Improved diode reverse recovery characteristics
- Zener-protected

Application

Switching applications

Description

These devices are made using the SuperMESH3™ Power MOSFET technology that is obtained via improvements applied to STMicroelectronics' SuperMESH™ technology combined with a new optimized vertical structure. The resulting product has an extremely low on resistance, superior dynamic performance and high avalanche capability, making it especially suitable for the most demanding applications.

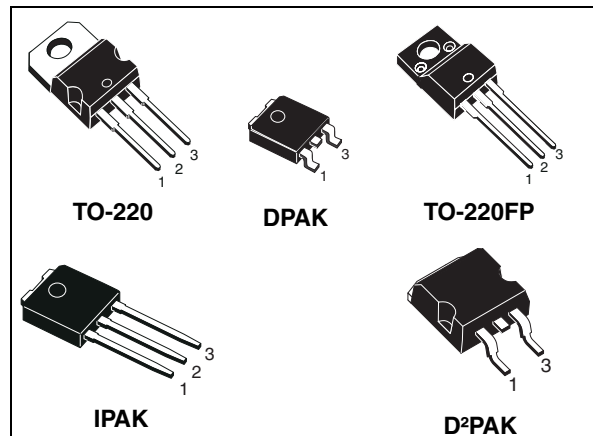


Figure 1. Internal schematic diagram

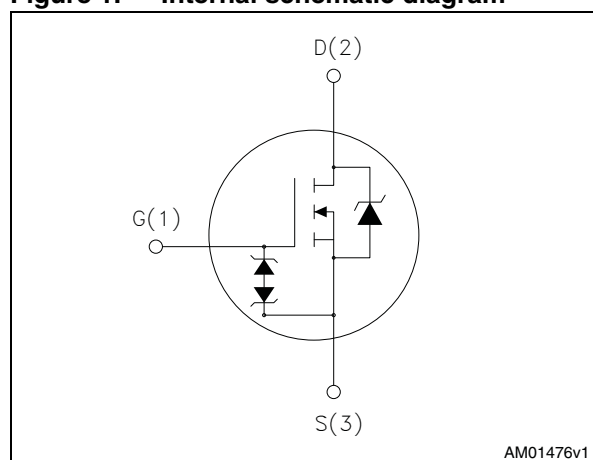


Table 1. Device summary

Order codes	Marking	Package	Packaging
STB5N52K3	5N52K3	D ² PAK	Tape and reel
STD5N52K3		DPAK	
STF5N52K3		TO-220FP	Tube
STP5N52K3		TO-220	
STU5N52K3		IPAK	

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value			Unit
		TO-220 D ² PAK	DPAK IPAK	TO-220FP	
V _{DS}	Drain- source voltage	525			V
V _{GS}	Gate- source voltage	± 30			V
I _D	Drain current (continuous) at T _C = 25 °C	4.4		4.4 ⁽¹⁾	A
I _D	Drain current (continuous) at T _C = 100 °C	2.77		2.77 ⁽¹⁾	A
I _{DM} ⁽²⁾	Drain current (pulsed)	17.6		17.6 ⁽¹⁾	A
P _{TOT}	Total dissipation at T _C = 25 °C	70		25	W
I _{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T _J max)	2.2			A
E _{AS}	Single pulse avalanche energy (starting T _J = 25 °C, I _D = I _{AR} , V _{DD} = 50 V)	100			mJ
dv/dt ⁽³⁾	Peak diode recovery voltage slope	12			V/ns
V _{ISO}	Insulation withstand voltage (AC)			2500	V
T _J T _{stg}	Operating junction temperature Storage temperature	- 55 to 150			°C

- Limited only by maximum temperature allowed
- Pulse width limited by safe operating area
- $I_{SD} \leq 4.4 \text{ A}$, $di/dt \leq 100 \text{ A}/\mu\text{s}$, $V_{DS \text{ peak}} \leq V_{(BR)DSS}$, $V_{DD} = 80\% V_{(BR)DSS}$.

Table 3. Thermal data

Symbol	Parameter	Value					Unit
		TO-220	D ² PAK	TO-220FP	IPAK	DPAK	
R _{thj-case}	Thermal resistance junction-case max.	1.79		5		1.79	°C/W
R _{thj-amb}	Thermal resistance junction-ambient max	62.5			100		°C/W
R _{thj-pcb}	Thermal resistance junction-pcb max.		30			50	°C/W
T _J	Maximum lead temperature for soldering purpose	300		300			°C/W

2 Electrical characteristics

(T_{case} =25 °C unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	I _D = 1 mA, V _{GS} = 0	525			V
I _{DSS}	Zero gate voltage drain current (V _{GS} = 0)	V _{DS} = Max rating V _{DS} = Max rating, T _C =125 °C			1 50	μA μA
I _{GSS}	Gate-body leakage current (V _{DS} = 0)	V _{GS} = ± 20 V; V _{DS} =0			10	μA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 50 μA	3	3.75	4.5	V
R _{DS(on)}	Static drain-source on resistance	V _{GS} = 10 V, I _D = 2.2 A		1.2	1.5	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C _{iss}	Input capacitance	V _{DS} = 100 V, f = 1 MHz, V _{GS} = 0	-	545	-	pF
C _{oss}	Output capacitance			45		
C _{rss}	Reverse transfer capacitance			8		
C _{oss eq.} ⁽¹⁾	Equivalent output capacitance	V _{DS} = 0 to 420 V, V _{GS} = 0	-	33	-	pF
R _g	Gate input resistance	f=1 MHz open drain	-	4.7	-	Ω
Q _g	Total gate charge	V _{DD} = 420 V, I _D = 4.4 A,	-	17	-	nC
Q _{gs}	Gate-source charge	V _{GS} = 10 V		3		
Q _{gd}	Gate-drain charge	(see Figure 19)		10		

1. C_{oss eq.} is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 420\text{ V}$, $I_D = 4.4\text{ A}$, $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (see Figure 18)	-	9	-	ns
t_r	Rise time		-	11	-	ns
$t_{d(off)}$	Turn-off-delay time		-	29	-	ns
t_f	Fall time		-	16	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
I_{SD}	Source-drain current		-		4.4	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				17.6	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 4.4\text{ A}$, $V_{GS} = 0$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 4.4\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$ (see Figure 20)	-	210		ns
Q_{rr}	Reverse recovery charge			1.3		μC
I_{RRM}	Reverse recovery current			12		A
t_{rr}	Reverse recovery time	$I_{SD} = 4.4\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$ $T_J = 150\text{ }^\circ\text{C}$ (see Figure 20)	-	240		ns
Q_{rr}	Reverse recovery charge			1.6		μC
I_{RRM}	Reverse recovery current			13		A

1. Pulse width limited by safe operating area

2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

Table 8. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
BV_{GSO}	Gate-source breakdown voltage	$I_{gs} = \pm 1\text{ mA}$ (open drain)	30	-	-	V

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area TO-220, D²PAK

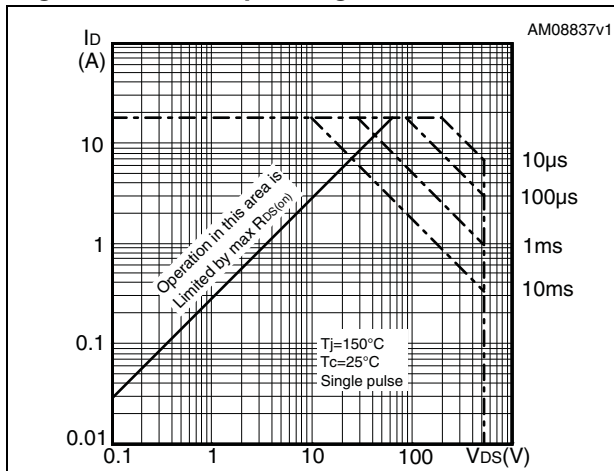


Figure 3. Thermal impedance TO-220, D²PAK

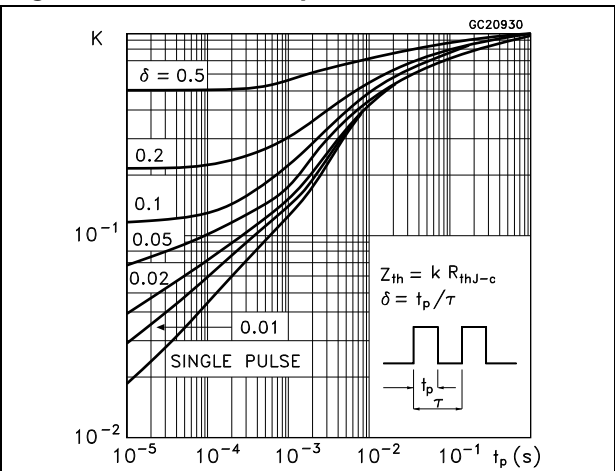


Figure 4. Safe operating area TO-220FP

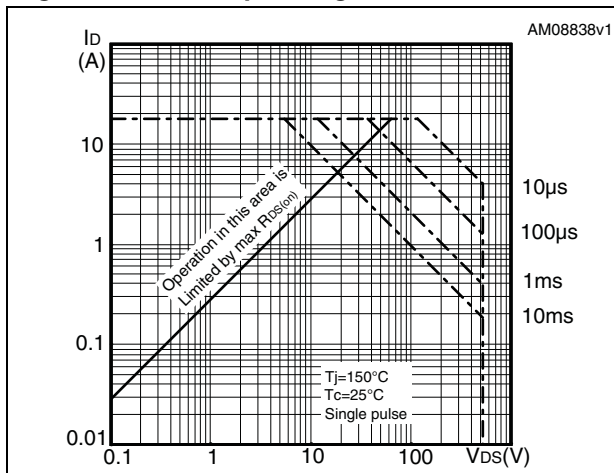


Figure 5. Thermal impedance TO-220FP

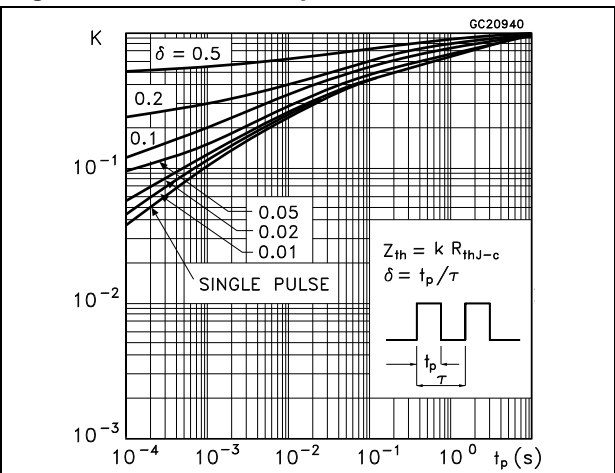


Figure 6. Safe operating area DPAK, IPAK

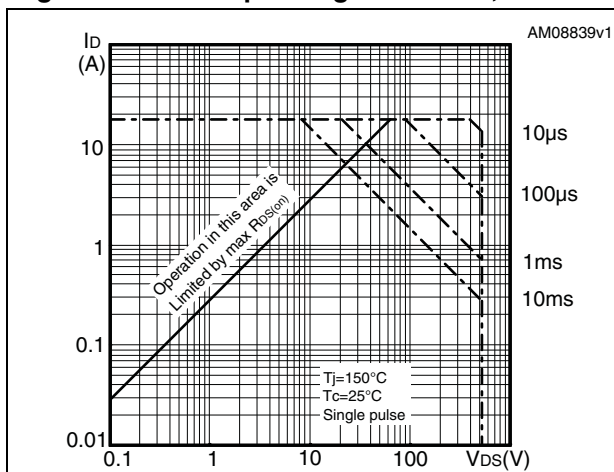


Figure 7. Thermal impedance DPAK, IPAK

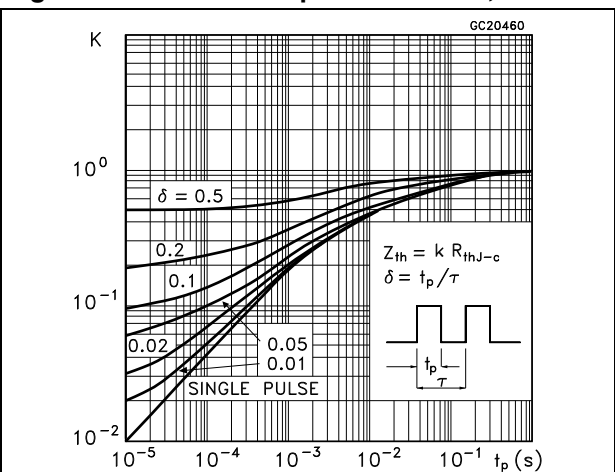


Figure 8. Output characteristics

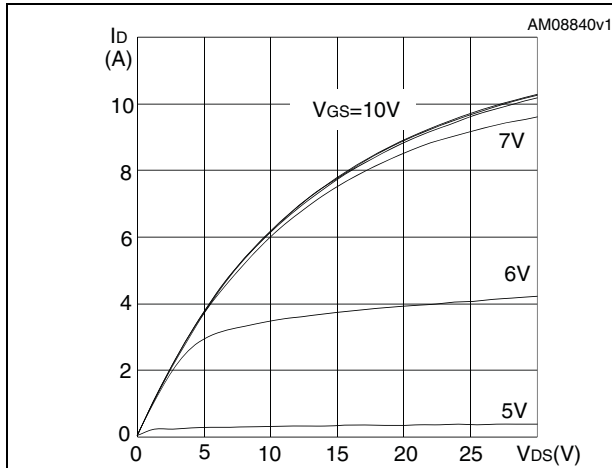


Figure 9. Transfer characteristics

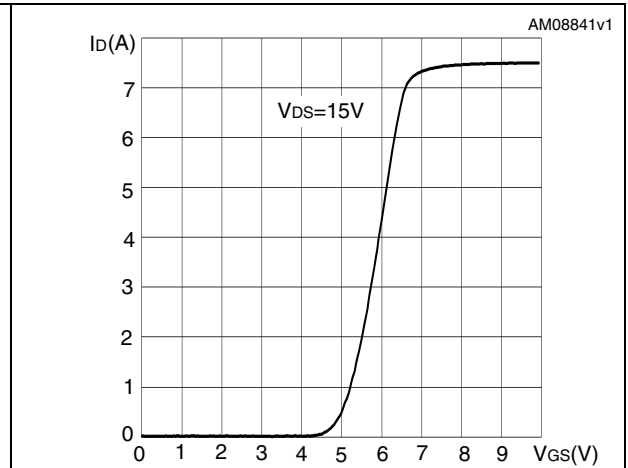


Figure 10. Normalized B_{VDSS} vs temperature

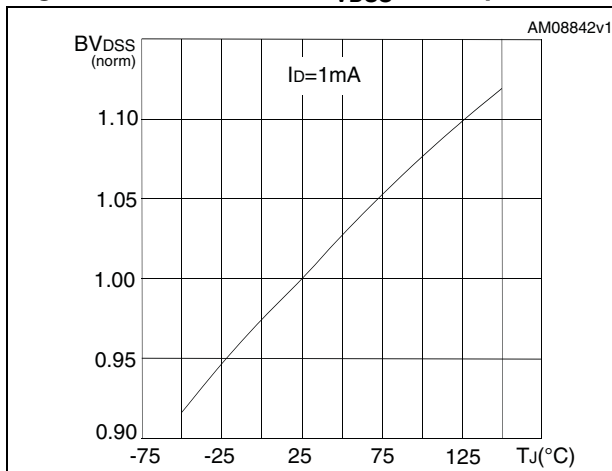


Figure 11. Static drain-source on resistance

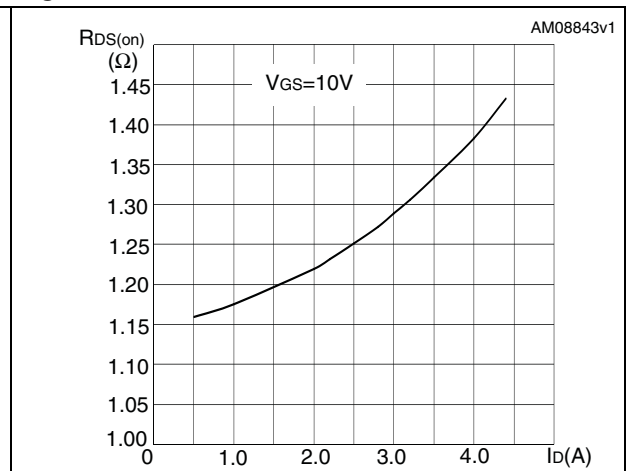


Figure 12. Gate charge vs gate-source voltage

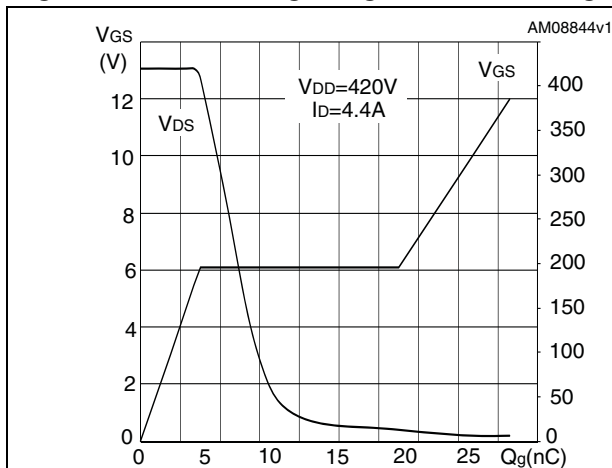


Figure 13. Capacitance variations

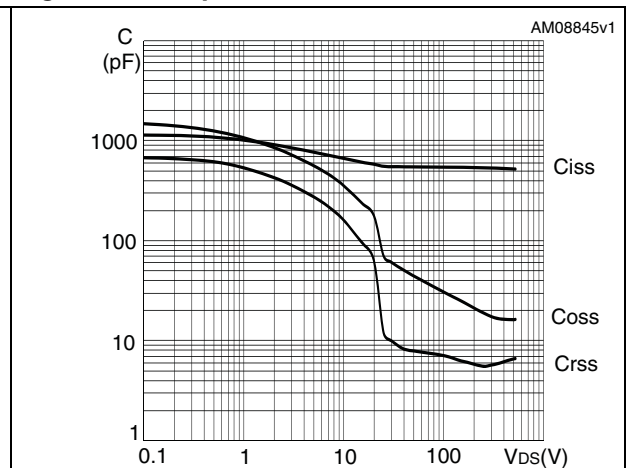


Figure 14. Normalized gate threshold voltage vs temperature

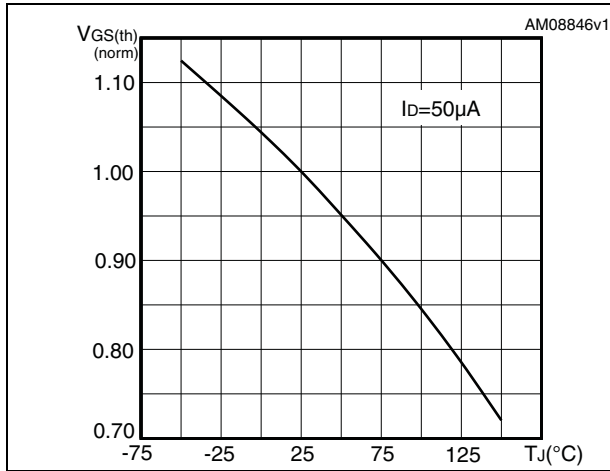


Figure 15. Normalized on resistance vs temperature

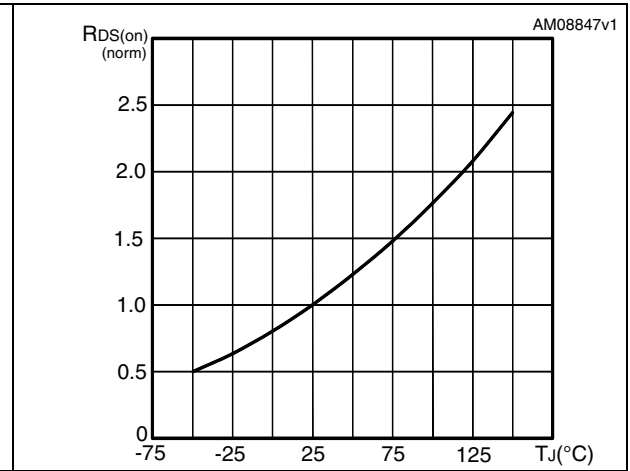


Figure 16. Source-drain diode forward characteristics

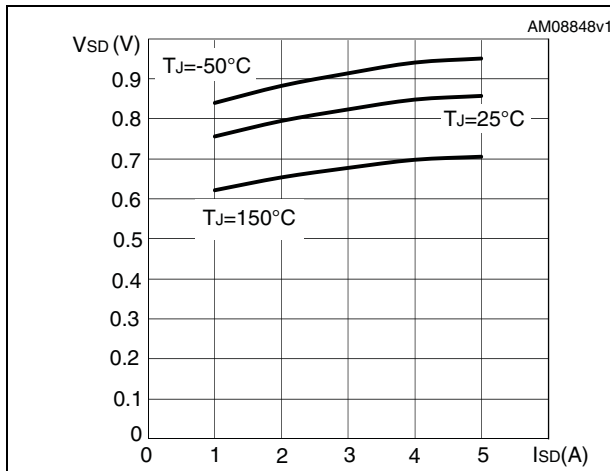
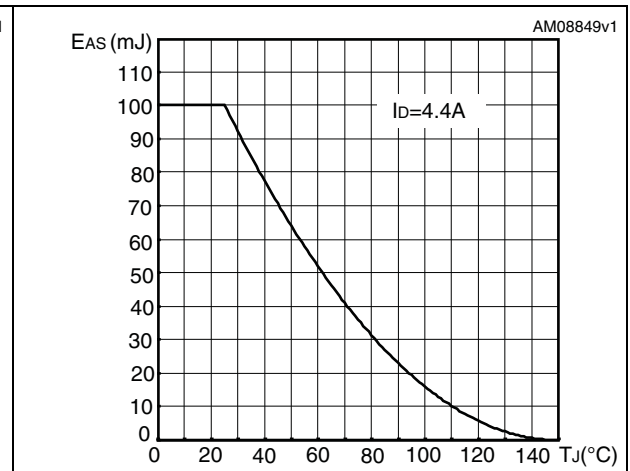


Figure 17. Maximum avalanche energy vs starting Tj



3 Test circuits

Figure 18. Switching times test circuit for resistive load

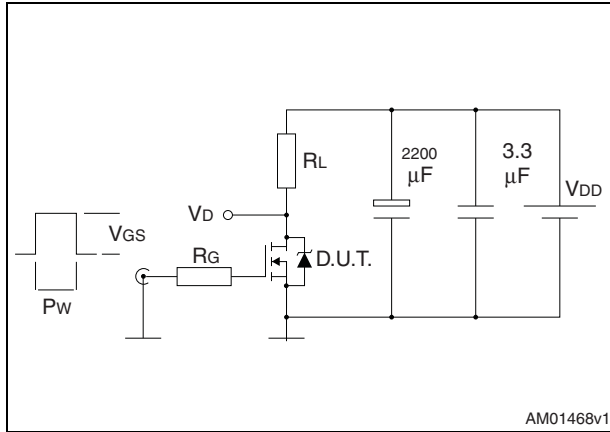


Figure 19. Gate charge test circuit

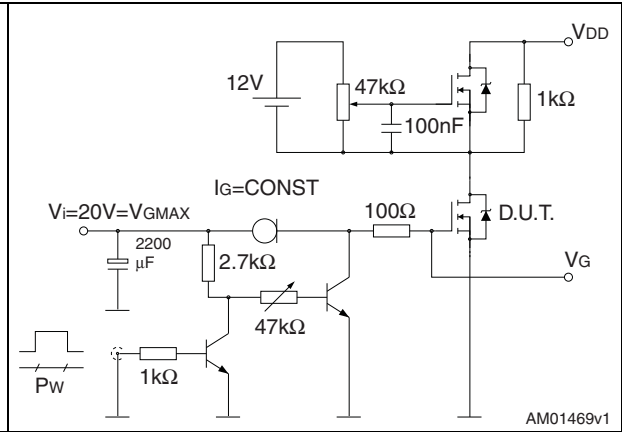


Figure 20. Test circuit for inductive load switching and diode recovery times

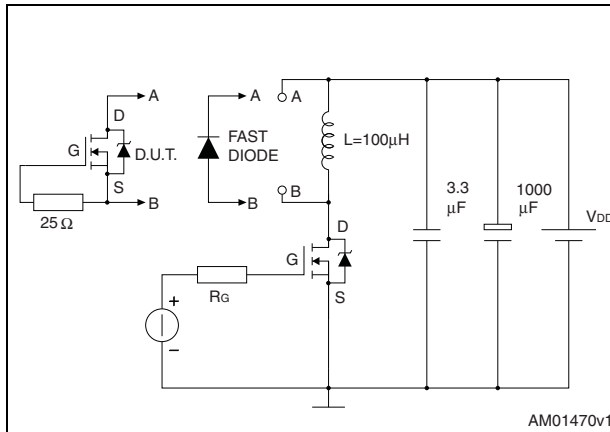


Figure 21. Unclamped inductive load test circuit

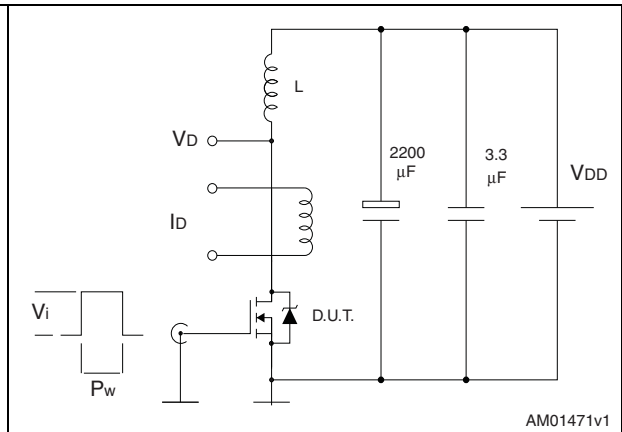


Figure 22. Unclamped inductive waveform

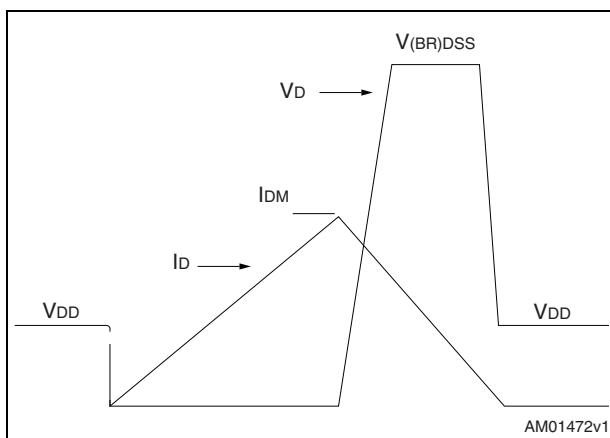
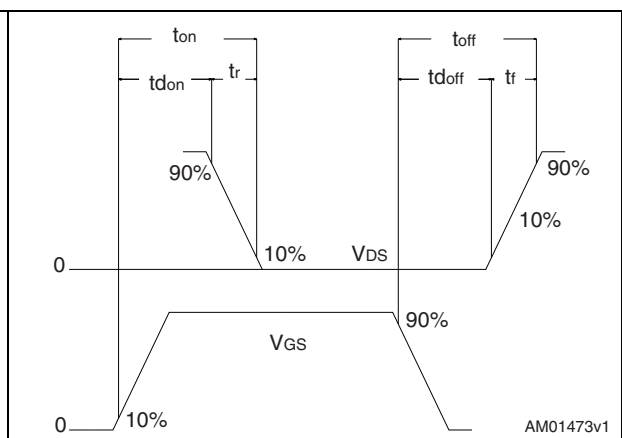


Figure 23. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 9. TO-220FP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

Figure 24. TO-220FP drawing

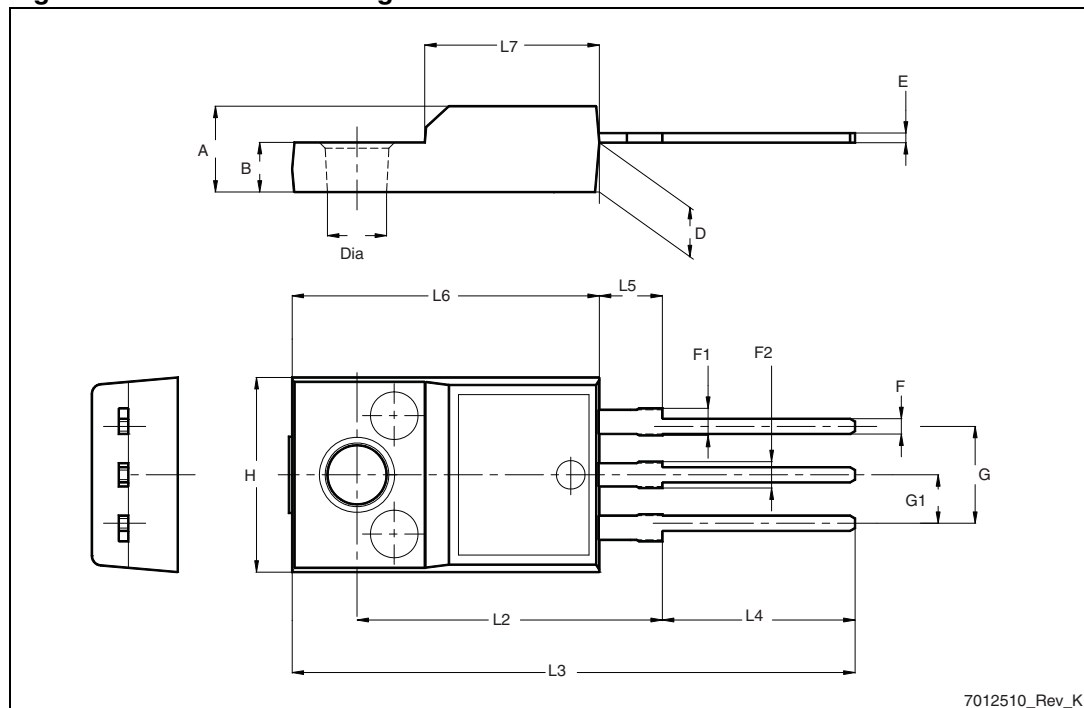


Table 10. DPAK (TO-252) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1		
L1		2.80	
L2		0.80	
L4	0.60		1
R		0.20	
V2	0°		8°

Figure 25. DPAK (TO-252) drawing

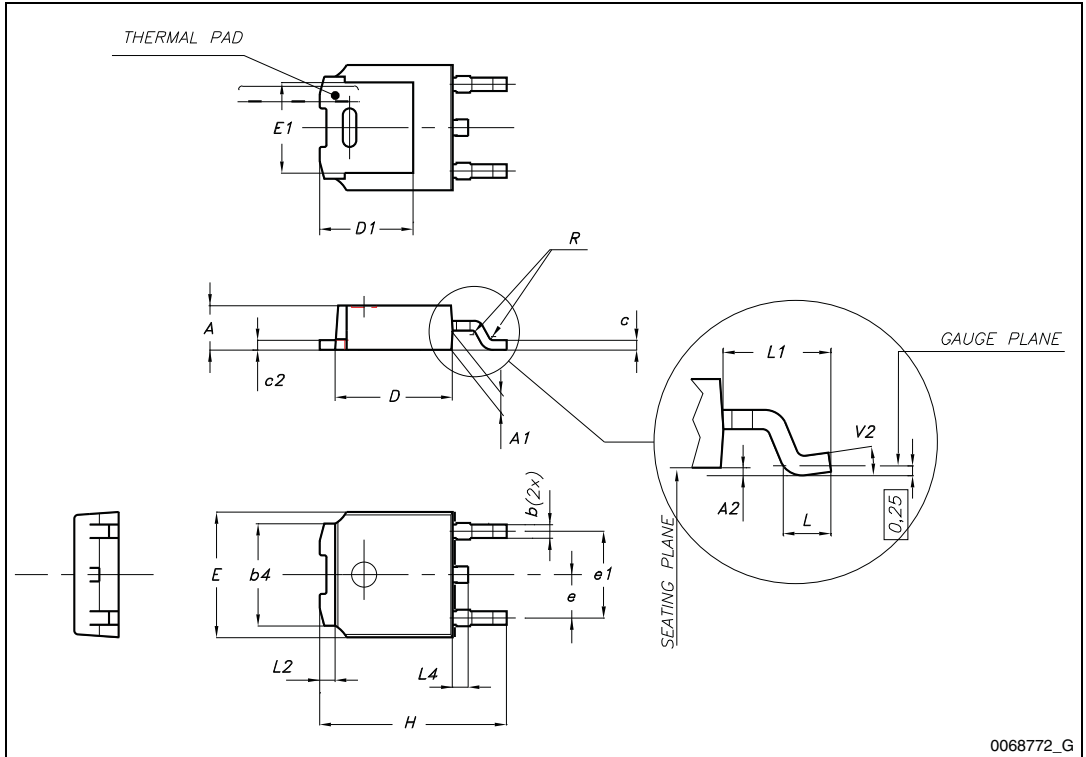


Table 11. TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
ØP	3.75		3.85
Q	2.65		2.95

Figure 26. TO-220 type A drawing

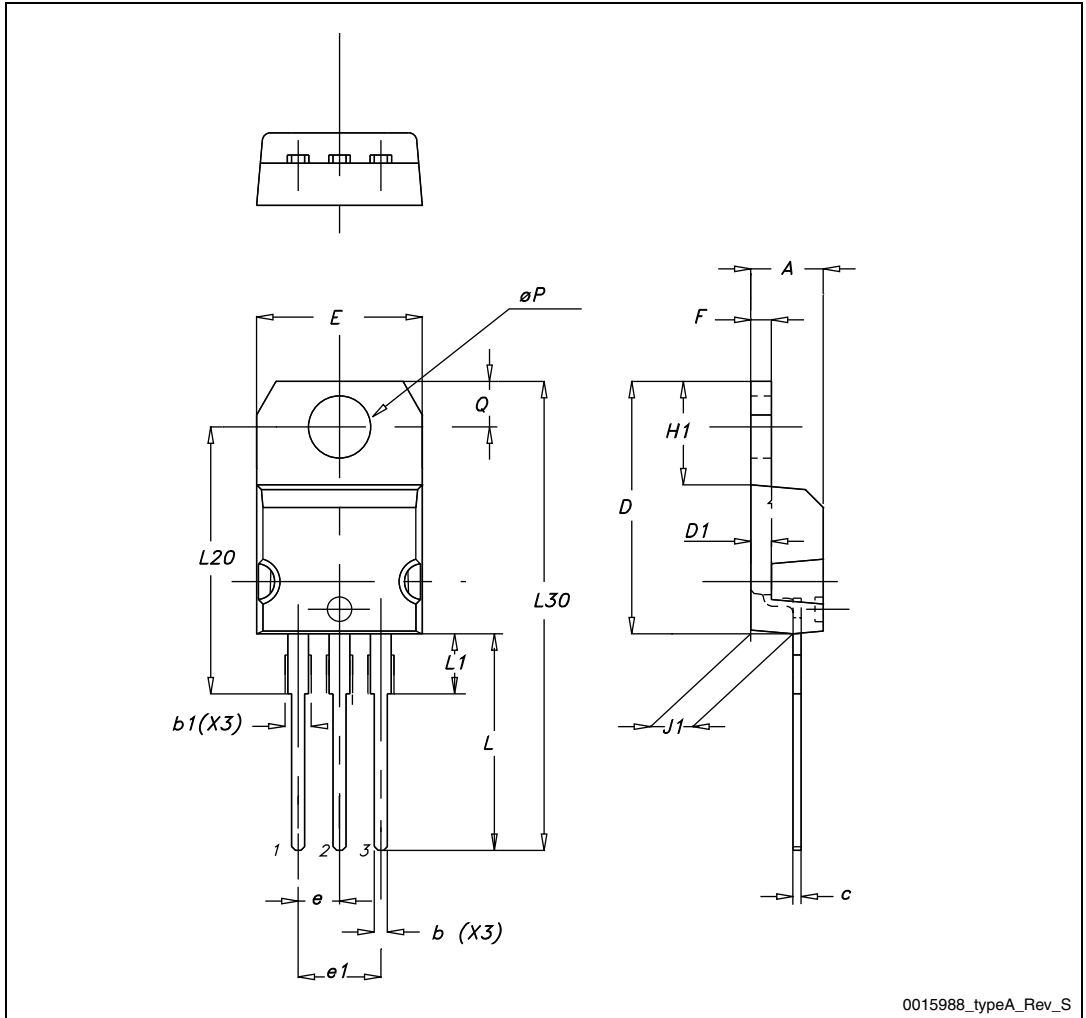


Table 12. D²PAK (TO-263) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50		
E	10		10.40
E1	8.50		
e		2.54	
e1	4.88		5.28
H	15		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.4	
V2	0°		8°

Figure 27. D²PAK (TO-263) drawing

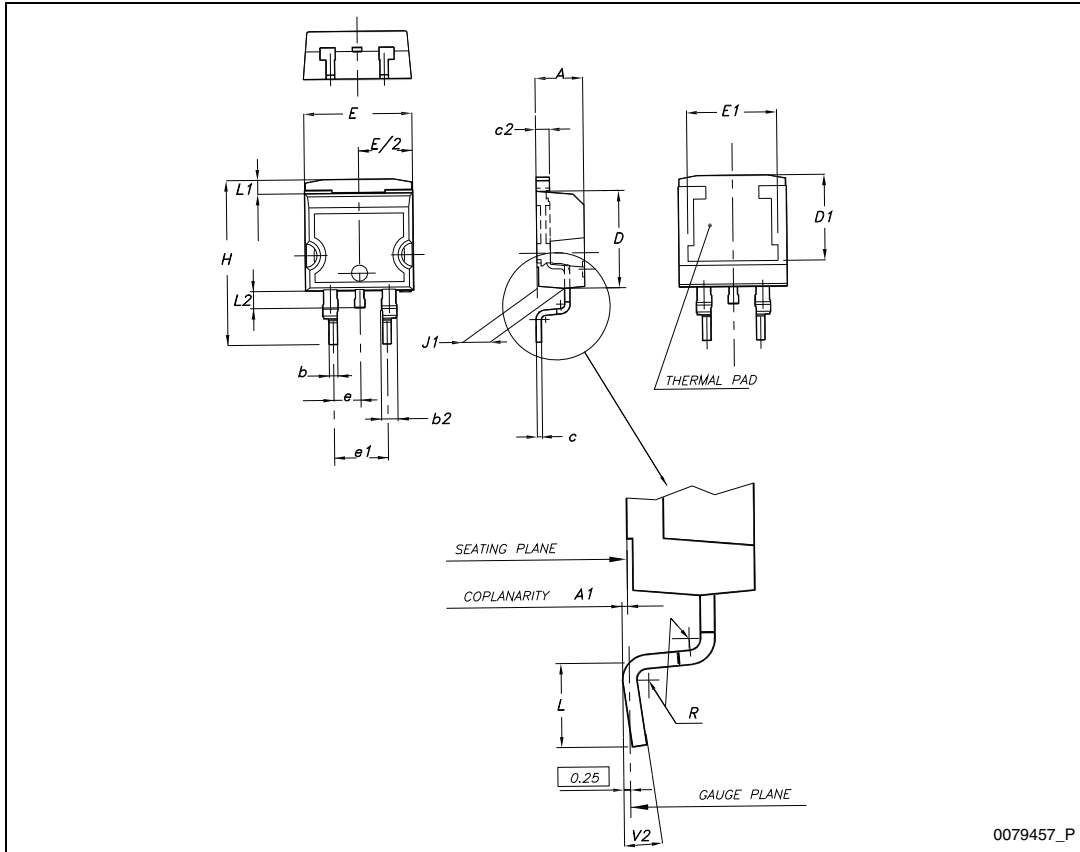


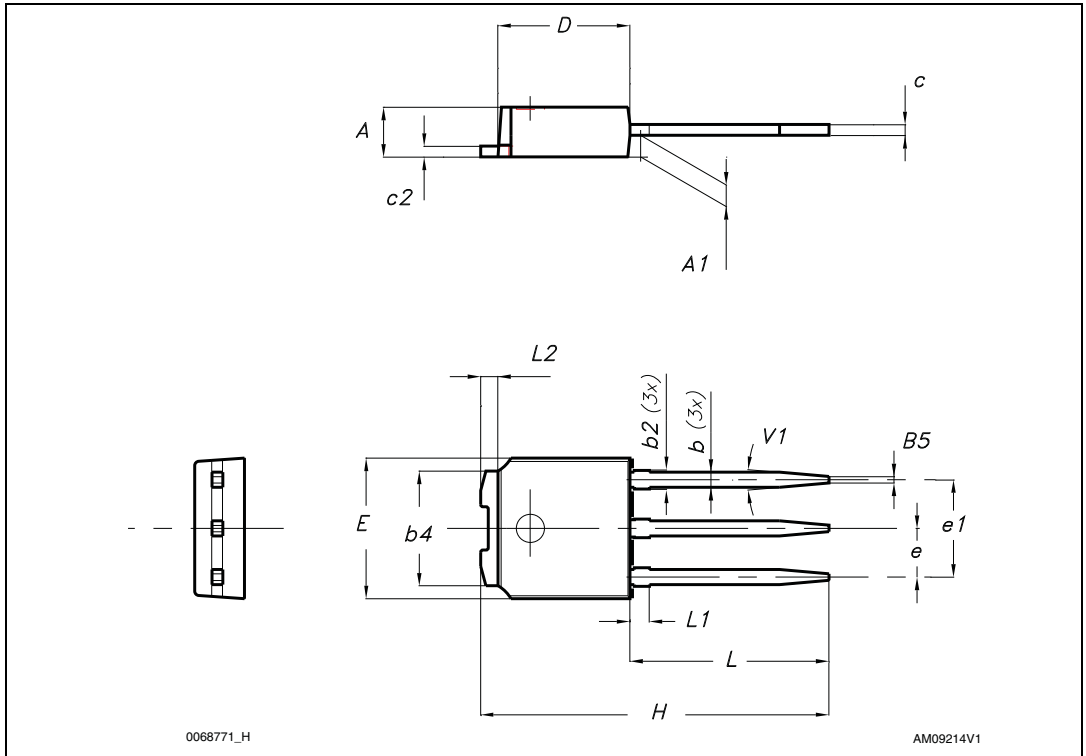
Table 13. IPAK (TO-251) mechanical data

DIM.	mm.		
	min.	typ	max.
A	2.20		2.40
A1	0.90		1.10
b	0.64		0.90
b2			0.95
b4	5.20		5.40
B5		0.3	
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
E	6.40		6.60
e		2.28	
e1	4.40		4.60

Table 13. IPAK (TO-251) mechanical data

H		16.10	
L	9.00		9.40
L1	0.80		1.20
L2		0.80	1.00
V1		10°	

Figure 28. IPAK (TO-251) drawing

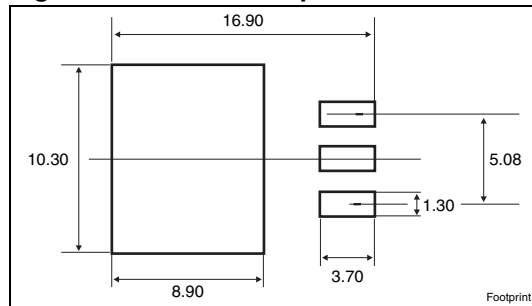


5 Package mechanical data

Table 14. D²PAK (TO-263) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base qty	1000	
P2	1.9	2.1	Bulk qty	1000	
R	50				
T	0.25	0.35			
W	23.7	24.3			

Figure 29. D²PAK footprint^(a)

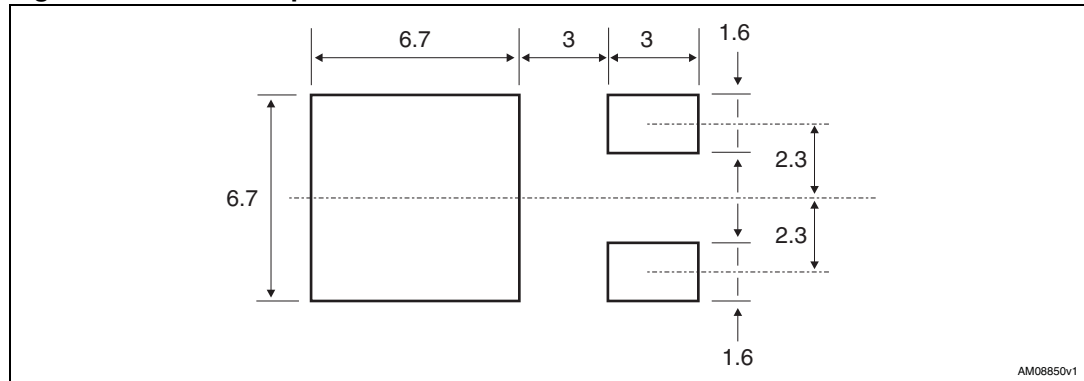


a. All dimension are in millimeters

Table 15. DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

Figure 30. DPAK footprint^(b)



b. All dimension are in millimeters

Figure 31. Tape for DPAK (TO-252) and D²PAK (TO-263)

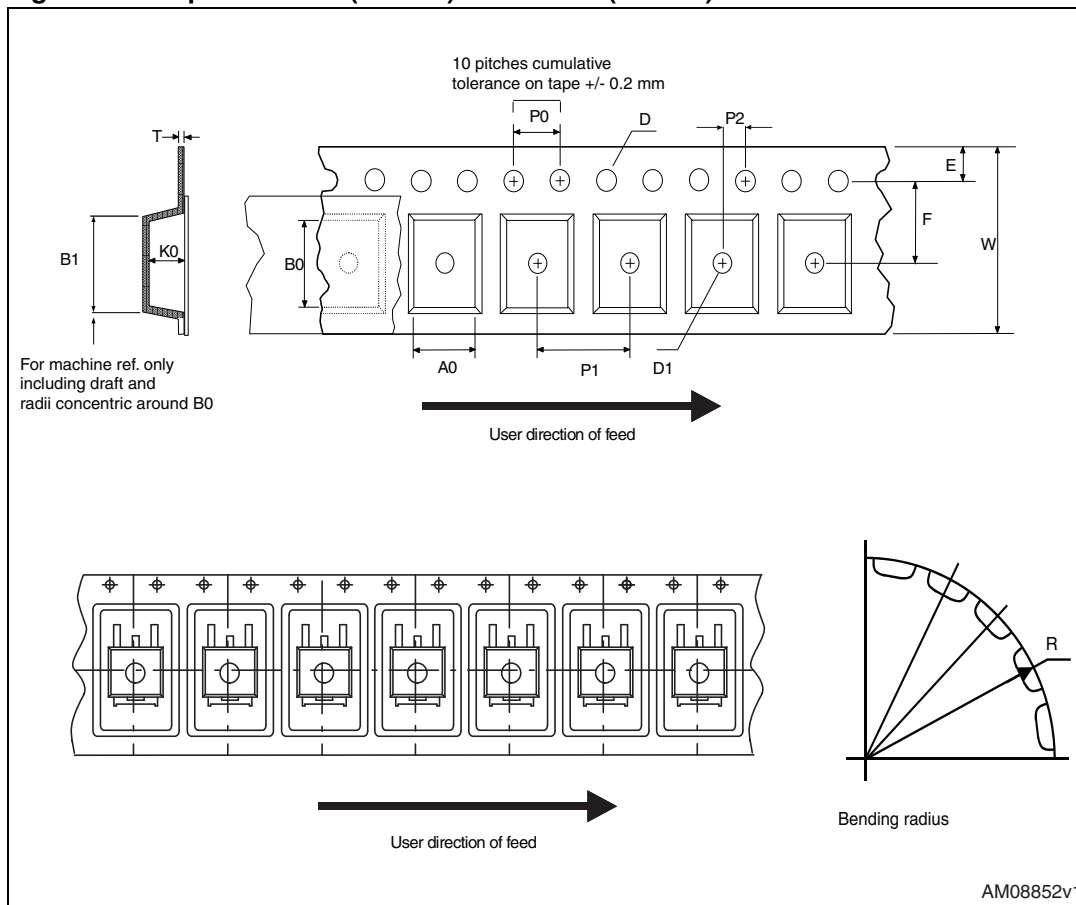
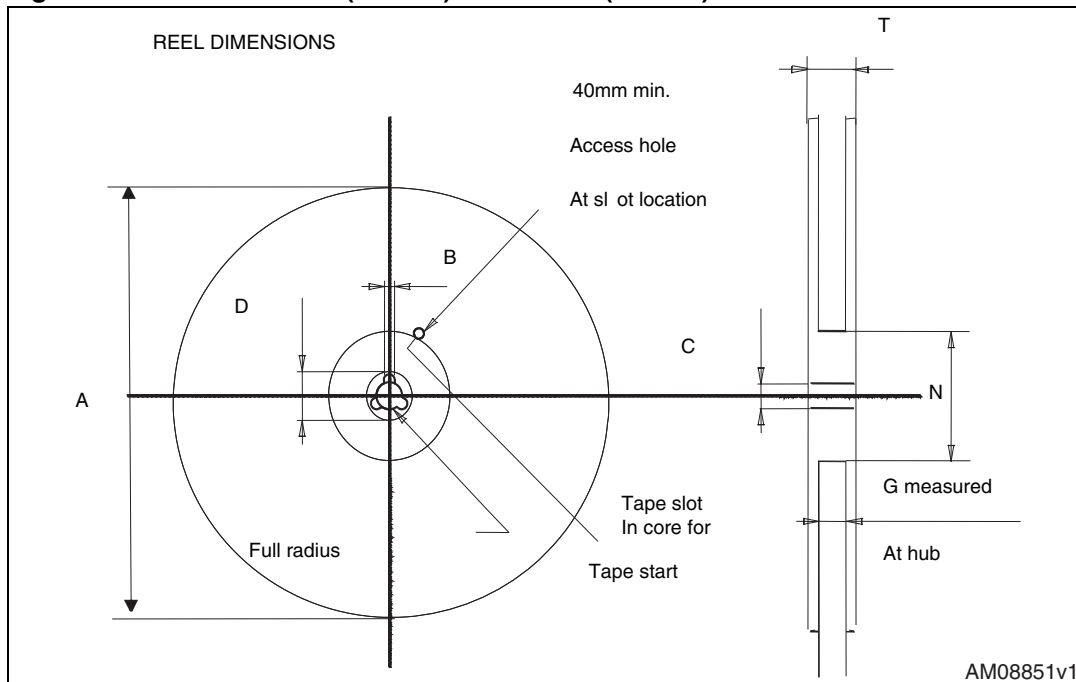


Figure 32. Reel for DPAK (TO-252) and D²PAK (TO-263)



6 Revision history

Table 16. Document revision history

Date	Revision	Changes
05-Jan-2010	1	First release.
14-Dec-2010	2	Document status promoted from preliminary data to datasheet.

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