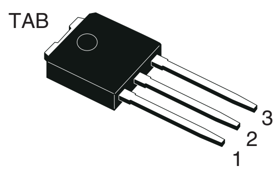
STU7NF25

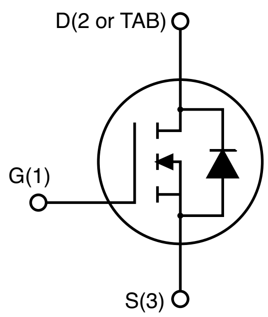
N-channel 250 V, 0.29 Ω typ., 8 A STripFET™ II Power MOSFET in IPAK package

Datasheet - production data



IPAK

Figure 1. Internal schematic diagram



Features

Order code	V_{DSS}	$R_{DS(on)}$ max.	I_D
STU7NF25	250 V	0.42 Ω	8 A

- 100% avalanche tested
- 175 °C junction temperature

Applications

- Switching applications

Description

This Power MOSFET has been developed using STMicroelectronics' unique STripFET process, which is specifically designed to minimize input capacitance and gate charge. This renders the device suitable for use as primary switch in advanced high-efficiency isolated DC-DC converters for telecom and computer applications, and applications with low gate charge driving requirements.

Table 1. Device summary

Order code	Marking	Package	Packaging
STU7NF25	7NF25	IPAK	Tube

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	250	V
V_{GS}	Gate-source voltage	±20	V
I_D	Drain current (continuous) at T_C = 25 °C	8	A
	Drain current (continuous) at T_C=100 °C	6	A
I_{DM}(1)	Drain current (pulsed)	32	A
P_{TOT}	Total dissipation at T_C = 25 °C	72	W
T_J T_{stg}	Operating junction temperature Storage temperature	-55 to 175	°C

1. Pulse width limited by safe operating area.

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	2.08	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-amb max	100	

Table 4. Avalanche data

Symbol	Parameter	Value	Unit
I_{AV}	Non-repetitive avalanche current	8	A
E_{AS}	Single pulse avalanche energy (starting T_J=25 °C, I_D=I_{AV}, V_{DD}=50 V)	110	mJ

2 Electrical characteristics

(T_{CASE}=25 °C unless otherwise specified).

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS}= 0	250	-		V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 250 V V_{DS} = 250 V, T_c=125 °C		-	1 50	µA µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = ±20 V		-	±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS}= V_{GS}, I_D = 250 µA	2	-	4	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS}= 10 V, I_D= 4 A		0.29	0.42	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} =25 V, f=1 MHz, V_{GS}=0	-	500	-	pF
C_{oss}	Output capacitance		-	90	-	pF
C_{rss}	Reverse transfer capacitance		-	15	-	pF
Q_g	Total gate charge	V_{DD}= 200 V, I_D = 8 A V_{GS} =10 V (see *Figure 14*)	-	16	-	nC
Q_{gs}	Gate-source charge		-	3.5	-	nC
Q_{gd}	Gate-drain charge		-	8	-	nC

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD}=125 V, I_D=4 A, R_G=4.7 Ω, V_{GS}=10 V (see *Figure 13* and *Figure 18*)	-	13	-	ns
t_r	Rise time		-	10	-	ns
$t_{d(off)}$	Turn-off delay time		-	26	-	ns
t_f	Fall time		-	6	-	ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM}	Source-drain current Source-drain current (pulsed)		-		8 32	A A
V_{SD}	Forward on voltage	I_{SD}=8 A, V_{GS}=0 V	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 8 A, di/dt = 100 A/µs, V_{DD} = 50 V (see *Figure 15*)	-	115		ns
Q_{rr}	Reverse recovery charge		-	470		nC
I_{RRM}	Reverse recovery current		-	8.5		A
t_{rr}	Reverse recovery time	I_{SD} = 8 A, di/dt = 100 A/µs, V_{DD} = 50 V, T_J= 150 °C (see *Figure 15*)	-	130		ns
Q_{rr}	Reverse recovery charge		-	580		nC
I_{RRM}	Reverse recovery current		-	9.5		A

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

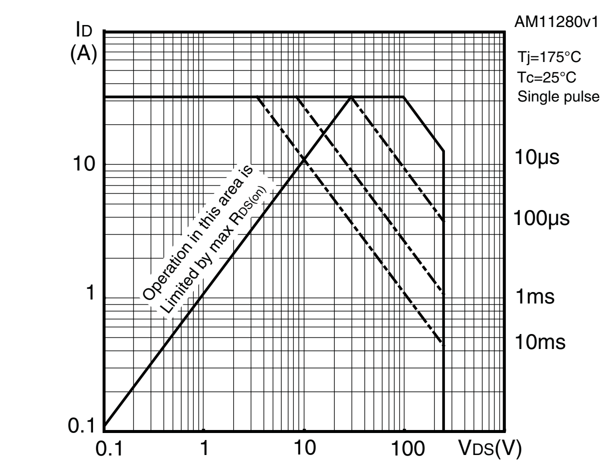


Figure 3. Thermal impedance

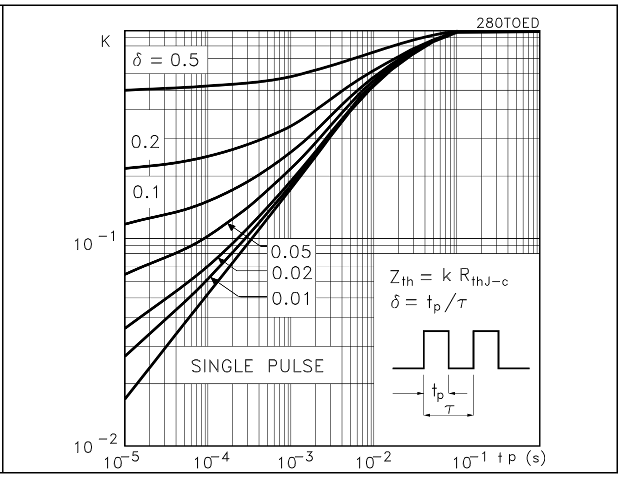


Figure 4. Output characteristics

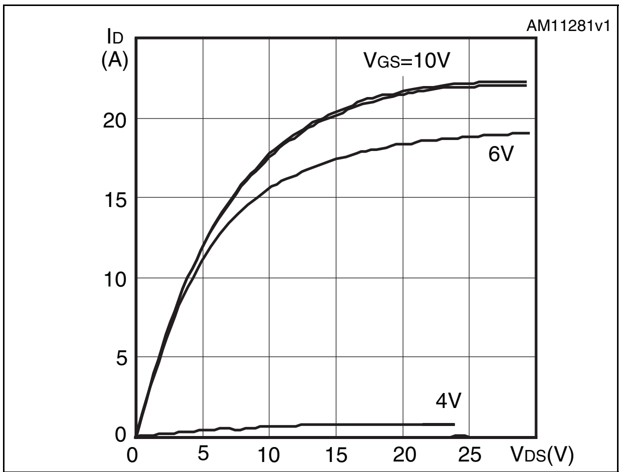


Figure 5. Transfer characteristics

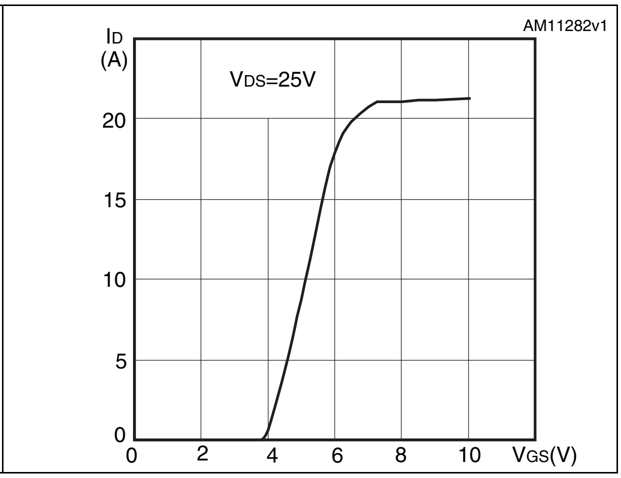


Figure 6. Normalized B_{VDSS} vs temperature

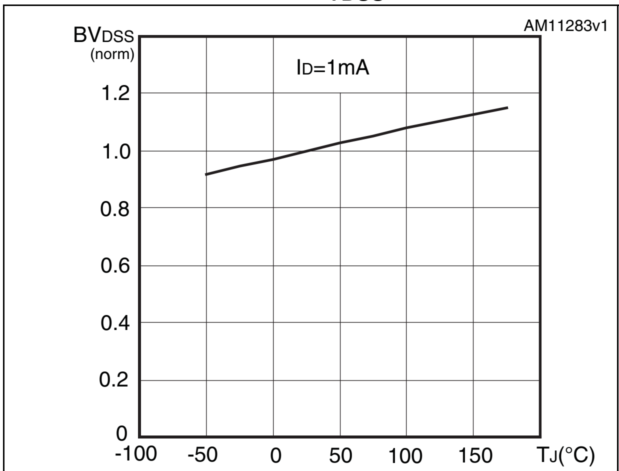


Figure 7. Static drain-source on-resistance

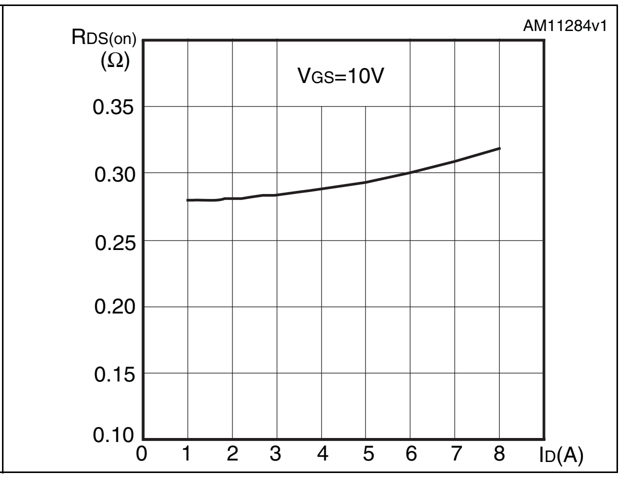


Figure 8. Gate charge vs gate-source voltage

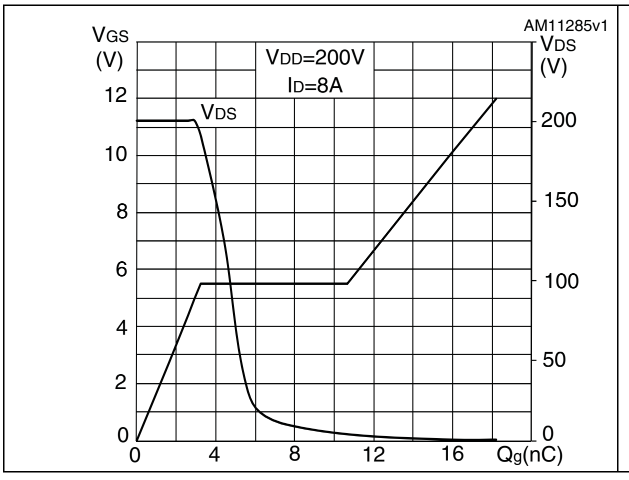


Figure 9. Capacitance variations

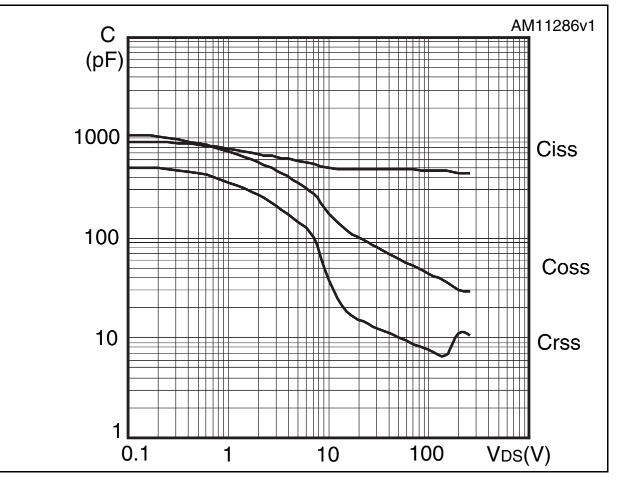


Figure 10. Normalized gate threshold voltage vs temperature

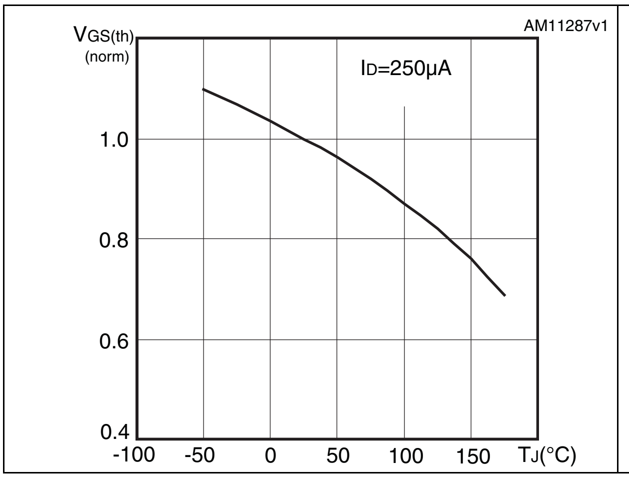


Figure 11. Normalized on resistance vs temperature

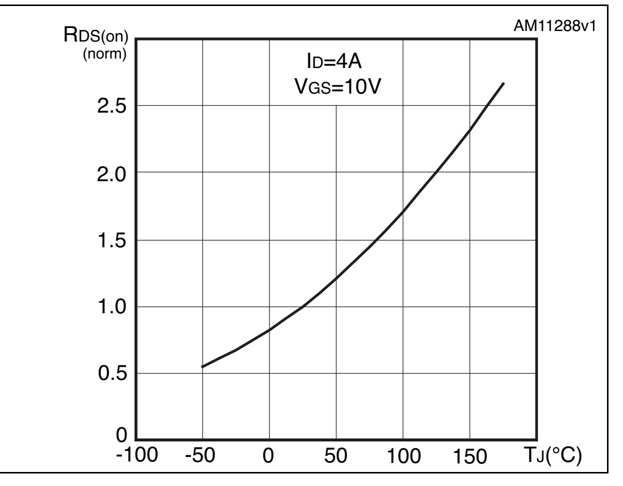
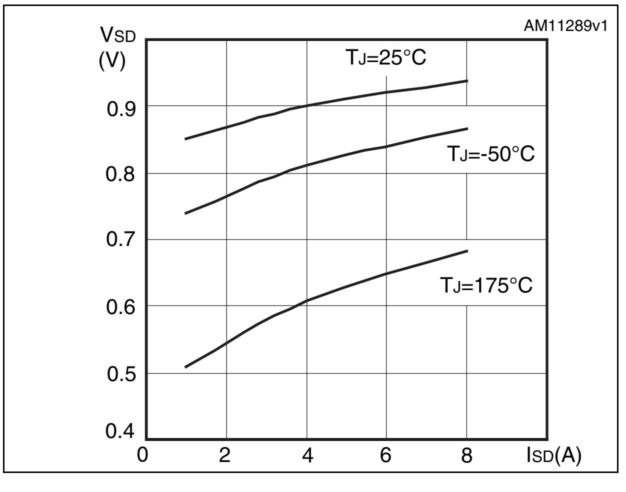


Figure 12. Source-drain diode forward characteristics



3 Test circuits

Figure 13. Switching times test circuit for resistive load

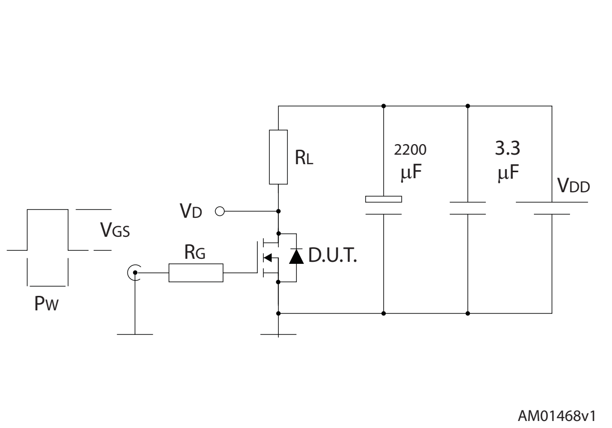


Figure 14. Gate charge test circuit

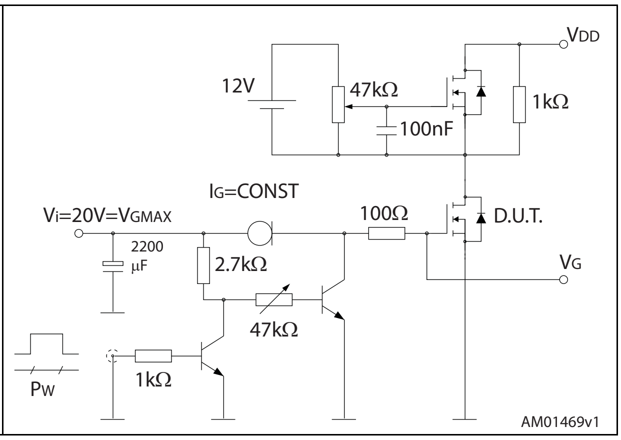


Figure 15. Test circuit for inductive load switching and diode recovery times

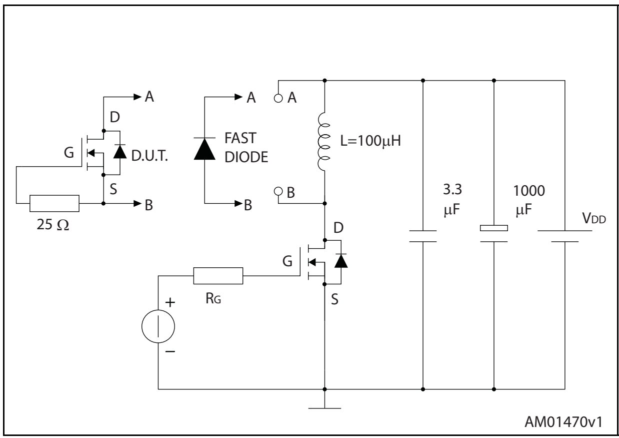


Figure 16. Unclamped inductive load test circuit

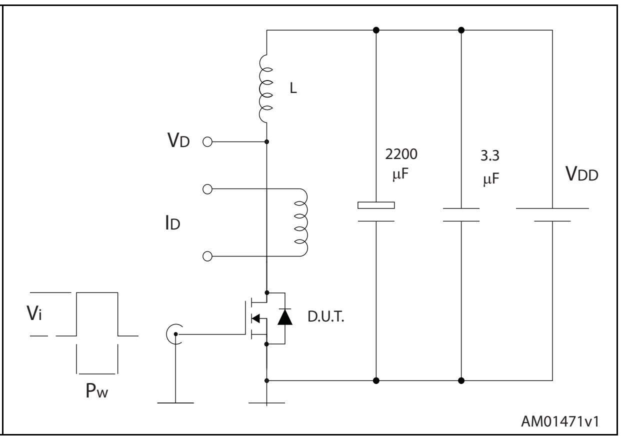


Figure 17. Unclamped inductive waveform

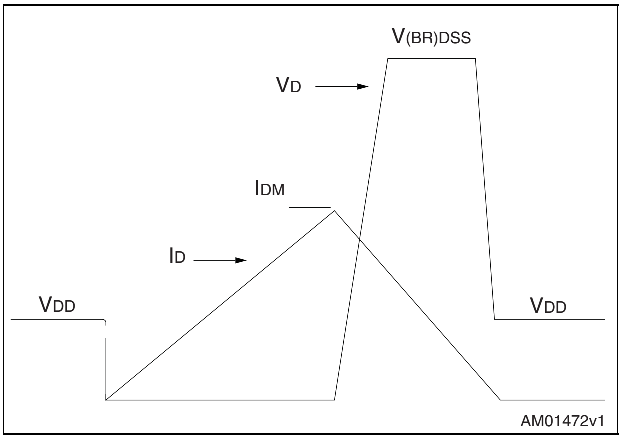
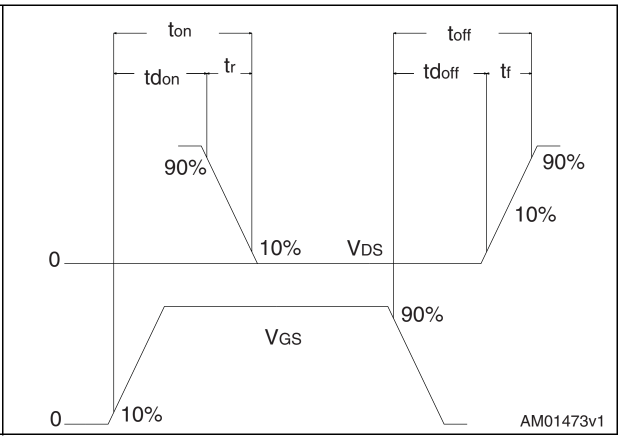


Figure 18. Switching time waveform



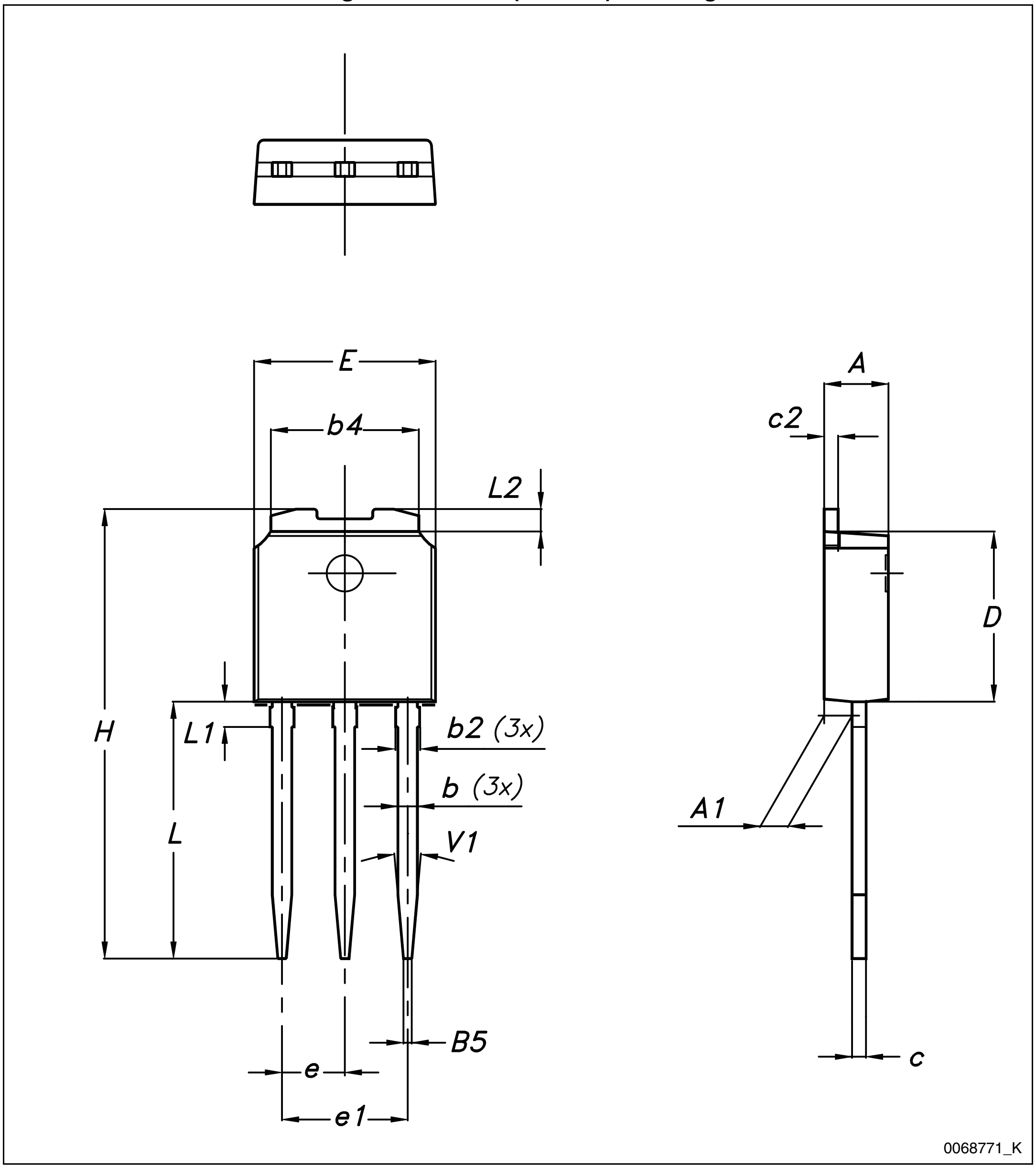
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 9. IPAK (TO-251) mechanical data

DIM	mm.		
	min.	typ.	max.
A	2.20		2.40
A1	0.90		1.10
b	0.64		0.90
b2			0.95
b4	5.20		5.40
B5		0.30	
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
E	6.40		6.60
e		2.28	
e1	4.40		4.60
H		16.10	
L	9.00		9.40
L1	0.80		1.20
L2		0.80	1.00
V1		10°	

Figure 19. IPAK (TO-251) drawing



5 Revision history

Table 10. Document revision history

Date	Revision	Changes
24-Jul-2013	1	First release.