

N-channel 600 V, 0.175  $\Omega$  typ., 18 A FDmesh II Plus™ low  $Q_g$  Power MOSFETs in D<sup>2</sup>PAK, TO-220 and TO-247 packages

Datasheet – production data

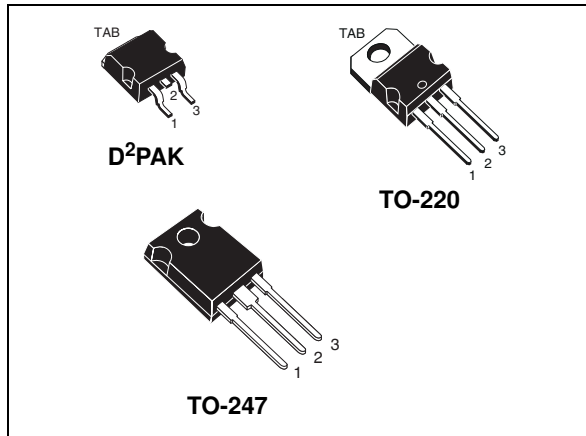
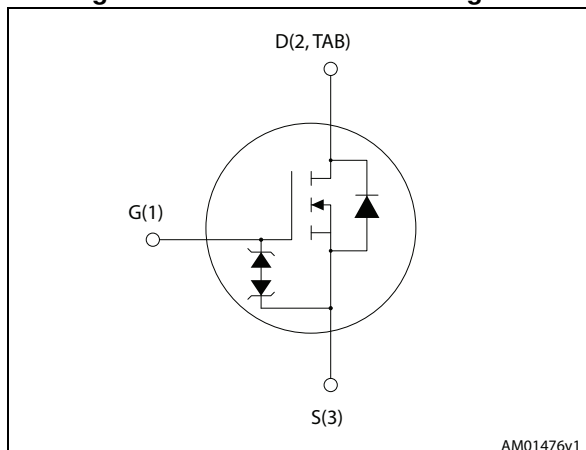


Figure 1. Internal schematic diagram



## Features

Order codes	$V_{DS}$ @ $T_{Jmax}$	$R_{DS(on)}$ max	$I_D$
STB24N60DM2	650 V	0.20 $\Omega$	18 A
STP24N60DM2			
STW24N60DM2			

- Extremely low gate charge and input capacitance
- Lower  $R_{DS(on)}$  x area vs previous generation
- Low gate input resistance
- 100% avalanche tested
- Zener-protected
- Extremely high dv/dt and avalanche capabilities

## Applications

- Switching applications

## Description

These FDmesh II Plus™ low  $Q_g$  Power MOSFETs with intrinsic fast-recovery body diode are produced using a new generation of MDmesh™ technology: MDmesh II Plus™ low  $Q_g$ . These revolutionary Power MOSFETs associate a vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. They are therefore suitable for the most demanding high efficiency converters and ideal for bridge topologies and ZVS phase-shift converters.

Table 1. Device summary

Order codes	Marking	Package	Packaging
STB24N60DM2	24N60DM2	D <sup>2</sup> PAK	Tape and reel
STP24N60DM2		TO-220	Tube
STW24N60DM2		TO-247	

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{GS}$	Gate-source voltage	$\pm 25$	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	18	A
$I_D$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	11	A
$I_{DM}^{(1)}$	Drain current (pulsed)	72	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	150	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	40	V/ns
$dv/dt^{(3)}$	MOSFET $dv/dt$ ruggedness	50	V/ns
$T_{stg}$	Storage temperature	- 55 to 150	$^\circ\text{C}$
$T_j$	Max. operating junction temperature		

1. Pulse width limited by safe operating area.
2.  $I_{SD} \leq 18\text{ A}$ ,  $di/dt \leq 400\text{ A}/\mu\text{s}$ ;  $V_{DS\text{ peak}} < V_{(BR)DSS}$ ;  $V_{DD}=400\text{ V}$ .
3.  $V_{DS} \leq 480\text{ V}$

**Table 3. Thermal data**

Symbol	Parameter	Value			Unit
		D <sup>2</sup> PAK	TO-220	TO-247	
$R_{thj-case}$	Thermal resistance junction-case max	0.83			$^\circ\text{C}/\text{W}$
$R_{thj-pcb}$	Thermal resistance junction-pcb max <sup>(1)</sup>	30			$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient max		62.5	50	$^\circ\text{C}/\text{W}$

1. When mounted on 1 inch<sup>2</sup> FR-4, 2 Oz copper board

**Table 4. Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AR}$	Avalanche current, repetitive or not repetitive (pulse width limited by $T_{jmax}$ )	3.5	A
$E_{AS}$	Single pulse avalanche energy (starting $T_j=25\text{ }^\circ\text{C}$ , $I_D = I_{AR}$ ; $V_{DD}=50$ )	180	mJ

## 2 Electrical characteristics

( $T_C = 25\text{ °C}$  unless otherwise specified)

**Table 5. On /off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$ , $V_{GS} = 0$	600			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = 600\text{ V}$			1.5	$\mu\text{A}$
		$V_{DS} = 600\text{ V}$ , $T_C = 125\text{ °C}$			100	$\mu\text{A}$
$I_{GSS}$	Gate-body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 25\text{ V}$			$\pm 10$	$\mu\text{A}$
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$ , $I_D = 9\text{ A}$		0.175	0.200	$\Omega$

**Table 6. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 100\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0$	-	1055	-	pF
$C_{oss}$	Output capacitance		-	56	-	pF
$C_{rss}$	Reverse transfer capacitance		-	2.4	-	pF
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{DS} = 0\text{ to }480\text{ V}$ , $V_{GS} = 0$	-	259	-	pF
$R_G$	Intrinsic gate resistance	$f = 1\text{ MHz}$ , $I_D = 0$	-	7	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 480\text{ V}$ , $I_D = 18\text{ A}$ , $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 17</a> )	-	29	-	nC
$Q_{gs}$	Gate-source charge		-	6	-	nC
$Q_{gd}$	Gate-drain charge		-	12	-	nC

1.  $C_{oss\text{ eq.}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$

**Table 7. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}$ , $I_D = 9\text{ A}$ , $R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 16</a> and <a href="#">21</a> )	-	15	-	ns
$t_r$	Rise time		-	8.7	-	ns
$t_{d(off)}$	Turn-off delay time		-	60	-	ns
$t_f$	Fall time		-	15	-	ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}^{(1)}$	Source-drain current		-		18	A
$I_{SDM}^{(2)}$	Source-drain current (pulsed)		-		72	A
$V_{SD}^{(3)}$	Forward on voltage	$I_{SD} = 18 \text{ A}$ , $V_{GS} = 0$	-		1.6	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 18 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 60 \text{ V}$ (see <a href="#">Figure 18</a> )	-	155		ns
$Q_{rr}$	Reverse recovery charge		-	956		nC
$I_{RRM}$	Reverse recovery current		-	12.5		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 18 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 60 \text{ V}$ , $T_j = 150 \text{ }^\circ\text{C}$ (see <a href="#">Figure 18</a> )	-	200		ns
$Q_{rr}$	Reverse recovery charge		-	1450		nC
$I_{RRM}$	Reverse recovery current		-	13		A

1. Limited by maximum junction temperature
2. Pulse width limited by safe operating area.
3. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for D<sup>2</sup>PAK, TO-220

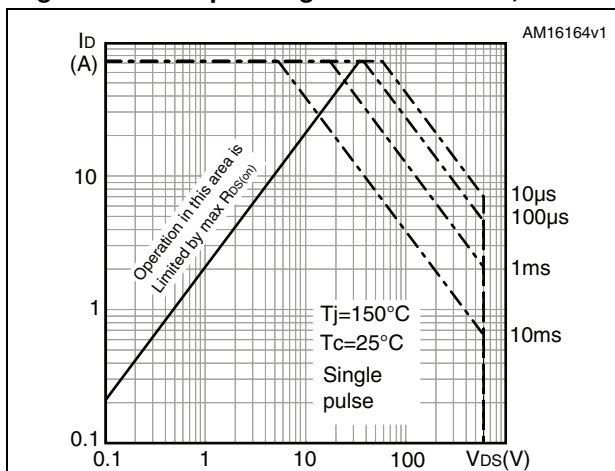


Figure 3. Thermal impedance D<sup>2</sup>PAK, TO-220

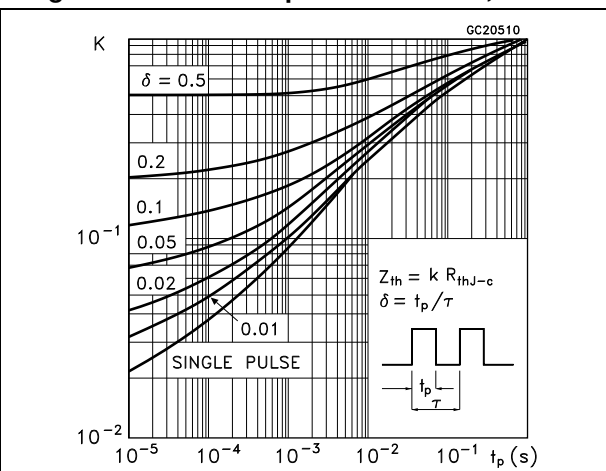


Figure 4. Safe operating area for TO-247

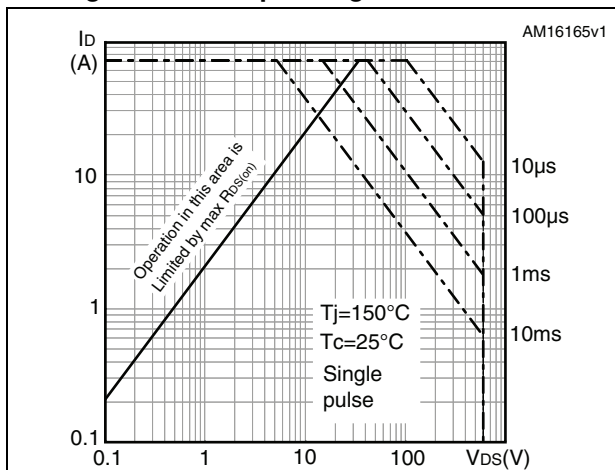


Figure 5. Thermal impedance for TO-247

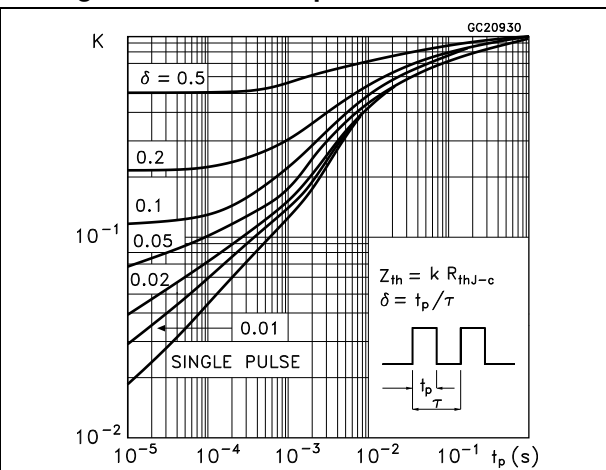


Figure 6. Output characteristics

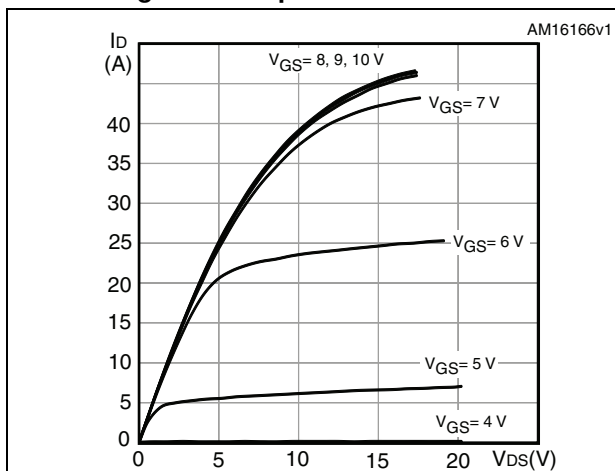


Figure 7. Transfer characteristics

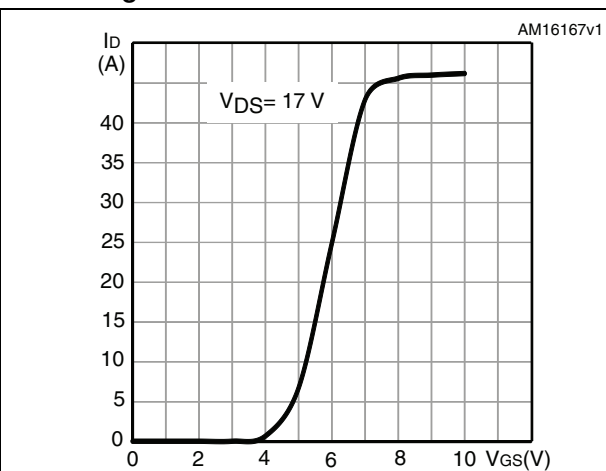


Figure 8. Gate charge vs gate-source voltage

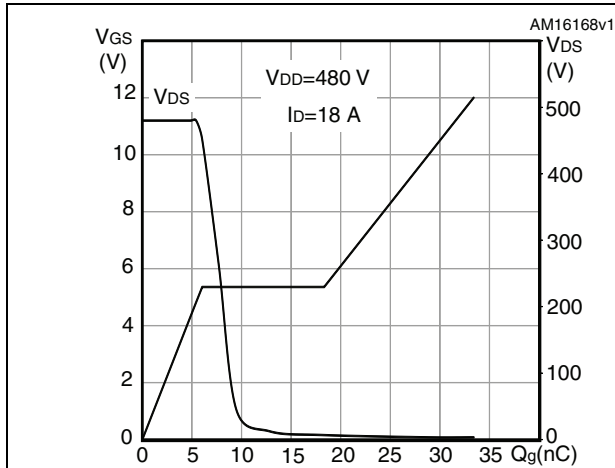


Figure 9. Static drain-source on-resistance

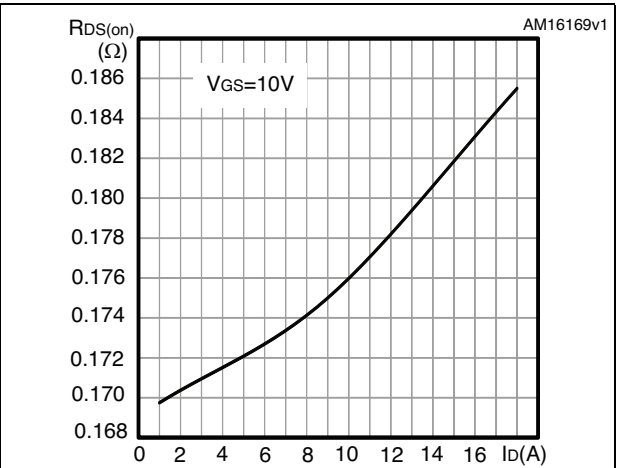


Figure 10. Capacitance variations

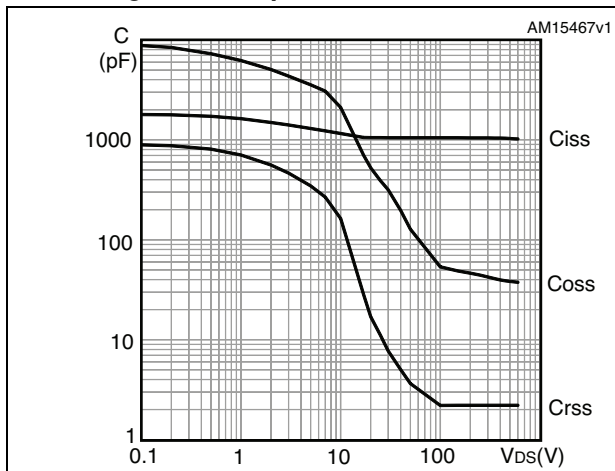


Figure 11. Output capacitance stored energy

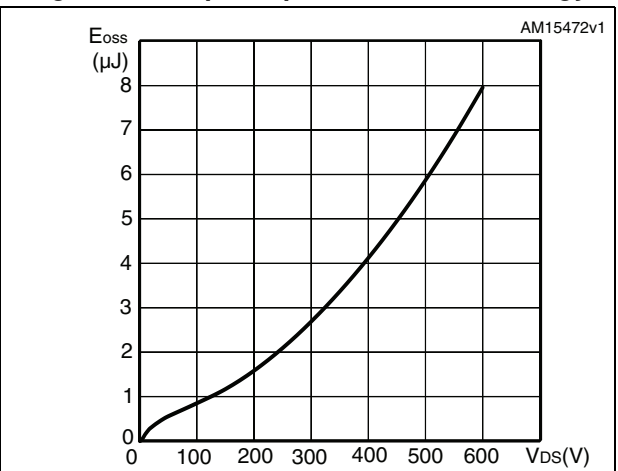


Figure 12. Normalized gate threshold voltage vs temperature

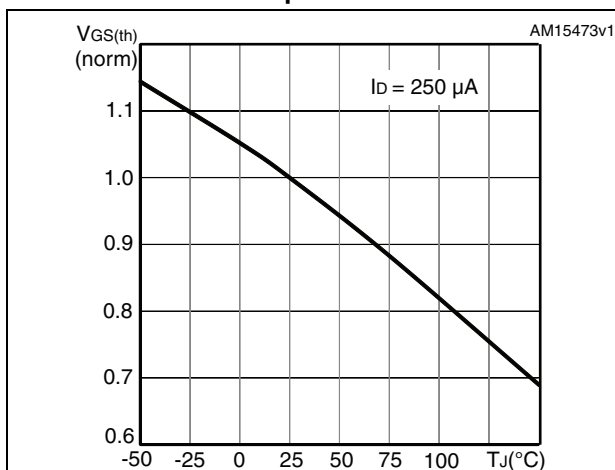


Figure 13. Normalized on-resistance vs temperature

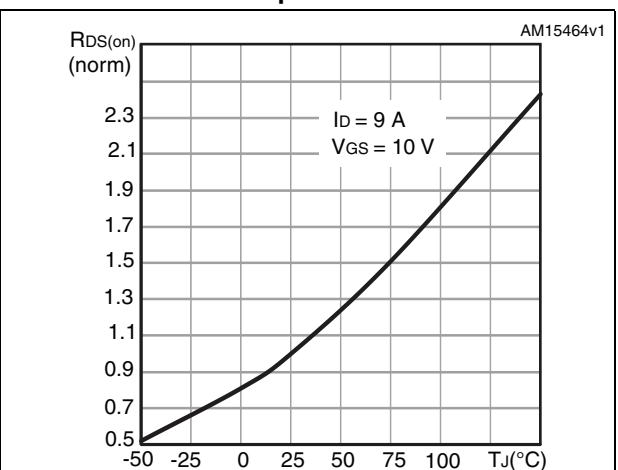


Figure 14. Source-drain diode forward characteristics

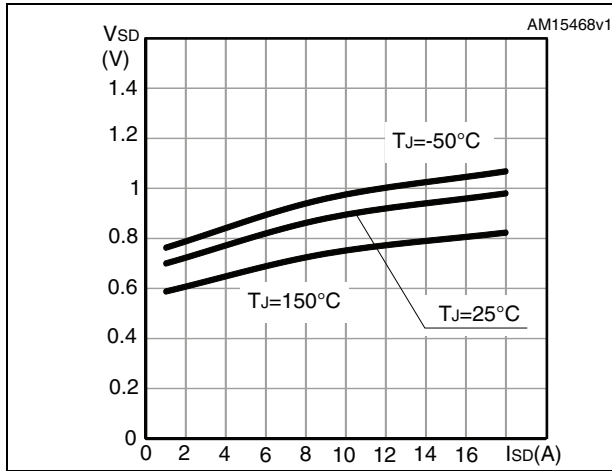
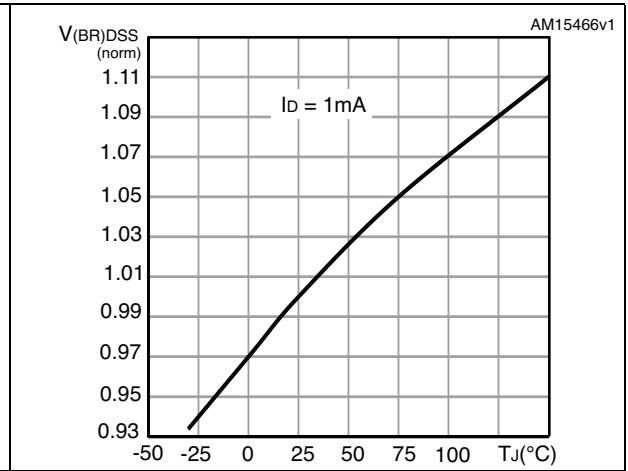


Figure 15. Normalized V<sub>(BR)DSS</sub> vs temperature





### 3 Test circuits

Figure 16. Switching times test circuit for resistive load

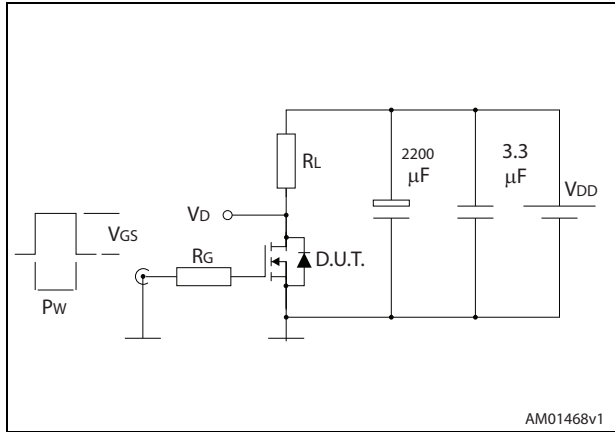


Figure 17. Gate charge test circuit

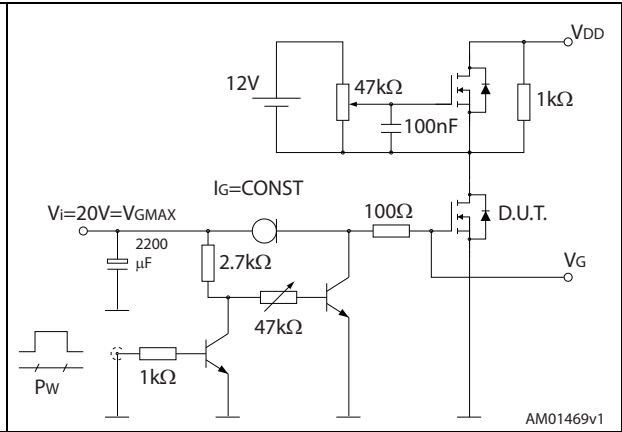


Figure 18. Test circuit for inductive load switching and diode recovery times

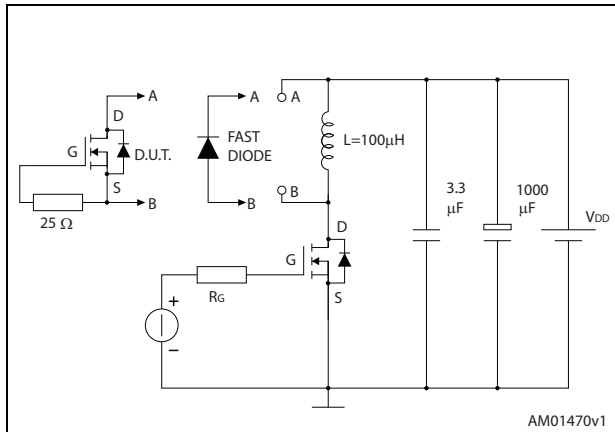


Figure 19. Unclamped inductive load test circuit

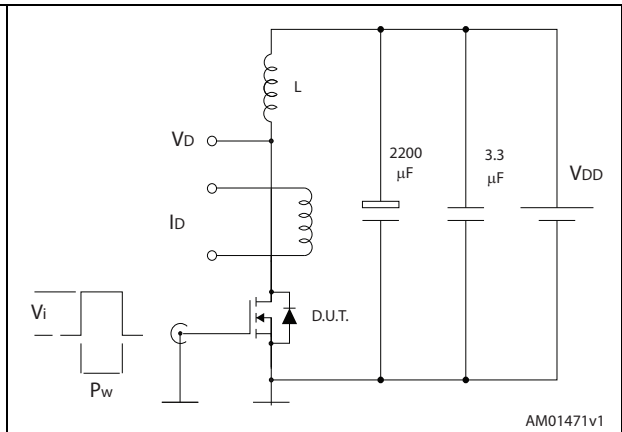


Figure 20. Unclamped inductive waveform

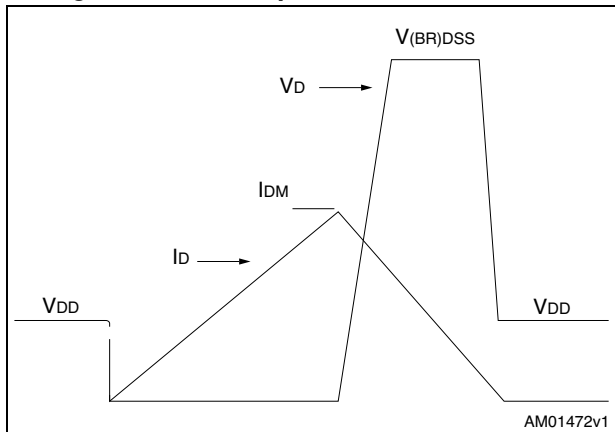
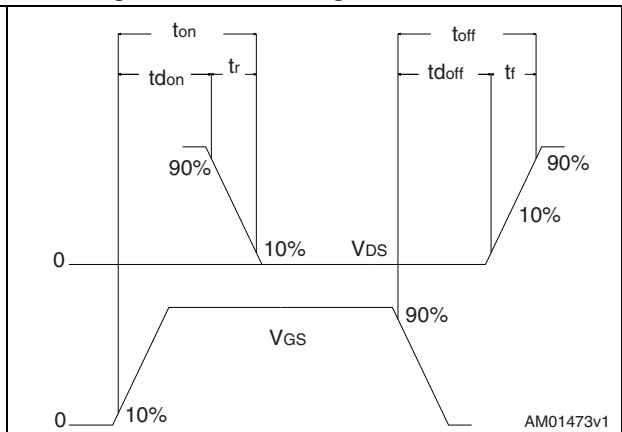


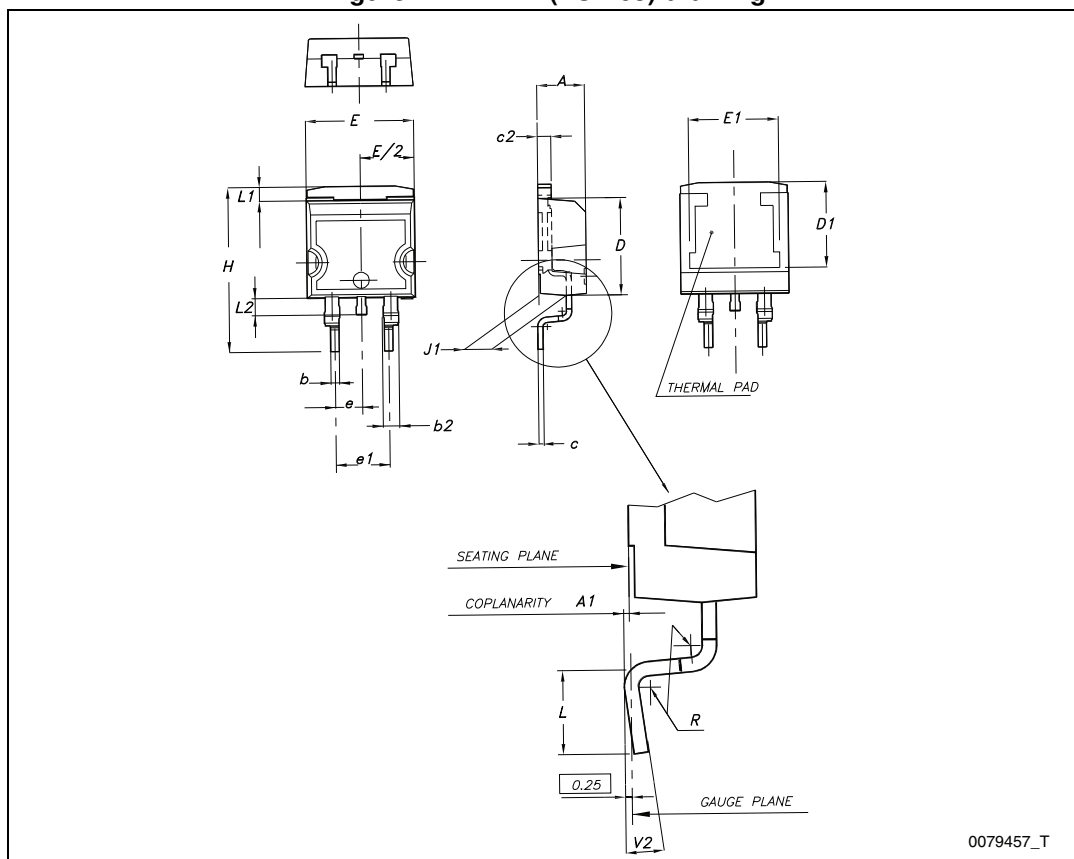
Figure 21. Switching time waveform



## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

Figure 22. D<sup>2</sup>PAK (TO-263) drawing

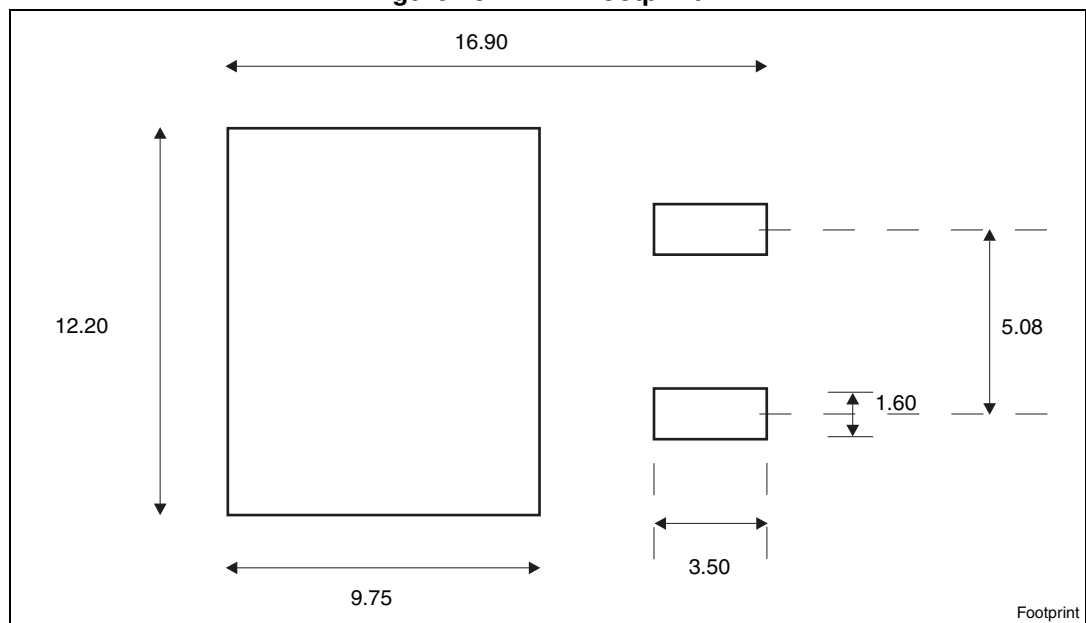


0079457\_T

Table 9. D<sup>2</sup>PAK (TO-263) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50		
E	10		10.40
E1	8.50		
e		2.54	
e1	4.88		5.28
H	15		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.4	
V2	0°		8°

Figure 23. D<sup>2</sup>PAK footprint<sup>(a)</sup>



a. All dimension are in millimeters

Figure 24. TO-220 type A drawing

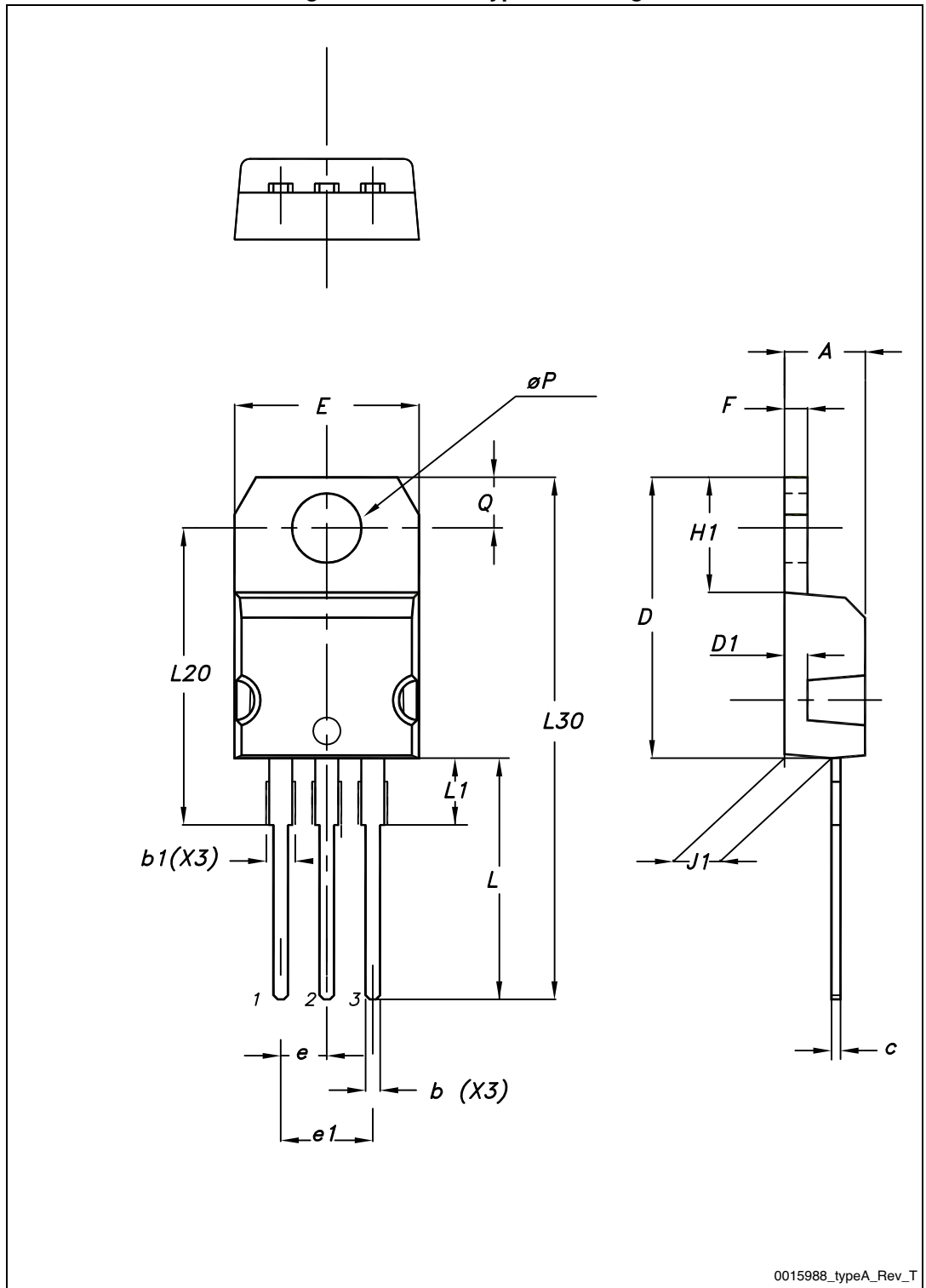


Table 10. TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
ØP	3.75		3.85
Q	2.65		2.95

Figure 25. TO-247 drawing

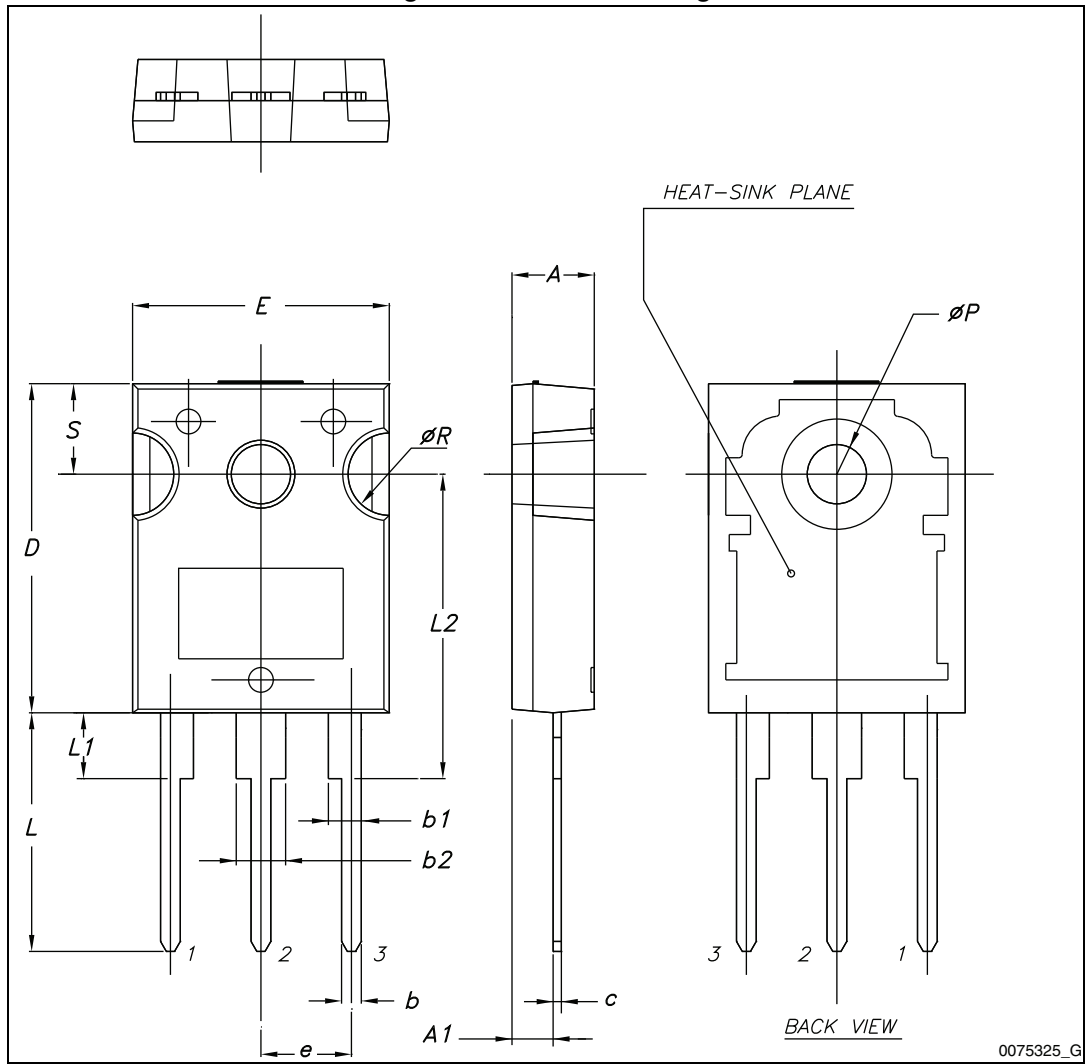




Table 11. TO-247 mechanical data

Dim.	mm.		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70

# 5 Packaging mechanical data

Figure 26. Tape

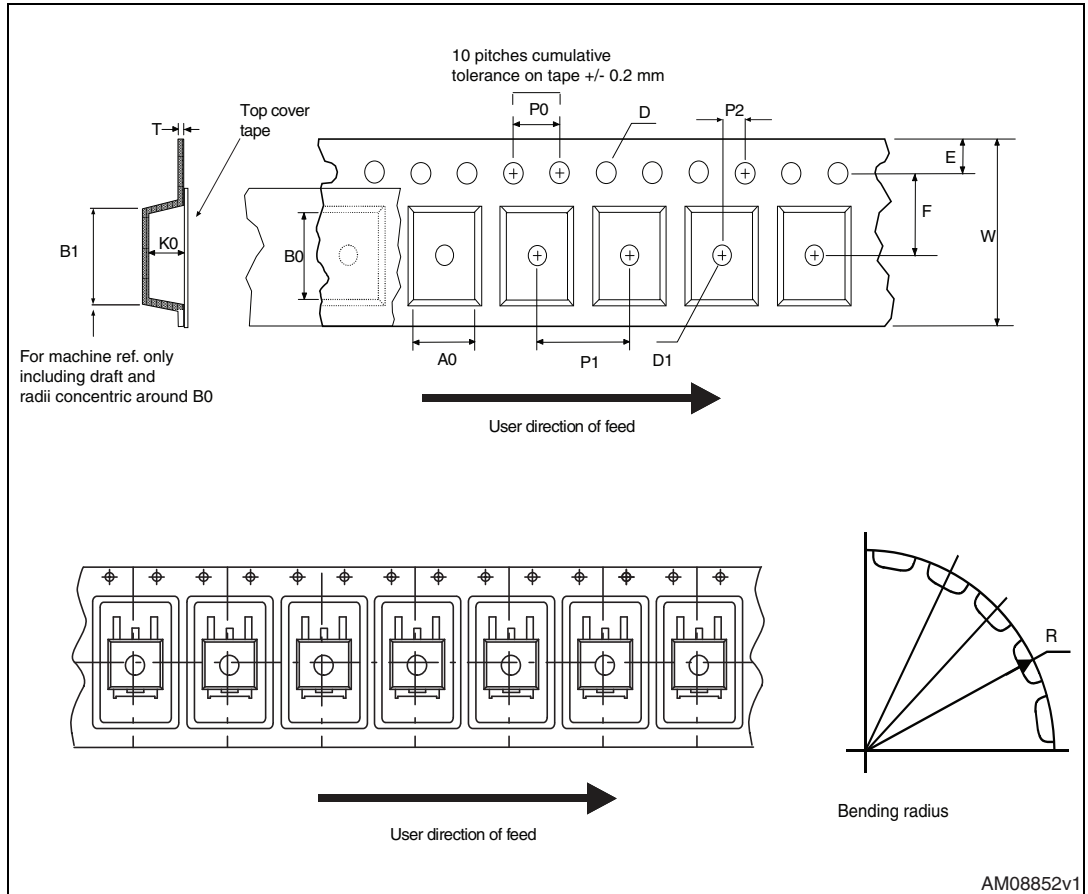


Figure 27. Reel

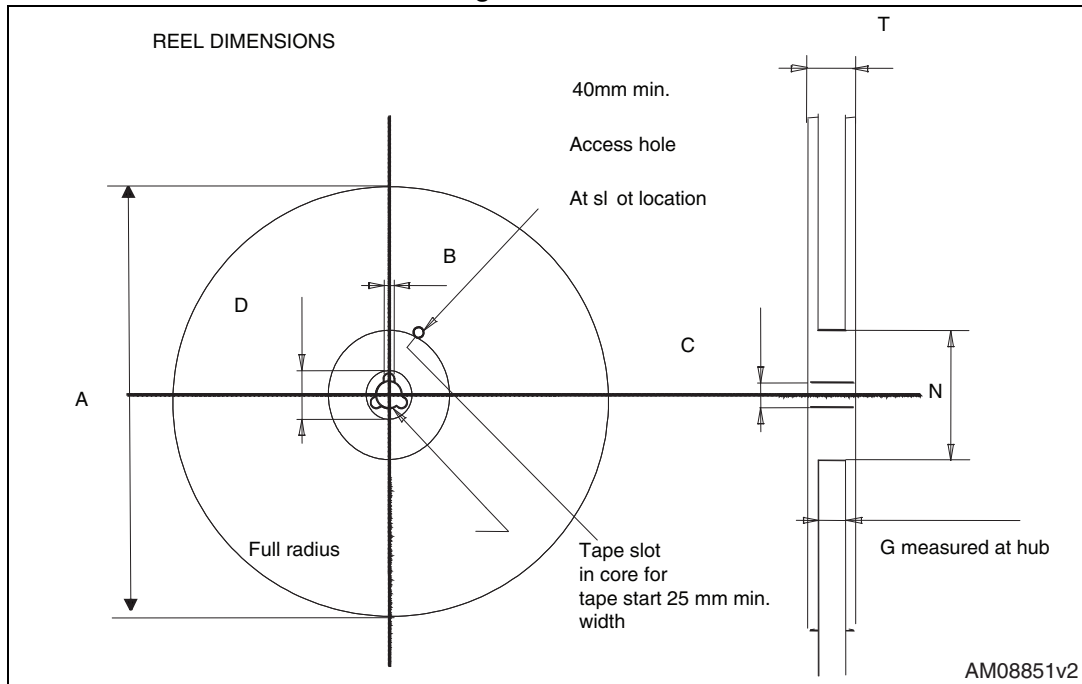


Table 12. D<sup>2</sup>PAK (TO-263) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base qty		1000
P2	1.9	2.1	Bulk qty		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

## 6 Revision history

**Table 13. Document revision history**

Date	Revision	Changes
12-Nov-2013	1	First release.
17-Jan-2014	2	<ul style="list-style-type: none"><li>– Document status promoted from preliminary data to production data</li><li>– Modified: <math>dv/dt</math> (peak diode recovery voltage slope) value in <a href="#">Table 2</a></li><li>– Modified: <math>I_{AR}</math> value in <a href="#">Table 4</a></li><li>– Modified: <math>I_{DSS}</math> and <math>V_{GS(th)}</math> values in <a href="#">Table 5</a></li><li>– Minor text changes</li></ul>
03-Mar-2014	3	<ul style="list-style-type: none"><li>– Modified: <math>I_{AR}</math> value in <a href="#">Table 4</a></li><li>– Added: <a href="#">note 1.:</a> <i>Limited by maximum junction temperature</i></li><li>– Minor text changes</li></ul>

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