

N-channel 950 V, 0.275 Ω typ., 17.5 A MDmesh™ K5 Power MOSFET in a TO-247 long leads package

Datasheet - production data

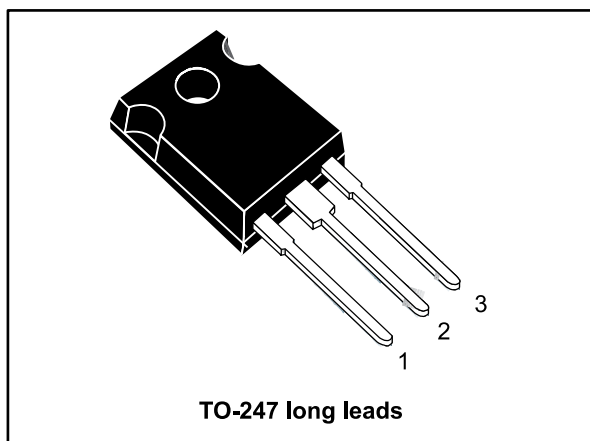
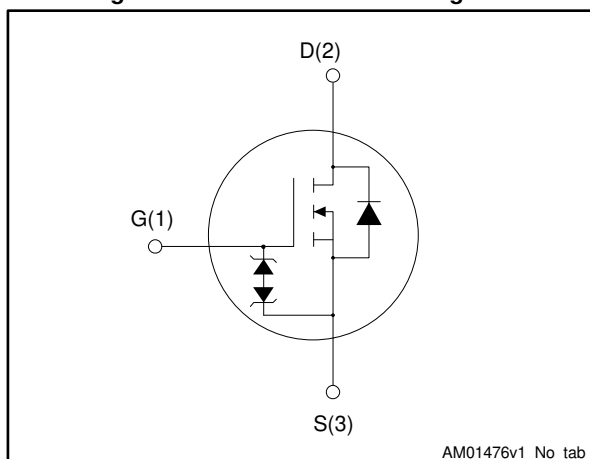


Figure 1: Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D	P_{TOT}
STWA20N95K5	950 V	0.330 Ω	17.5 A	250 W

- Industry's lowest $R_{DS(on)}$ x area
- Industry's best FoM (figure of merit)
- Ultra-low gate charge
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

This very high voltage N-channel Power MOSFET is designed using MDmesh™ K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

Table 1: Device summary

Order code	Marking	Package	Packing
STWA20N95K5	20N95K5	TO-247 long leads	Tube

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V _{GS}	Gate-source voltage	±30	V
I _D	Drain current (continuous) at T _C = 25 °C	17.5	A
I _D	Drain current (continuous) at T _C = 100 °C	11	A
I _D ⁽¹⁾	Drain current (pulsed)	70	A
P _{TOT}	Total dissipation at T _C = 25 °C	250	W
ESD	Gate-source human body model (R= 1.5 kΩ, C = 100 pF)	2	kV
dv/dt ⁽²⁾	Peak diode recovery voltage slope	6	V/ns
dv/dt ⁽³⁾	MOSFET dv/dt ruggedness	50	
T _j	Operating junction temperature range	-55 to 150	°C
T _{stg}	Storage temperature range		

Notes:

(1)Pulse width limited by safe operating area.

(2)I_{SD} ≤ 17.5 A, di/dt ≤ 100 A/μs; V_{DS} peak ≤ V_{(BR)DSS}

(3)V_{DS} ≤ 760 V

Table 3: Thermal data

Symbol	Parameter	Value	Unit
R _{thj-case}	Thermal resistance junction-case	0.5	°C/W
R _{thj-amb}	Thermal resistance junction-ambient	50	°C/W

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I _{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T _{jmax} .)	6	A
E _{AS}	Single pulse avalanche energy (starting T _j = 25 °C, I _D = I _{AR} , V _{DD} = 50 V)	200	mJ

2 Electrical characteristics

$T_C = 25\text{ }^\circ\text{C}$ unless otherwise specified

Table 5: On/off-state

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$, $I_D = 1\text{ mA}$	950			V
I_{DSS}	Zero-gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 950\text{ V}$			1	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 950\text{ V}$ $T_C = 125\text{ }^\circ\text{C}$ ⁽¹⁾			50	μA
I_{GSS}	Gate body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 20\text{ V}$			± 10	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 100\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 9\text{ A}$		0.275	0.330	Ω

Notes:

⁽¹⁾Defined by design, not subject to production test

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 100\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	1550	-	pF
C_{oss}	Output capacitance		-	140	-	pF
C_{rss}	Reverse transfer capacitance		-	1	-	pF
$C_{o(er)}$ ⁽¹⁾	Equivalent capacitance energy related	$V_{GS} = 0\text{ V}$, $V_{DS} = 0\text{ to }760\text{ V}$	-	65	-	pF
$C_{o(tr)}$ ⁽²⁾	Equivalent capacitance time related			178	-	pF
R_g	Intrinsic gate resistance	$f = 1\text{ MHz}$, $I_D = 0\text{ A}$	-	3.5	-	Ω
Q_g	Total gate charge	$V_{DD} = 760\text{ V}$, $I_D = 17.5\text{ A}$, $V_{GS} = 10\text{ V}$ (see Figure 16: "Test circuit for gate charge behavior")	-	48	-	nC
Q_{gs}	Gate-source charge		-	9	-	nC
Q_{gd}	Gate-drain charge		-	32.5	-	nC

Notes:

⁽¹⁾ $C_{o(er)}$ is a constant capacitance value that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

⁽²⁾ $C_{o(tr)}$ is a constant capacitance value that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 475 \text{ V}$, $I_D = 9 \text{ A}$, $R_G = 4.7 \Omega$ $V_{GS} = 10 \text{ V}$ (see <i>Figure 15: "Test circuit for resistive load switching times"</i> and <i>Figure 20: "Switching time waveform"</i>)	-	18	-	ns
t_r	Rise time		-	9	-	ns
$t_{d(off)}$	Turn-off delay time		-	65	-	ns
t_f	Fall time		-	18	-	ns

Table 8: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		17.5	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		70	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 17.5 \text{ A}$, $V_{GS} = 0 \text{ V}$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 17.5 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$, $V_{DD} = 60 \text{ V}$ (see <i>Figure 17: "Test circuit for inductive load switching and diode recovery times"</i>)	-	513		ns
Q_{rr}	Reverse recovery charge		-	12		μC
I_{RRM}	Reverse recovery current		-	46		A
t_{rr}	Reverse recovery time	$I_{SD} = 17.5 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 60 \text{ V}$, $T_j = 150 \text{ }^\circ\text{C}$ (see <i>Figure 17: "Test circuit for inductive load switching and diode recovery times"</i>)	-	670		ns
Q_{rr}	Reverse recovery charge		-	15		μC
I_{RRM}	Reverse recovery current		-	44		A

Notes:

(1)Pulse width limited by safe operating area

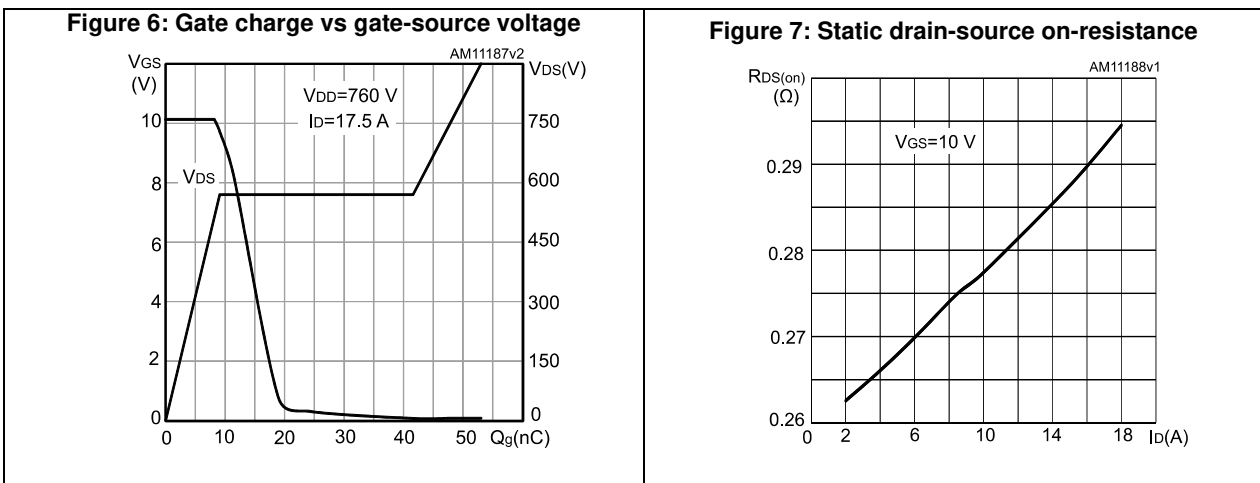
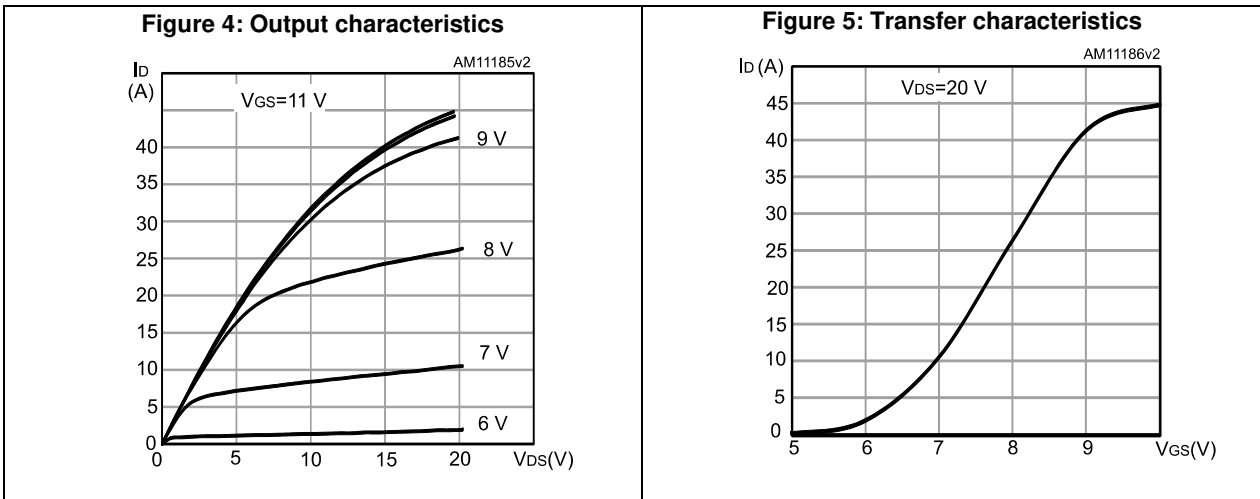
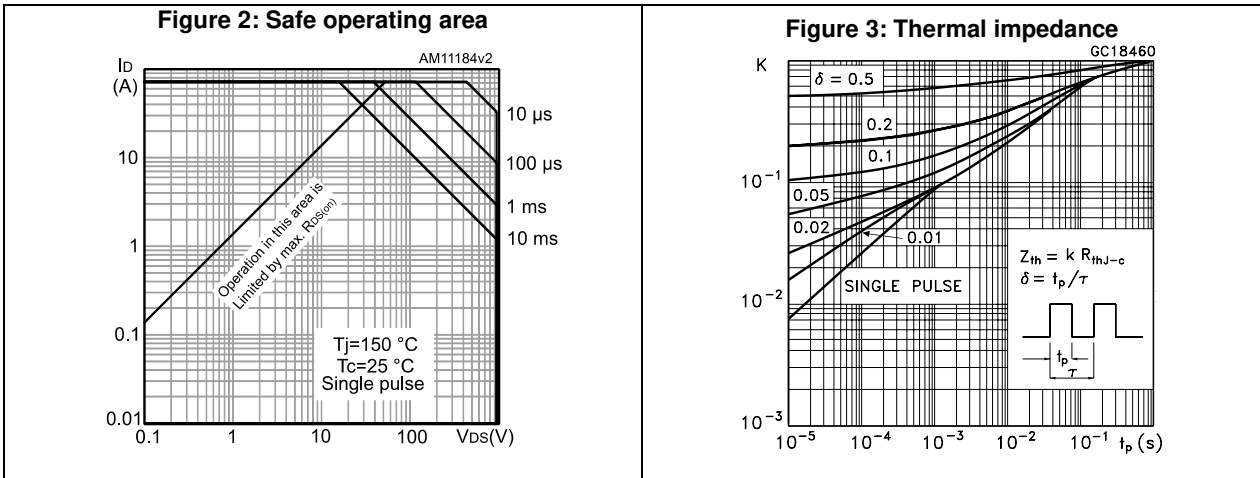
(2)Pulsed: pulse duration = 300 μs , duty cycle 1.5%

Table 9: Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR) GSO}$	Gate-source breakdown voltage	$I_{GS} = \pm 1 \text{ mA}$, $I_D = 0 \text{ A}$	30	-	-	V

The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.

2.1 Electrical characteristics (curves)



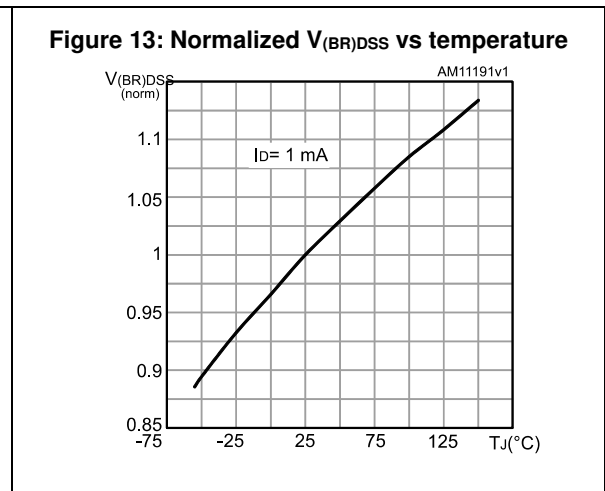
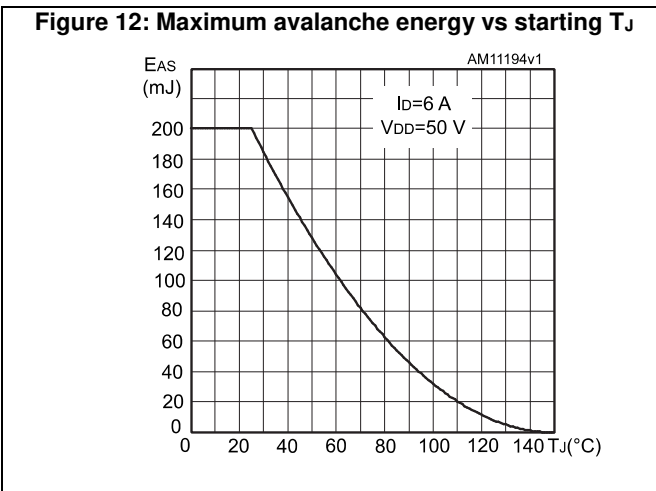
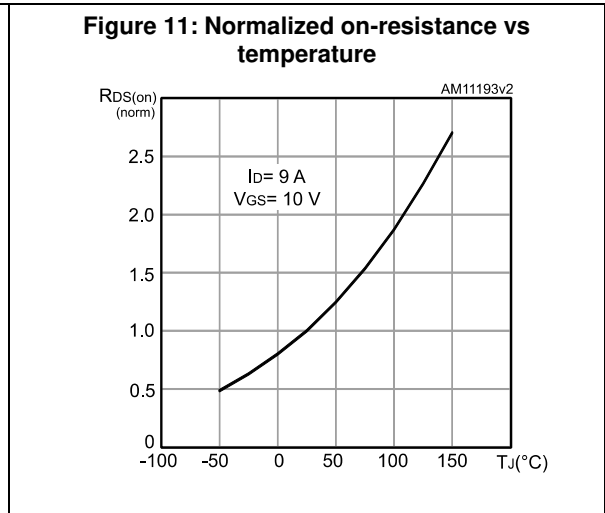
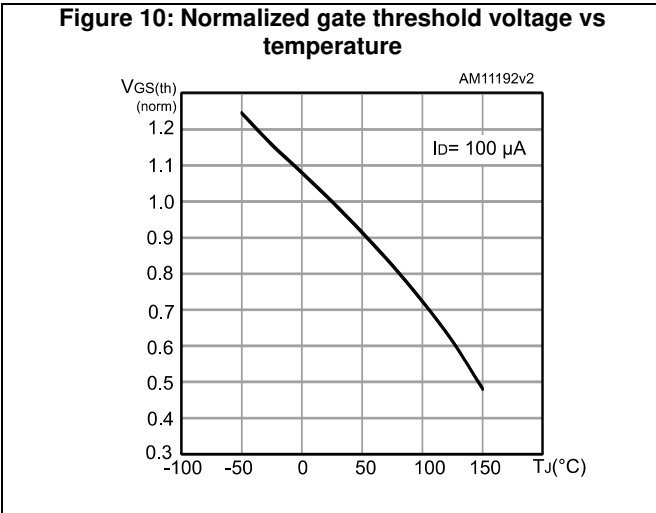
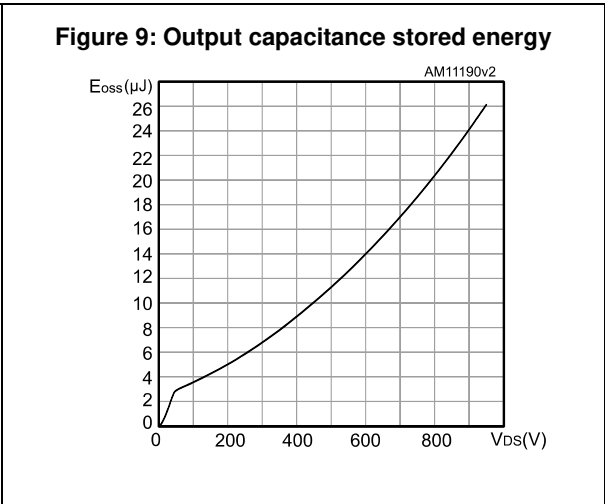
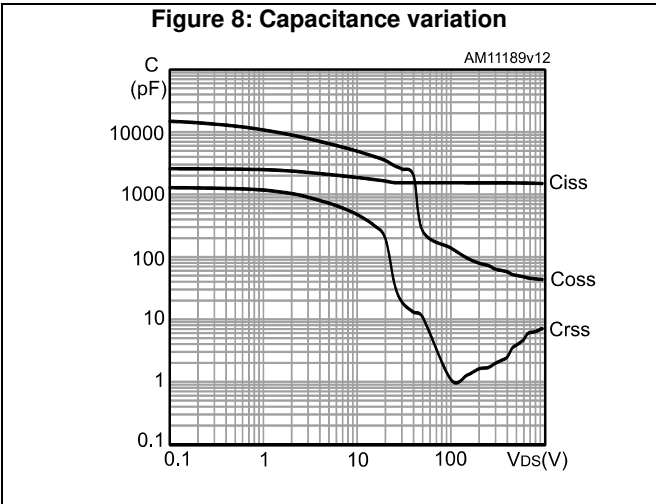
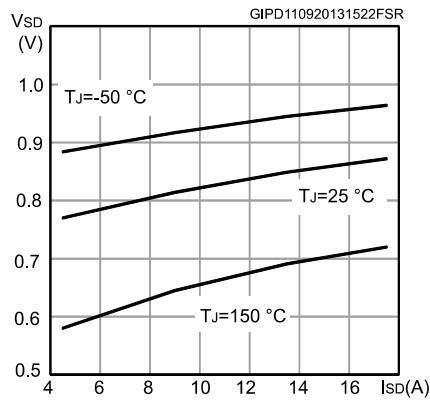
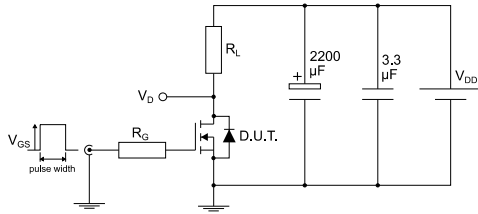


Figure 14: Source-drain diode forward characteristics



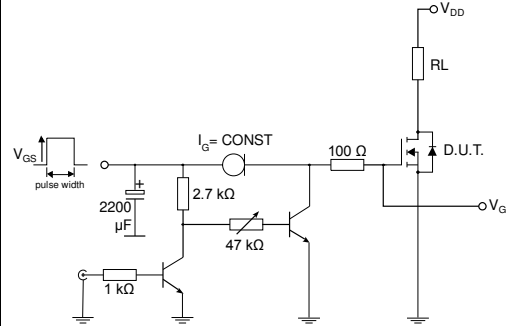
3 Test circuits

Figure 15: Test circuit for resistive load switching times



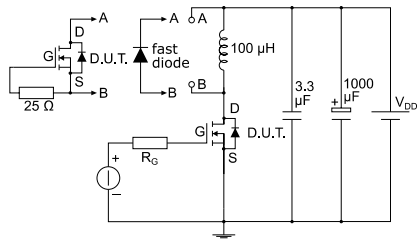
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Figure 16: Test circuit for gate charge behavior



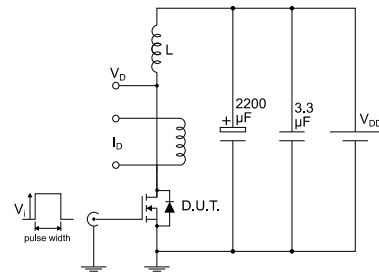
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Figure 17: Test circuit for inductive load switching and diode recovery times



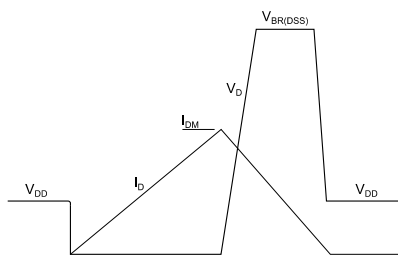
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Figure 18: Unclamped inductive load test circuit



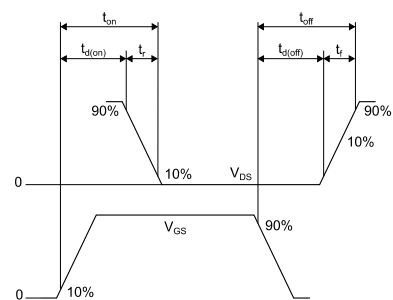
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Figure 19: Unclamped inductive waveform



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Figure 20: Switching time waveform



AM01473v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 TO-247 long leads package information

Figure 21: TO-247 long leads package outline

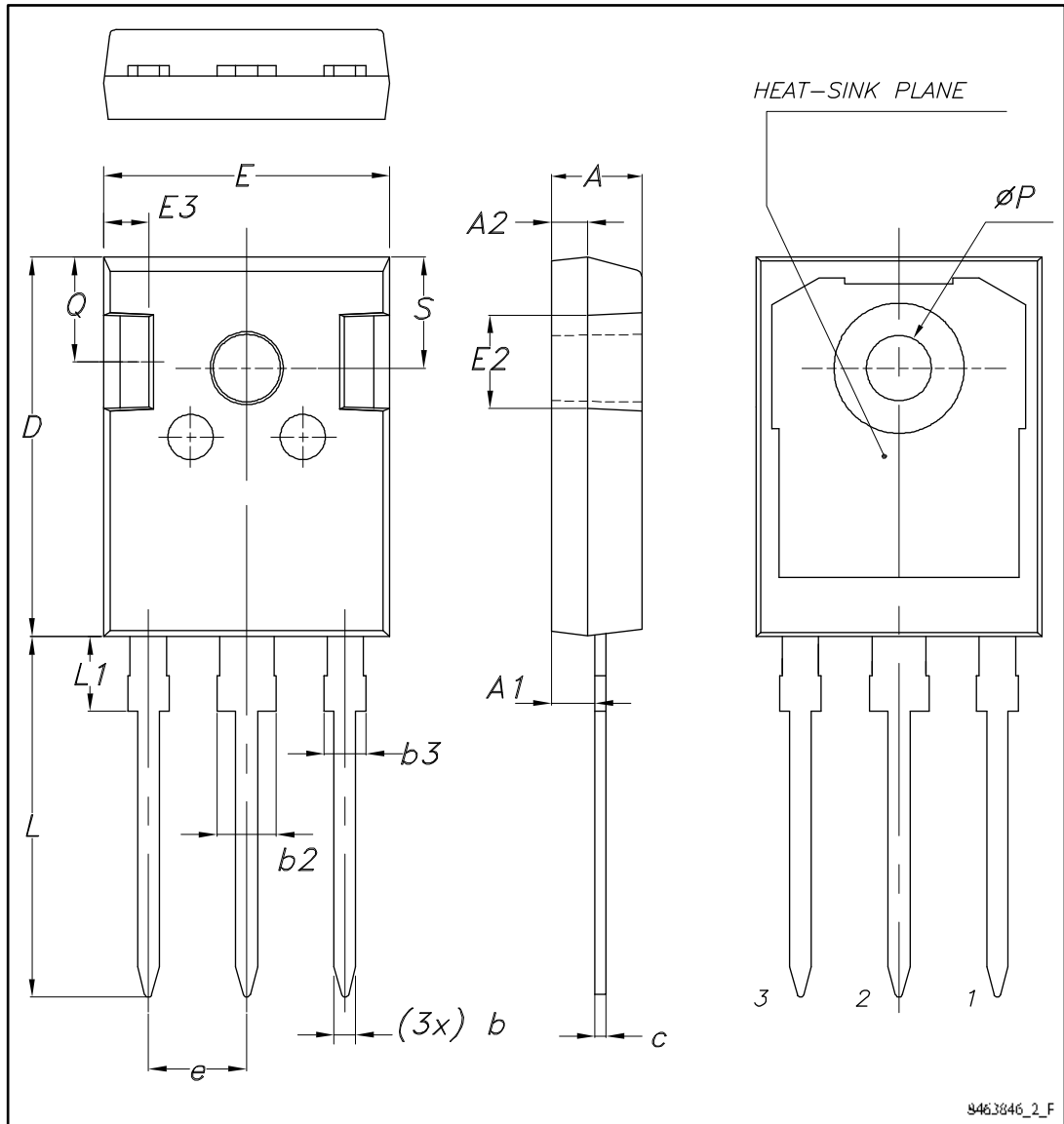


Table 10: TO-247 long leads package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.90	5.00	5.10
A1	2.31	2.41	2.51
A2	1.90	2.00	2.10
b	1.16		1.26
b2			3.25
b3			2.25
c	0.59		0.66
D	20.90	21.00	21.10
E	15.70	15.80	15.90
E2	4.90	5.00	5.10
E3	2.40	2.50	2.60
e	5.34	5.44	5.54
L	19.80	19.92	20.10
L1			4.30
P	3.50	3.60	3.70
Q	5.60		6.00
S	6.05	6.15	6.25

5 Revision history

Table 11: Document revision history

Date	Revision	Changes
21-Nov-2013	1	First release.
16-Jan-2017	2	Datasheet promoted from preliminary to production data. Modified: title. Updated: features, applications and description in cover page. Minor text changes in <i>Section 1: "Electrical ratings"</i> and <i>Section 2: "Electrical characteristics"</i> . Updated <i>Section 2.1: "Electrical characteristics (curves)"</i> . Updated <i>Section 4.1: "TO-247 long leads package information"</i> .

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