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CSD13383F4

SLPS517-DECEMBER 2014

CSD13383F4 12 V N-Channel FemtoFET™ MOSFET

1 Features

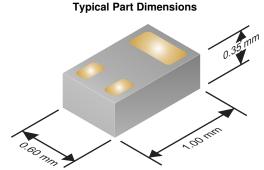
- Low On-Resistance
- Ultra Low Q_g and Q_{gd}
- Ultra-Small Footprint (0402 Case Size)
 - 1.0 mm × 0.6 mm
- Low Profile
 - 0.35 mm Height
- Integrated ESD Protection Diode
 - Rated > 2 kV HBM
 - Rated > 2 kV CDM
- Lead and Halogen Free
- RoHS Compliant

2 Applications

- Optimized for Load Switch Applications
- Optimized for General Purpose Switching Applications
- Single-Cell Battery Applications
- · Handheld and Mobile Applications

3 Description

This 37 m Ω , 12 V N-Channel FemtoFETTM MOSFET technology is designed and optimized to minimize the footprint in many handheld and mobile applications. This technology is capable of replacing standard small signal MOSFETs while providing at least a 60% reduction in footprint size.



Product Summary

T _A = 25°	c	TYPICAL VA	UNIT		
V _{DS}	Drain-to-Source Voltage 12				
Qg	Gate Charge Total (4.5 V)	2.0	nC		
Q _{gd}	Gate Charge Gate-to-Drain	0.6		nC	
D	Drain-to-Source On-Resistance	$V_{GS} = 2.5 V$	53	mΩ	
R _{DS(on)}	Drain-to-Source On-Resistance	$V_{GS} = 4.5 V$	37	1117	
V _{GS(th)}	Threshold Voltage	1.0		V	

Ordering Information⁽¹⁾

Device	Qty	Media	Package	Ship
CSD13383F4	3000	7-Inch	Femto (0402) 1.0 mm ×	Tape and
CSD13383F4T	250	Reel	0.6 mm SMD Lead Less	Reel

(1) For all available packages, see the orderable addendum at the end of the data sheet.

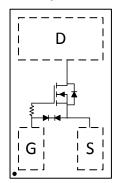
Absolute Maximum Ratings

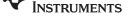
T _A = 25	°C	VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	12	V
V_{GS}	Gate-to-Source Voltage	±10	V
ID	Continuous Drain Current ⁽¹⁾	2.9	А
I _{DM}	Pulsed Drain Current ⁽¹⁾⁽²⁾	27	А
	Continuous Gate Clamp Current	25	mA
I _G	Pulsed Gate Clamp Current ⁽¹⁾⁽²⁾	250	ma
PD	Power Dissipation	500	mW
ESD	Human Body Model (HBM)	2	kV
Rating	Charged Device Model (CDM)	2	kV
T _J , T _{stg}	Operating Junction and Storage Temperature Range	-55 to 150	°C
E _{AS}	Avalanche Energy, single pulse I_D = 6.7, L = 0.1 mH, R_G = 25 Ω	2.2	mJ

(1) Typical $R_{\theta JA} = 250^{\circ}C/W$.

(2) Pulse duration $\leq 100 \ \mu$ s, duty cycle $\leq 1\%$.

Top View





EXAS

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4 Revision History

DATE	REVISION	NOTES
December 2014	*	Initial release.

5 Specifications

5.1 Electrical Characteristics

 $(T_A = 25^{\circ}C \text{ unless otherwise stated})$

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC	CHARACTERISTICS					
BV _{DSS}	Drain-to-Source Voltage	$V_{GS} = 0 V, I_{DS} = 250 \mu A$	12			V
I _{DSS}	Drain-to-Source Leakage Current	$V_{GS} = 0 V, V_{DS} = 9.6 V$			1	μA
I _{GSS}	Gate-to-Source Leakage Current	$V_{DS} = 0 V, V_{GS} = 10 V$			10	μA
V _{GS(th)}	Gate-to-Source Threshold Voltage	$V_{DS} = V_{GS}$, $I_{DS} = 250 \ \mu A$	0.70	1.00	1.25	V
Р	Drain to Course On Registeres	V _{GS} = 2.5 V, I _{DS} =0.5 A		53	65	mΩ
R _{DS(on)}	Drain-to-Source On-Resistance	V _{GS} = 4.5 V, I _{DS} =0.5 A		37	44	mΩ
g _{fs}	Transconductance	V _{DS} = 6 V, I _{DS} = 0.5 A		5.4		S
DYNAMI	C CHARACTERISTICS	•				
C _{iss}	Input Capacitance			224	291	pF
C _{oss}	Output Capacitance	$V_{GS} = 0 V, V_{DS} = 6 V, f = 1 MHz$		68	88	pF
C _{rss}	Reverse Transfer Capacitance			47	61	pF
R _G	Series Gate Resistance			240		Ω
Qg	Gate Charge Total (4.5 V)			2.0	2.6	nC
Q _{gd}	Gate Charge Gate-to-Drain			0.6		nC
Q _{gs}	Gate Charge Gate-to-Source	$V_{\rm DS} = 6 \ V, \ I_{\rm DS} = 0.5 \ A$		0.4		nC
Q _{g(th)}	Gate Charge at V _{th}			0.1		nC
Q _{oss}	Output Charge	$V_{DS} = 6 V, V_{GS} = 0 V$		0.9		nC
t _{d(on)}	Turn On Delay Time			39		ns
t _r	Rise Time	$V_{DS} = 6 V, V_{GS} = 4.5 V,$		123		ns
t _{d(off)}	Turn Off Delay Time	$I_{DS} = 0.5 \text{ Å}, R_G = 2 \Omega$		96		ns
t _f	Fall Time			315		ns
DIODE C	CHARACTERISTICS	+	· ·		ŀ	
V _{SD}	Diode Forward Voltage	I _{SD} = 0.5 A, V _{GS} = 0 V		0.7	1.0	V

5.2 Thermal Information

 $(T_A = 25^{\circ}C \text{ unless otherwise stated})$

	THERMAL METRIC	MIN	ТҮР	MAX	UNIT
Р	Junction-to-Ambient Thermal Resistance ⁽¹⁾		90		°C/W
R _{θJA}	Junction-to-Ambient Thermal Resistance ⁽²⁾		250		-0/10

(1) Device mounted on FR4 material with 1 inch² (6.45 cm²), 2 oz. (0.071 mm thick) Cu.

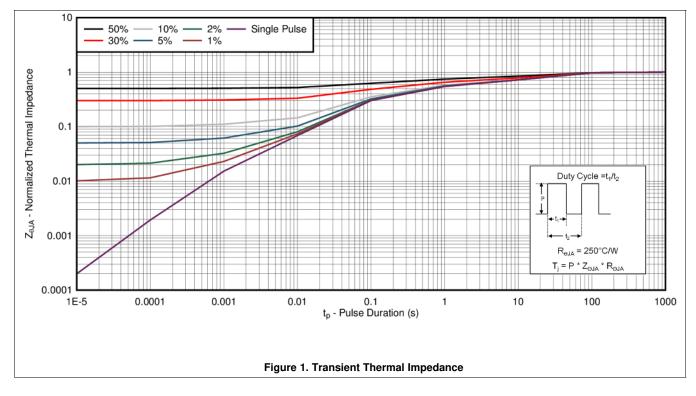
(2) Device mounted on FR4 material with minimum Cu mounting area.

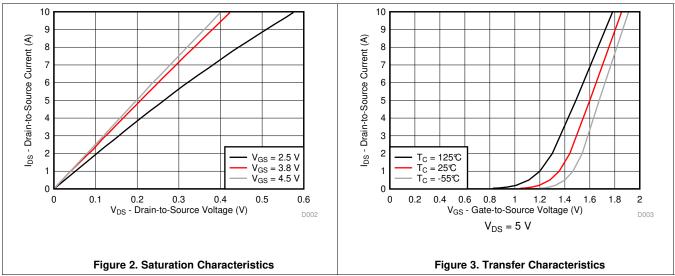
NSTRUMENTS

Texas

5.3 Typical MOSFET Characteristics

 $(T_A = 25^{\circ}C \text{ unless otherwise stated})$

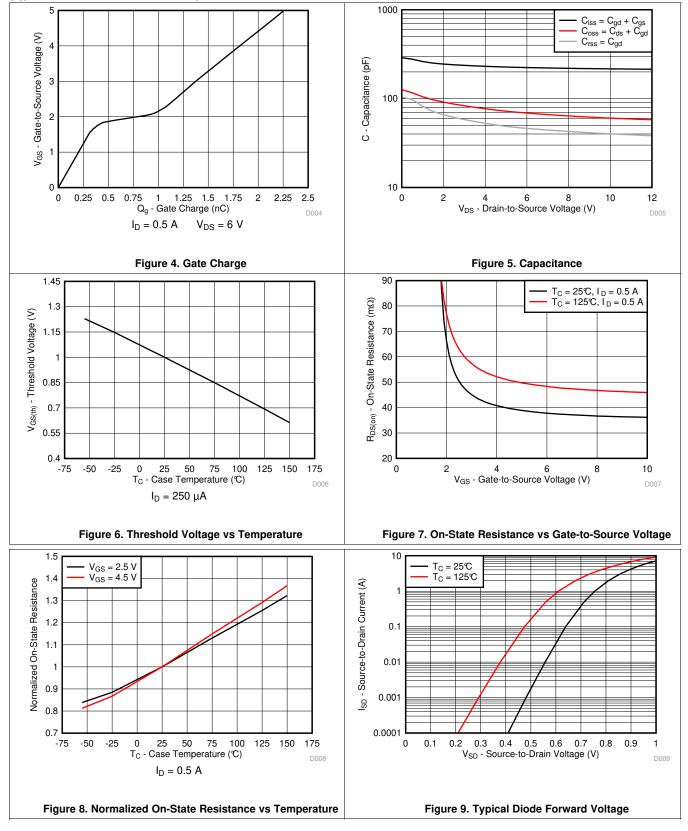






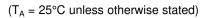
Typical MOSFET Characteristics (continued)

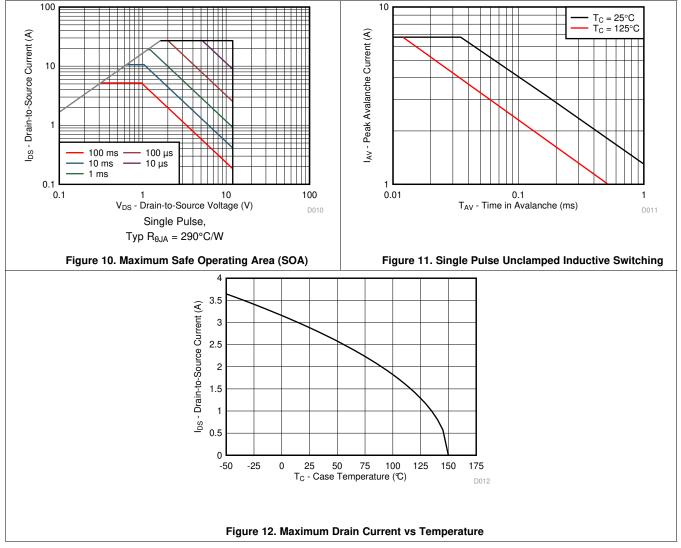
 $(T_A = 25^{\circ}C \text{ unless otherwise stated})$





Typical MOSFET Characteristics (continued)







6 Device and Documentation Support

6.1 Trademarks

FemtoFET is a trademark of Texas Instruments. All other trademarks are the property of their respective owners.

6.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

6.3 Glossary

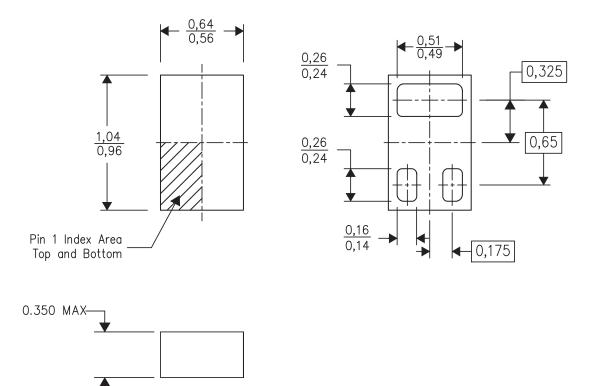
SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

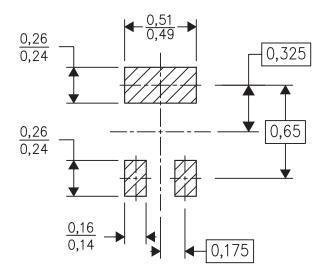
7.1 Mechanical Dimensions



- (1) All linear dimensions are in millimeters (dimensions and tolerancing per AME T14.5M-1994).
- (2) This drawing is subject to change without notice.
- (3) This package is a PB-free solder land design.

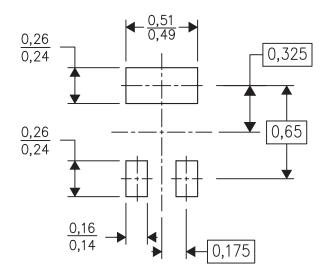


7.2 Recommended Minimum PCB Layout



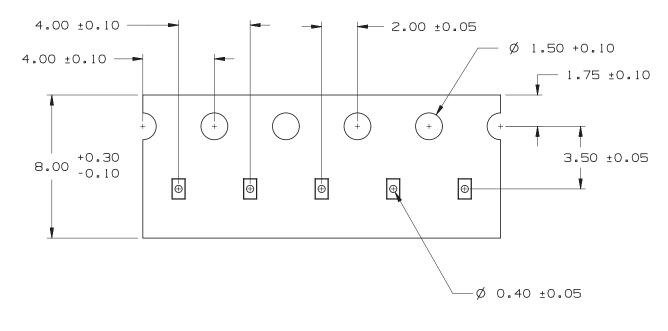
(1) All dimensions are in millimeters.

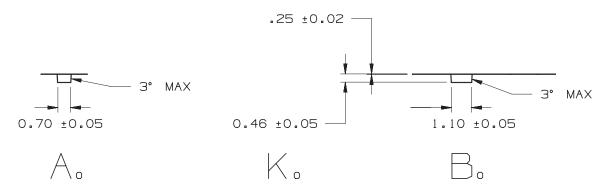
7.3 Recommended Stencil Pattern



(1) All dimensions are in millimeters.

7.4 CSD17381F4 Embossed Carrier Tape Dimensions





(1) Pin 1 is oriented in the top-right quadrant of the tape enclosure (quadrant 2), closest to the carrier tape sprocket holes.



14-Dec-2014

PACKAGING INFORMATION

Orderable Device	Status	Package Type	Package	Pins	Package	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking	Samples
	(1)		Drawing		Qty	(2)	(6)	(3)		(4/5)	
CSD13383F4	ACTIVE	PICOSTAR	YJC	3	3000	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM		GC	Samples
CSD13383F4T	ACTIVE	PICOSTAR	YJC	3	250	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM		GC	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between

the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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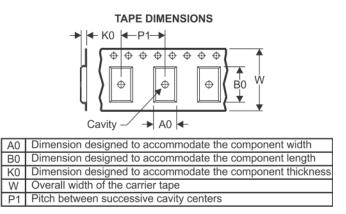
PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device		Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD13383F4	PICOST AR	YJC	3	3000	180.0	8.4	0.7	1.1	0.46	4.0	8.0	Q2

TEXAS INSTRUMENTS

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PACKAGE MATERIALS INFORMATION

13-Dec-2014



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD13383F4	PICOSTAR	YJC	3	3000	182.0	182.0	17.0

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