



# N-Channel Reduced $Q_g$ , Fast Switching MOSFET

PRODUCT SUMMARY						
V <sub>DS</sub> (V)	$R_{DS(on)}$ ( $\Omega$ )	I <sub>D</sub> (A)	Q <sub>g</sub> (Typ.)			
30	0.007 at V <sub>GS</sub> = 10 V	16	11			
	0.0095 at V <sub>GS</sub> = 4.5 V	13.5				

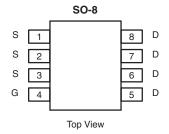
# **FEATURES**

- Halogen-free According to IEC 61249-2-21 Available
- TrenchFET<sup>®</sup> Gen II Power MOSFETs
- · PWM Optimized
- 100 % R<sub>g</sub> Tested

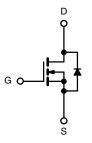


## **APPLICATIONS**

• DC/DC Conversion for PC



Ordering Information: Si4386DY-T1-E3 (Lead (Pb)-free) Si4386DY-T1-GE3 (Lead (Pb)-free and Halogen-free)



N-Channel MOSFET

<b>ABSOLUTE MAXIMUM RATINGS</b>	$T_A = 25$ °C, unles	ss otherwise n	oted		
Parameter		Symbol	10 s	Steady State	Unit
Drain-Source Voltage		V <sub>DS</sub>	30		V
Gate-Source Voltage		$V_{GS}$	± 20		V
Continuous Proin Current /T = 150 °C\a	T <sub>A</sub> = 25 °C	I <sub>D</sub>	16	11	
Continuous Drain Current (T <sub>J</sub> = 150 °C) <sup>a</sup>	T <sub>A</sub> = 70 °C		13	9	
Pulsed Drain Current		I <sub>DM</sub>	± 50		Α
Continuous Source Current (Diode Conduction) <sup>a</sup>		I <sub>S</sub>	2.8	1.3	
Single Pulse Avalanche Current	L = 0.1 mH	I <sub>AS</sub>			I
Avalanche Energy	L = 0.111111	E <sub>AS</sub>			mJ
Manian and Danier Disable attends	T <sub>A</sub> = 25 °C	- P <sub>D</sub>	3.1	1.47	W
Maximum Power Dissipation <sup>a</sup>	T <sub>A</sub> = 70 °C	' D	2	0.95	VV
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stq</sub>	- 55	5 to 150	°C

THERMAL RESISTANCE RATINGS						
Parameter	Symbol	Typical	Maximum	Unit		
Maximum Loration to Austinut (MOOFFT)	t ≤ 10 s	R <sub>thJA</sub>	34	40		
Maximum Junction-to-Ambient (MOSFET) <sup>a</sup>	Steady State	' 'thJA	71	85	°C/W	
Maximum Junction-to-Foot (Drain)	Steady State	$R_{thJF}$	18	22		

Notes

a. Surface Mounted on 1" x 1" FR4 board.

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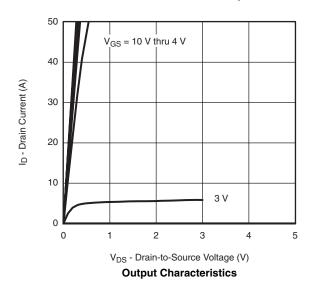
MOSFET SPECIFICATIONS T <sub>J</sub> = 25 °C, unless otherwise noted							
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static			•	•			
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	1.5	2.0	2.5	V	
Gate-Body Leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA	
Zava Cata Valtaga Drain Current	I <sub>DSS</sub>	$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}$			1		
Zero Gate Voltage Drain Current		$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 70 ^{\circ}\text{C}$	$_{S} = 0 \text{ V}, T_{J} = 70 ^{\circ}\text{C}$ 10		10	μΑ	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	40			Α	
	В	$V_{GS} = 10 \text{ V}, I_D = 16 \text{ A}$		0.0058	0.007	0	
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	$V_{GS} = 4.5 \text{ V}, I_D = 13.5 \text{ A}$		0.0078	0.0095	Ω	
Forward Transconductance <sup>a</sup>	9 <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 16 A		51		S	
Diode Forward Voltage <sup>a</sup>	$V_{SD}$	$I_S = 2.8 \text{ A}, V_{GS} = 0 \text{ V}$		0.75	1.1	V	
Dynamic <sup>b</sup>	L		<u>'</u>	•	l .		
Total Gate Charge	$Q_g$			11	18		
Gate-Source Charge	$Q_{gs}$ $V_{DS} = 1$	$V_{DS} = 15 \text{ V}, V_{GS} = 4.5 \text{ V}, I_{D} = 16 \text{ A}$		5.8		nC	
Gate-Drain Charge	Q <sub>gd</sub>			3.0			
Gate Resistance	$R_g$		0.8	1.7	2.5	Ω	
Turn-On Delay Time	t <sub>d(on)</sub>			12	18		
Rise Time	t <sub>r</sub>	$V_{DD}$ = 15 V, $R_L$ = 15 $\Omega$		9	14		
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_{d(off)}$ $I_{D} \cong 1 \text{ A, V}_{GEN} = 10 \text{ V, R}_{g} = 6 \Omega$		35	53	ns	
Fall Time	t <sub>f</sub>			10	15		
Source-Drain Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 2.8 A, dI/dt = 100 A/μs		25	50		

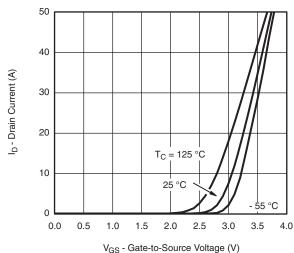
### Notes:

- a. Pulse test; pulse width  $\leq$  300  $\mu s,$  duty cycle  $\leq$  2 %.
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

# TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted





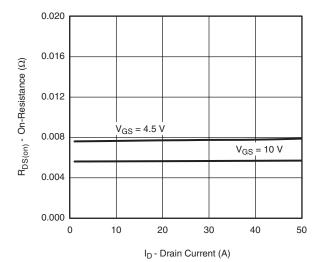
Transfer Characteristics



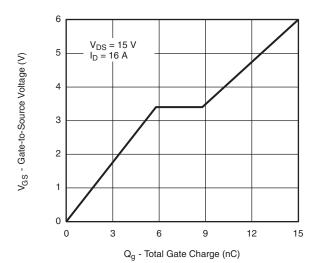




# TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



On-Resistance vs. Drain Current



T<sub>J</sub> = 150 °C 10 T<sub>J</sub> = 25 °C

**Gate Charge** 

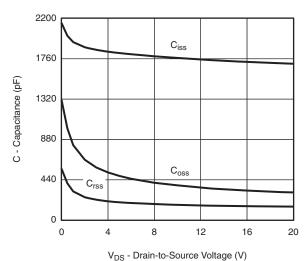
 $V_{SD}$  - Source-to-Drain Voltage (V) Source-Drain Diode Forward Voltage

0.6

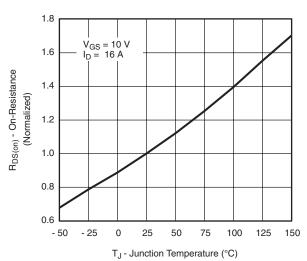
0.8

1.2

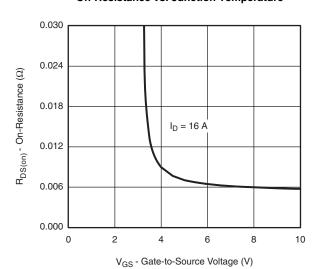
1.0







On-Resistance vs. Junction Temperature



On-Resistance vs. Gate-to-Source Voltage

0.00

0.2

0.4

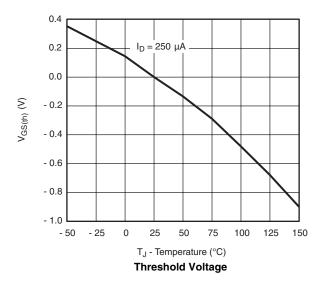
60

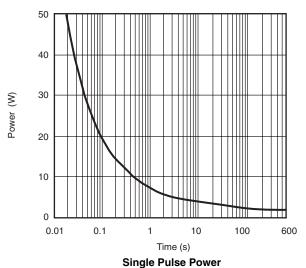
I<sub>S</sub> - Source Current (A)

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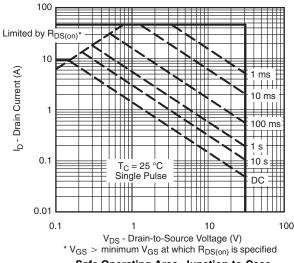
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# TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

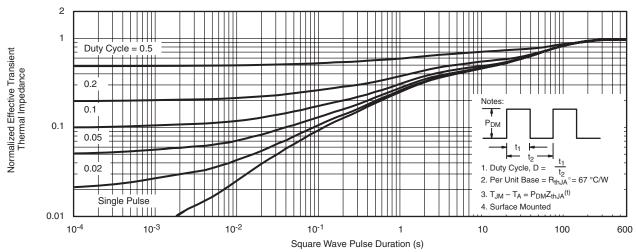




Single Pulse Power



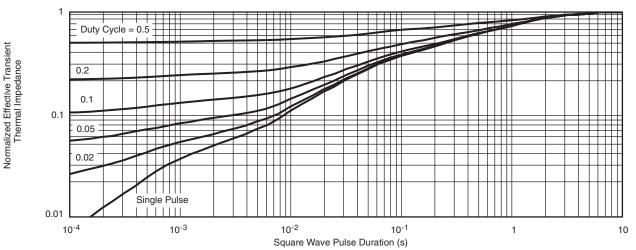
Safe Operating Area, Junction-to-Case



Normalized Thermal Transient Impedance, Junction-to-Ambient



# TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



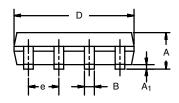
Normalized Thermal Transient Impedance, Junction-to-Foot

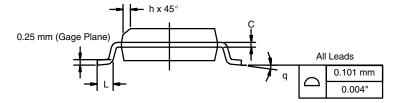
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SOIC (NARROW): 8-LEAD JEDEC Part Number: MS-012







	MILLIMETERS INCHE			HES		
DIM	Min	Max	Min	Max		
Α	1.35	1.75	0.053	0.069		
A <sub>1</sub>	0.10	0.20	0.004	0.008		
В	0.35	0.51	0.014	0.020		
С	0.19	0.25	0.0075	0.010		
D	4.80	5.00	0.189	0.196		
Е	3.80	4.00	0.150	0.157		
е	1.27 BSC		0.050	0.050 BSC		
Н	5.80	6.20	0.228	0.244		
h	0.25	0.50	0.010	0.020		
L	0.50	0.93	0.020	0.037		
q	0°	8°	0°	8°		
S	0.44	0.64	0.018	0.026		
ECN: C-06527-Rev. I. 11-Sep-06						

DWG: 5498

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# APPLICATION NOTE



# **RECOMMENDED MINIMUM PADS FOR SO-8**



Recommended Minimum Pads Dimensions in Inches/(mm)

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