

## P-Channel 20-V (D-S) MOSFET

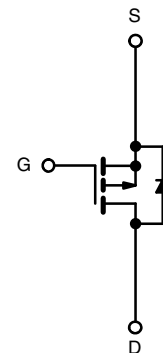
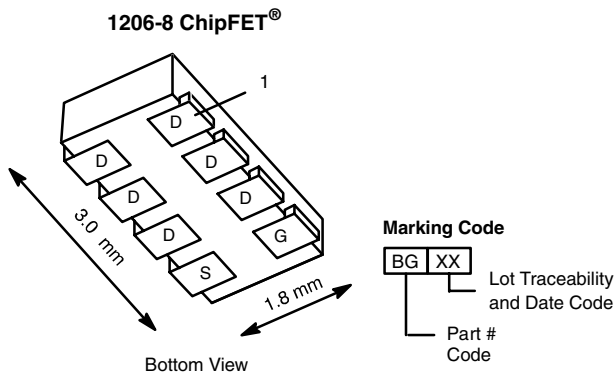
PRODUCT SUMMARY		
$V_{DS}$ (V)	$R_{DS(on)}$ ( $\Omega$ )	$I_D$ (A)
- 20	0.076 at $V_{GS} = - 4.5$ V	- 4.8
	0.110 at $V_{GS} = - 2.5$ V	- 4.0
	0.160 at $V_{GS} = - 1.8$ V	- 3.3

### FEATURES

- Halogen-free According to IEC 61249-2-21 Available
- TrenchFET® Power MOSFETs: 1.8 V Rated



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**  
Available



P-Channel MOSFET

**Ordering Information:** Si5447DC-T1-E3 (Lead (Pb)-free)  
Si5447DC-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS $T_A = 25$ °C, unless otherwise noted				
Parameter	Symbol	5 s	Steady State	Unit
Drain-Source Voltage	$V_{DS}$	- 20		V
Gate-Source Voltage	$V_{GS}$	$\pm 8$		
Continuous Drain Current ( $T_J = 150$ °C) <sup>a</sup>	$I_D$	$T_A = 25$ °C	- 4.8	A
		$T_A = 85$ °C	- 3.5	
Pulsed Drain Current	$I_{DM}$	- 15		A
Continuous Source Current <sup>a</sup>	$I_S$	- 2.1	- 1.1	
Maximum Power Dissipation <sup>a</sup>	$P_D$	$T_A = 25$ °C	2.5	W
		$T_A = 85$ °C	1.3	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to 150		°C
Soldering Recommendations (Peak Temperature) <sup>b, c</sup>		260		

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient <sup>a</sup>	$t \leq 5$ s	$R_{thJA}$	43	50	°C/W
	Steady State		83	95	
Maximum Junction-to-Foot (Drain)	Steady State	$R_{thJF}$	14	20	

Notes:

a. Surface Mounted on 1" x 1" FR4 board.

b. See Reliability Manual for profile. The ChipFET is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

c. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

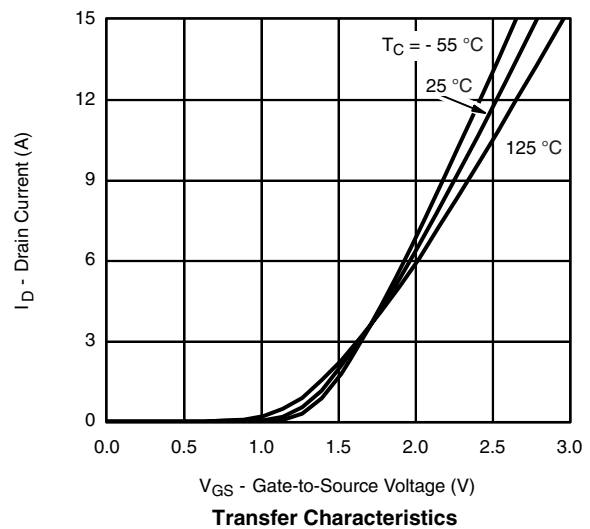
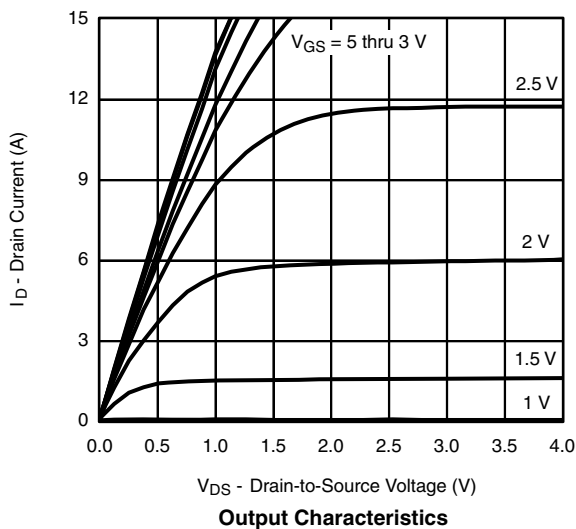
SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>Static</b>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	-0.45			V
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 8\text{ V}$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = -16\text{ V}, V_{GS} = 0\text{ V}$			-1	$\mu\text{A}$
		$V_{DS} = -16\text{ V}, V_{GS} = 0\text{ V}, T_J = 85\text{ }^\circ\text{C}$			-5	
On-State Drain Current <sup>a</sup>	$I_{D(on)}$	$V_{DS} \leq -5\text{ V}, V_{GS} = -4.5\text{ V}$	-15			A
Drain-Source On-State Resistance <sup>a</sup>	$R_{DS(on)}$	$V_{GS} = -4.5\text{ V}, I_D = -3.5\text{ A}$		0.064	0.076	$\Omega$
		$V_{GS} = -2.5\text{ V}, I_D = -2.9\text{ A}$		0.091	0.110	
		$V_{GS} = -1.8\text{ V}, I_D = -1\text{ A}$		0.130	0.160	
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = -10\text{ V}, I_D = -3.5\text{ A}$		9		S
Diode Forward Voltage <sup>a</sup>	$V_{SD}$	$I_S = -1.1\text{ A}, V_{GS} = 0\text{ V}$		-0.8	-1.2	V
<b>Dynamic<sup>b</sup></b>						
Total Gate Charge	$Q_g$	$V_{DS} = -10\text{ V}, V_{GS} = -4.5\text{ V}, I_D = -3.5\text{ A}$		6.5	10	nC
Gate-Source Charge	$Q_{gs}$		1.4			
Gate-Drain Charge	$Q_{gd}$		1.3			
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -10\text{ V}, R_L = 10\text{ }\Omega$ $I_D \cong -1\text{ A}, V_{GEN} = -4.5\text{ V}, R_G = 6\text{ }\Omega$		14	21	ns
Rise Time	$t_r$		29	45		
Turn-Off Delay Time	$t_{d(off)}$		42	65		
Fall Time	$t_f$		35	55		
Source-Drain Reverse Recovery Time	$t_{rr}$	$I_F = -1.1\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$		30	60	

Notes:

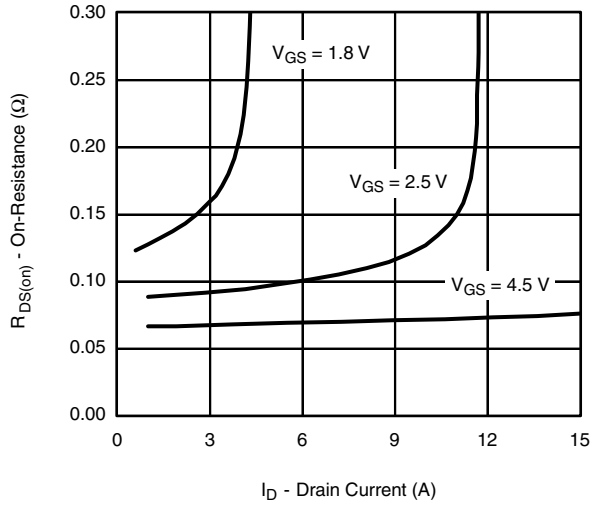
- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

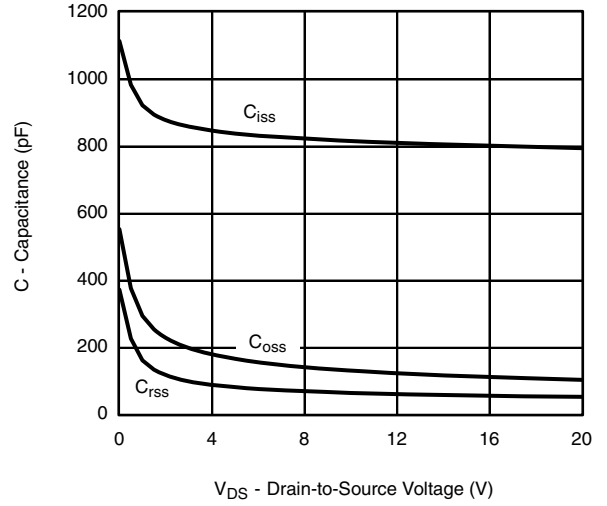
**TYPICAL CHARACTERISTICS**  $25\text{ }^\circ\text{C}$ , unless otherwise noted



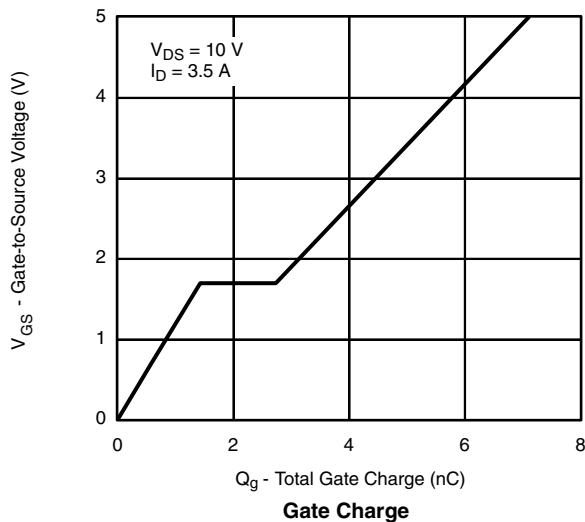
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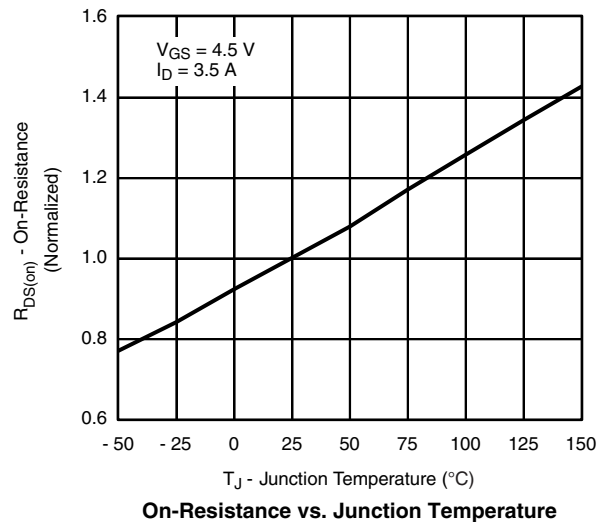
**On-Resistance vs. Drain Current**



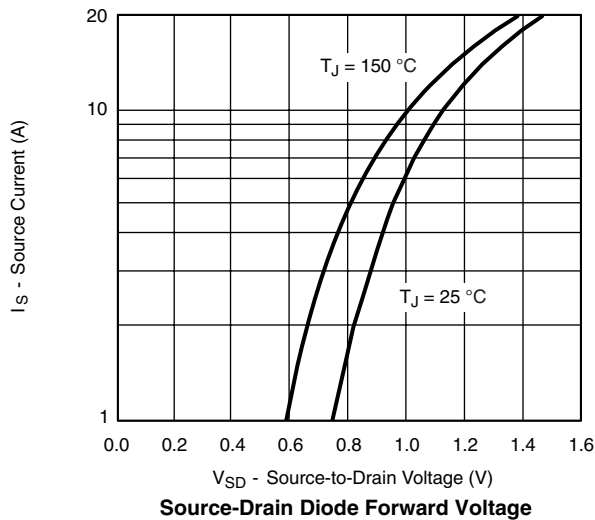
**Capacitance**



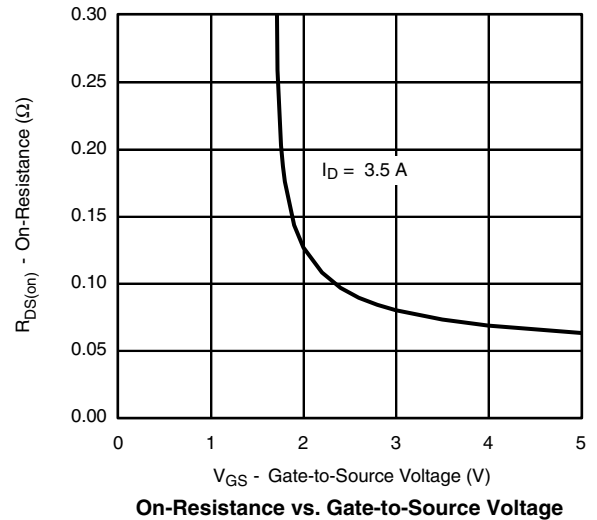
**Gate Charge**



**On-Resistance vs. Junction Temperature**

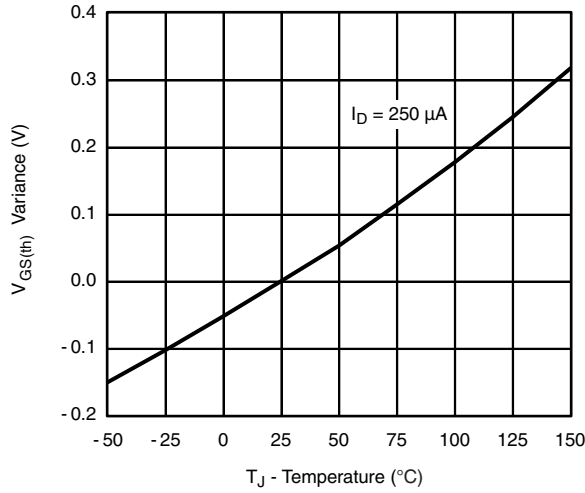


**Source-Drain Diode Forward Voltage**

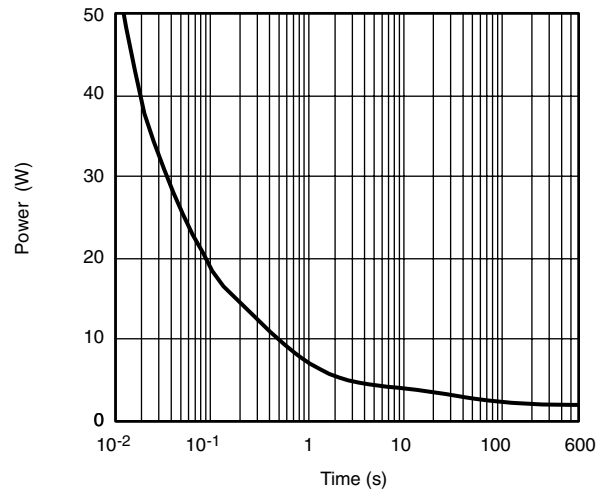


**On-Resistance vs. Gate-to-Source Voltage**

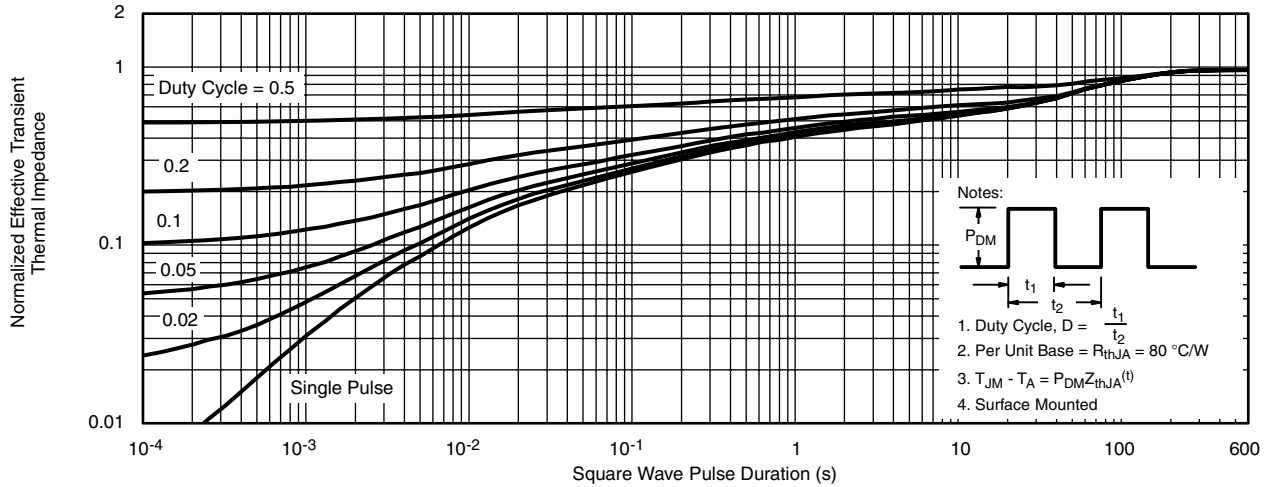
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



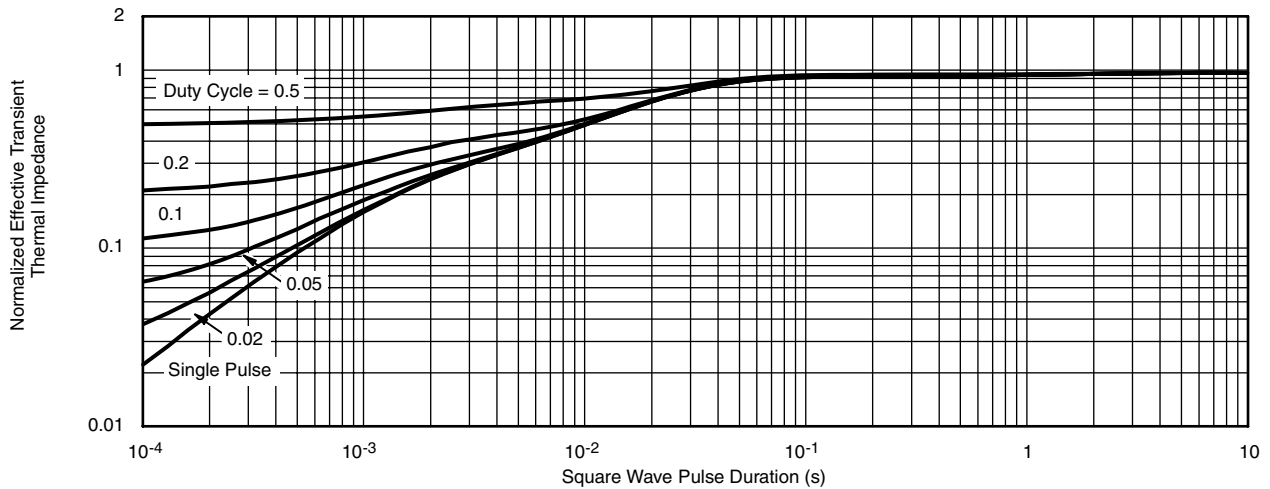
**Threshold Voltage**



**Single Pulse Power**



**Normalized Thermal Transient Impedance, Junction-to-Ambient**



**Normalized Thermal Transient Impedance, Junction-to-Foot**

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