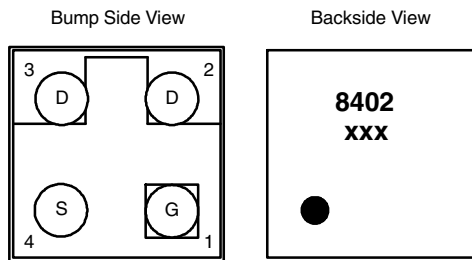


## 20 V N-Channel 1.8 V (G-S) MOSFET

PRODUCT SUMMARY		
V <sub>DS</sub> (V)	R <sub>DS(on)</sub> (Ω)	I <sub>D</sub> (A)
20	0.037 at V <sub>GS</sub> = 4.5 V	7.3
	0.039 at V <sub>GS</sub> = 2.5 V	7.1
	0.043 at V <sub>GS</sub> = 1.8 V	6.8

### MICRO FOOT



Device Marking: 8402  
xxx = Date/Lot Traceability Code

### FEATURES

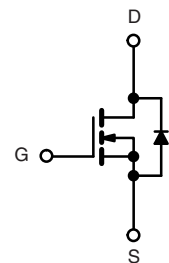
- TrenchFET<sup>®</sup> Power MOSFET
- MICRO FOOT<sup>®</sup> Chipscale Packaging  
Reduces Footprint Area Profile (0.62 mm) and On-Resistance Per Footprint Area
- Material categorization:  
For definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

### APPLICATIONS

- PA, Battery and Load Switch for Portable Devices



N-Channel MOSFET

Ordering Information: Si8402DB-T1-E1 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS (T <sub>A</sub> = 25 °C, unless otherwise noted)					
Parameter	Symbol	5 s	Steady State	Unit	
Drain-Source Voltage	V <sub>DS</sub>	20		V	
Gate-Source Voltage	V <sub>GS</sub>	± 8			
Continuous Drain Current (T <sub>J</sub> = 150 °C) <sup>a</sup>	I <sub>D</sub>	T <sub>A</sub> = 25 °C	7.3	5.3	A
		T <sub>A</sub> = 70 °C	5.9	4.3	
Pulsed Drain Current	I <sub>DM</sub>	30			
Continuous Source Current (Diode Conduction) <sup>a</sup>	I <sub>S</sub>	2.3	1.2	W	
Maximum Power Dissipation <sup>a</sup>	P <sub>D</sub>	T <sub>A</sub> = 25 °C	2.77		1.47
		T <sub>A</sub> = 70 °C	1.77		0.94
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150		°C	
Package Reflow Conditions <sup>b</sup>	IR/Convection	260			

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient <sup>a</sup>	R <sub>thJA</sub>	t ≤ 5 s	35	45	°C/W
		Steady State	72	85	
Maximum Junction-to-Foot (Drain)	R <sub>thJF</sub>	16	20		

Notes:

- a. Surface mounted on 1" x 1" FR4 board.  
b. Refer to IPC/JEDEC (J-STD-020), no manual or hand soldering.

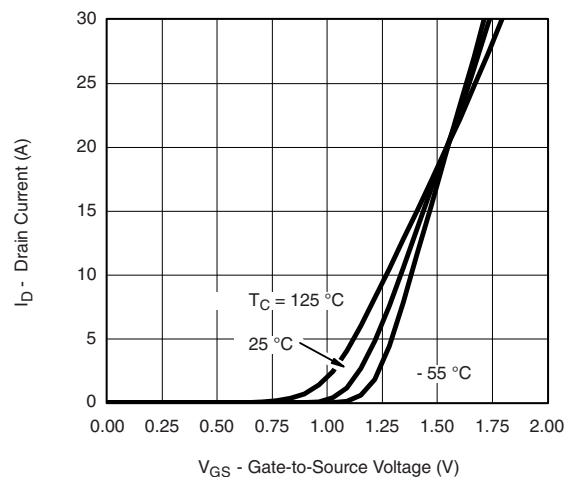
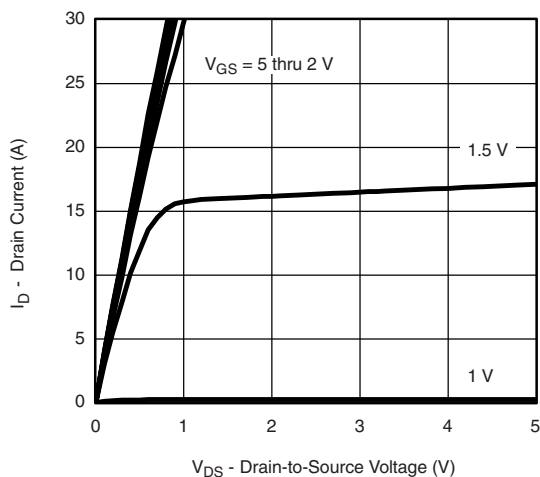
**SPECIFICATIONS** ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>Static</b>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	0.4		1	V
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0\ \text{V}, V_{GS} = \pm 8\ \text{V}$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 20\ \text{V}, V_{GS} = 0\ \text{V}$			1	$\mu\text{A}$
		$V_{DS} = 20\ \text{V}, V_{GS} = 0\ \text{V}, T_J = 70\text{ }^\circ\text{C}$			5	
On-State Drain Current <sup>a</sup>	$I_{D(on)}$	$V_{DS} \leq 5\ \text{V}, V_{GS} = 4.5\ \text{V}$	5			A
Drain-Source On-State Resistance <sup>a</sup>	$R_{DS(on)}$	$V_{GS} = 4.5\ \text{V}, I_D = 1\ \text{A}$		0.031	0.037	$\Omega$
		$V_{GS} = 2.5\ \text{V}, I_D = 1\ \text{A}$		0.033	0.039	
		$V_{GS} = 1.8\ \text{V}, I_D = 1\ \text{A}$		0.035	0.043	
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = 10\ \text{V}, I_D = 1\ \text{A}$		12		S
Diode Forward Voltage <sup>a</sup>	$V_{SD}$	$I_S = 1\ \text{A}, V_{GS} = 0\ \text{V}$		0.8	1.2	V
<b>Dynamic<sup>b</sup></b>						
Total Gate Charge	$Q_g$	$V_{DS} = 10\ \text{V}, V_{GS} = 4.5\ \text{V}, I_D = 1\ \text{A}$		17	26	nC
Gate-Source Charge	$Q_{gs}$			2		
Gate-Drain Charge	$Q_{gd}$			3.1		
Gate Resistance	$R_g$	$f = 1\ \text{MHz}$		15		$\Omega$
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 10\ \text{V}, R_L = 10\ \Omega$ $I_D \cong 1\ \text{A}, V_{GEN} = 4.5\ \text{V}, R_g = 6\ \Omega$		30	45	ns
Rise Time	$t_r$			45	70	
Turn-Off Delay Time	$t_{d(off)}$			145	220	
Fall Time	$t_f$			75	115	
Source-Drain Reverse Recovery Time	$t_{rr}$	$I_F = 1\ \text{A}, di/dt = 100\ \text{A}/\mu\text{s}$		30	60	

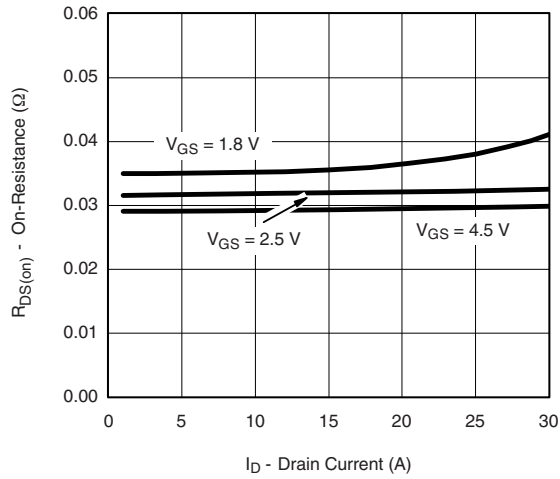
## Notes:

- a. Pulse test; pulse width  $\leq 300\ \mu\text{s}$ , duty cycle  $\leq 2\%$ .  
b. Guaranteed by design, not subject to production testing.

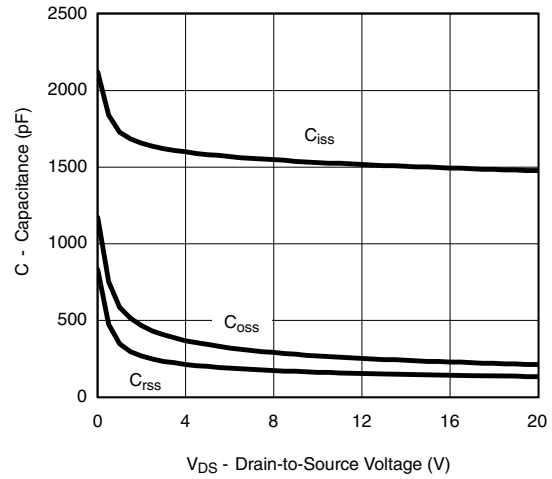
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**TYPICAL CHARACTERISTICS** ( $25\text{ }^\circ\text{C}$ , unless otherwise noted)

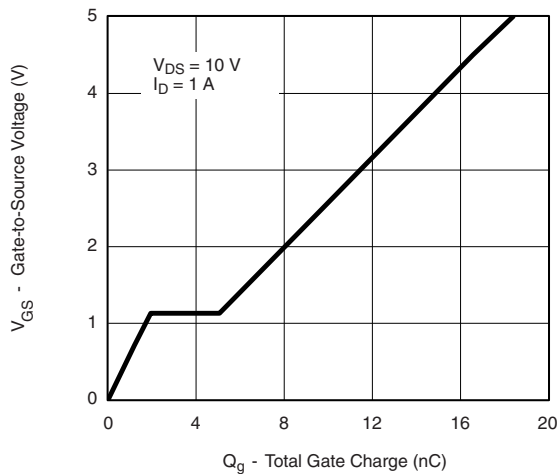
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



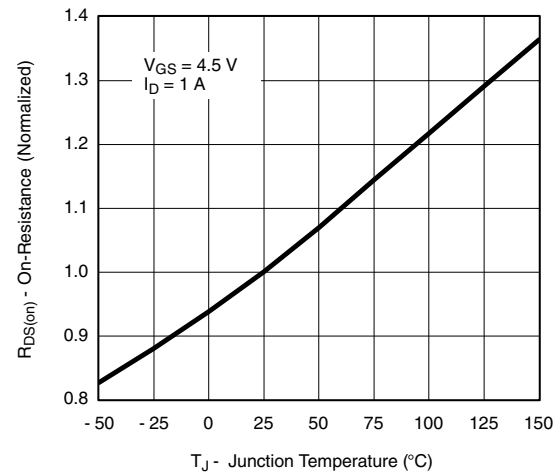
**On-Resistance vs. Drain Current**



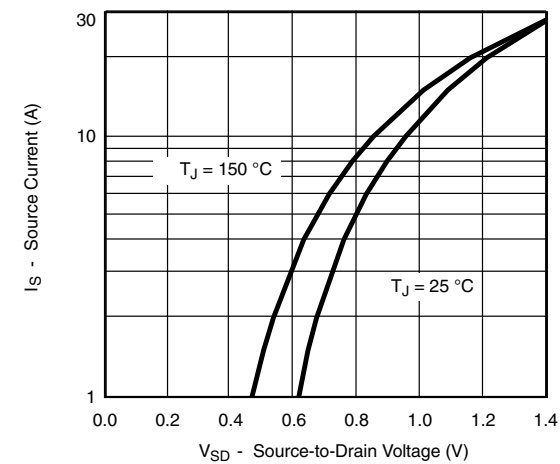
**Capacitance**



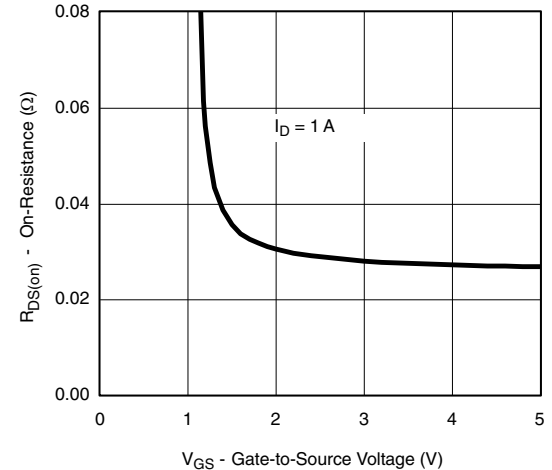
**Gate Charge**



**On-Resistance vs. Junction Temperature**

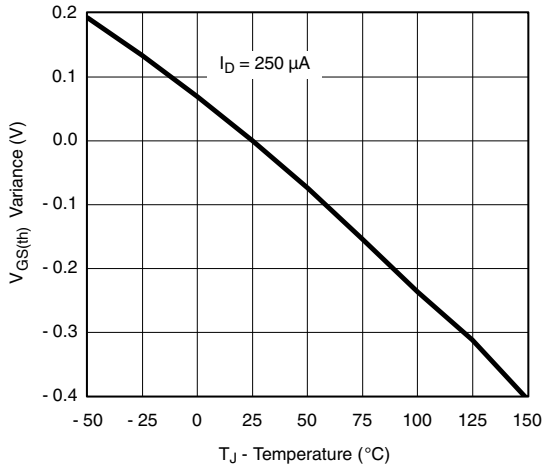


**Source-Drain Diode Forward Voltage**

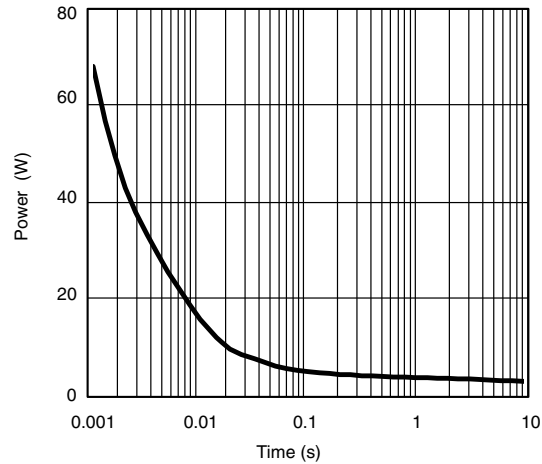


**On-Resistance vs. Gate-to-Source Voltage**

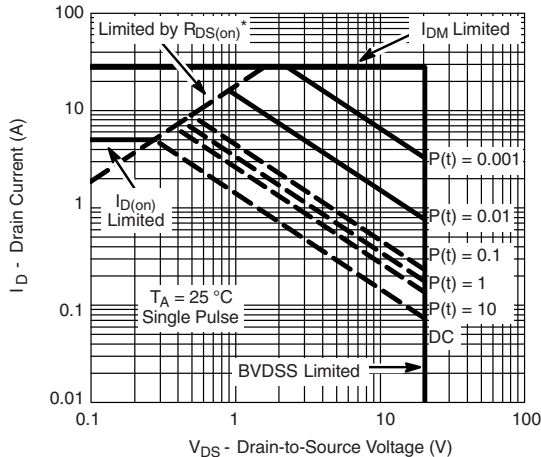
## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Threshold Voltage

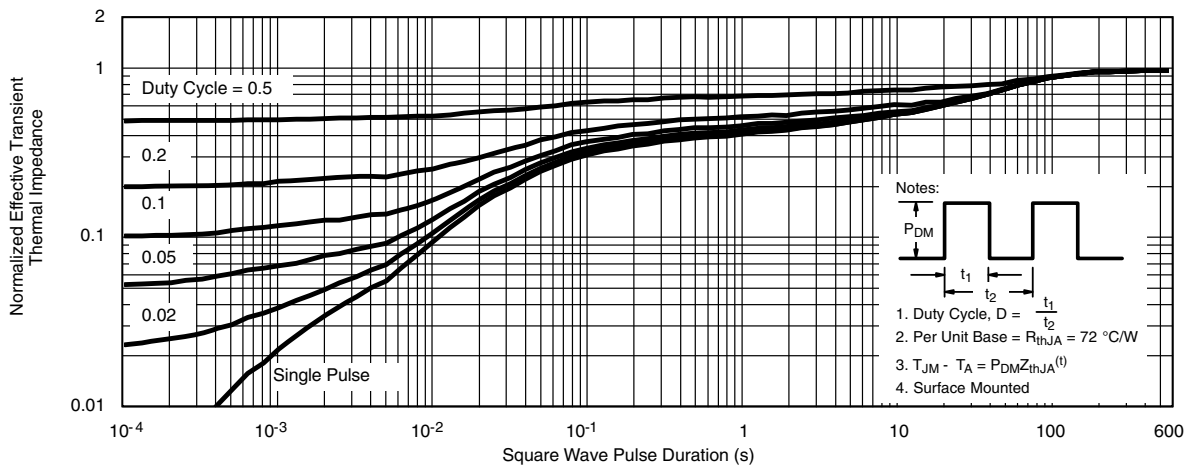


Single Pulse Power, Junction-to-Ambient



\*  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

Safe Operating Area

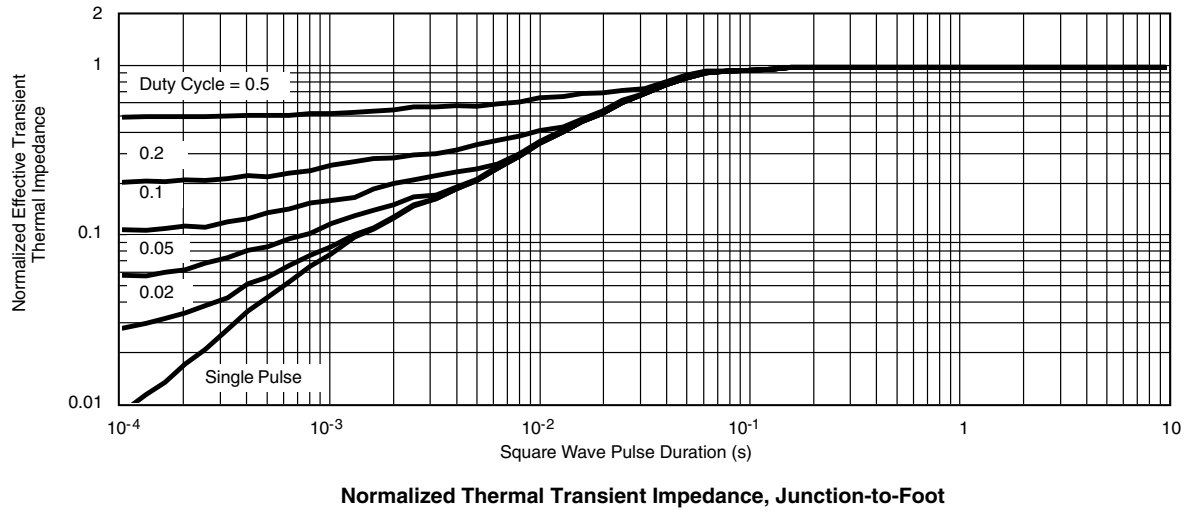


Notes:

1. Duty Cycle,  $D = \frac{t_1}{t_2}$
2. Per Unit Base =  $R_{thJA} = 72 \text{ }^\circ\text{C/W}$
3.  $T_{JM} - T_A = P_{DM} Z_{thJA}(t)$
4. Surface Mounted

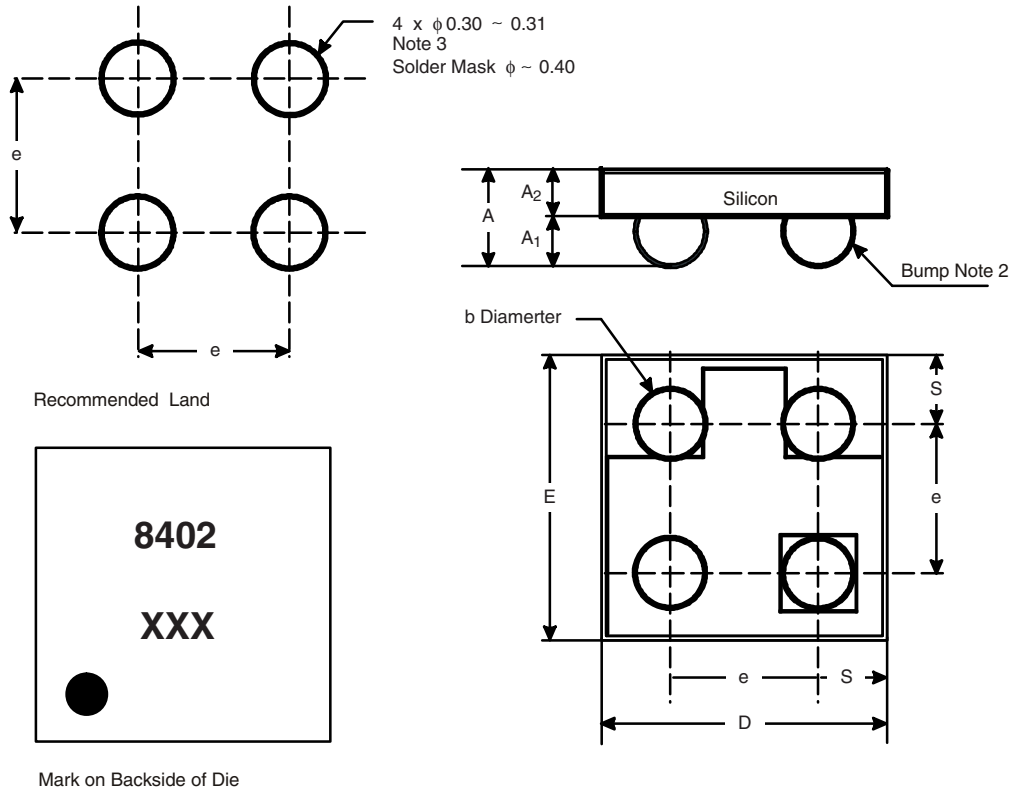
Normalized Thermal Transient Impedance, Junction-to-Ambient

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



## PACKAGE OUTLINE

### MICRO FOOT: 4-BUMP (0.8 mm PITCH)



Notes (Unless Otherwise Specified):

1. Laser mark on the silicon die back, coated with a thin metal.
2. Bumps are 95.5/3.8/0.7 Sn/Ag/Cu.
3. Non-solder mask defined copper landing pad.
4. The flat side of wafers is oriented at the bottom.

Dim.	Millimeters <sup>a</sup>		Inches	
	Min.	Max.	Min.	Max.
A	0.600	0.650	0.0236	0.0256
A <sub>1</sub>	0.260	0.290	0.0102	0.0114
A <sub>2</sub>	0.340	0.360	0.0134	0.0142
b	0.370	0.410	0.0146	0.0161
D	1.520	1.600	0.0598	0.0630
E	1.520	1.600	0.0598	0.0630
e	0.800		0.0315	
S	0.360	0.400	0.0142	0.0157

Notes:

- a. Use millimeters as the primary measurement.

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