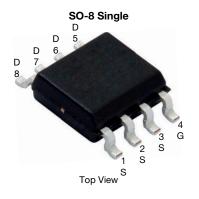
# SQ4483EY



Vishay Siliconix

# Automotive P-Channel 30 V (D-S) 175 °C MOSFET

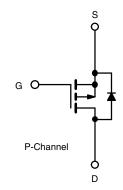
PRODUCT SUMMARY					
V <sub>DS</sub> (V)	-30				
$R_{DS(on)} (\Omega)$ at $V_{GS} = -10 V$	0.0085				
$R_{DS(on)} (\Omega)$ at $V_{GS} = -4.5 V$	0.0200				
I <sub>D</sub> (A)	-22				
Configuration	Single				
Package	SO-8				



#### **FEATURES**

- TrenchFET<sup>®</sup> power MOSFET
- AEC-Q101 qualified <sup>c</sup>
- 100 %  $R_q$  and UIS tested
- Material categorization: for definitions of compliance please see <u>www.vishay.com/doc?99912</u>





<b>ABSOLUTE MAXIMUM RATINGS</b> (T <sub>C</sub> = 25 °C, unless otherwise noted)					
PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-Source Voltage		V <sub>DS</sub>	-30	V	
Gate-Source Voltage		V <sub>GS</sub>	± 20		
Continuous Drain Current	T <sub>C</sub> = 25 °C	I-	-30		
Continuous Drain Current	T <sub>C</sub> = 125 °C	I <sub>D</sub>	-30		
Continuous Source Current (Diode Conduction)		I <sub>S</sub>	-30	А	
Pulsed Drain Current <sup>a</sup>		I <sub>DM</sub>	-84		
Single Pulse Avalanche Current	L = 0.1 mH	I <sub>AS</sub>	-32		
Single Pulse Avalanche Energy	L = 0.1 min	E <sub>AS</sub>	51	mJ	
Maximum Power Dissipation <sup>a</sup>	T <sub>C</sub> = 25 °C	PD	7	W	
	T <sub>C</sub> = 125 °C	гр	2	۷V	
Operating Junction and Storage Temperature Ra	nge	T <sub>J</sub> , T <sub>stg</sub>	-55 to +175	°C	

THERMAL RESISTANCE RATINGS						
PARAMETER		SYMBOL	LIMIT	UNIT		
Junction-to-Ambient	PCB Mount <sup>b</sup>	R <sub>thJA</sub>	85	°C/W		
Junction-to-Foot (Drain)		R <sub>thJF</sub>	21	0/10		

#### Notes

- a. Pulse test; pulse width  $\leq 300~\mu s,~duty~cycle \leq 2~\%.$
- b. When mounted on 1" square PCB (FR4 material).

c. Parametric verification ongoing.

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PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static	•	-					
Drain-Source Breakdown Voltage	V <sub>DS</sub>	$V_{GS} = 0 V, I_D = -250 \mu A$		-30	-	-	v
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =	$V_{DS} = V_{GS}$ , $I_D = -250 \ \mu A$		-2.0	-2.5	v
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>DS</sub> =	$V_{DS} = 0 V, V_{GS} = \pm 20 V$		-	± 100	nA
		$V_{GS} = 0 V$	V <sub>DS</sub> = -30 V	-	-	-1	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	$V_{GS} = 0 V$	$V_{DS}=-30~V,~T_J=125~^\circ C$	-	-	-50	μA
		$V_{GS} = 0 V$	$V_{DS}$ = -30 V, $T_{J}$ = 175 °C	-	-	-150	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{GS}$ = -10 V	$V_{DS} \le -5 V$	-30	-	-	Α
		$V_{GS} = -10 V$	I <sub>D</sub> = -10 A	-	0.0070	0.0085	Ω
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	$V_{GS} = -10 V$	I <sub>D</sub> = -10 A, T <sub>J</sub> = 125 °C	-	-	0.0130	
Drain-Source On-State Resistance	· •D3(01)	$V_{GS} = -10 V$	I <sub>D</sub> = -10 A, T <sub>J</sub> = 175 °C	-	-	0.0150	
		$V_{GS} = -4.5 V$	I <sub>D</sub> = -7 A	-	0.0160	160 0.0200	
Forward Transconductance b	9 <sub>fs</sub>	$V_{DS} = -10 \text{ V}, \text{ I}_{D} = -10 \text{ A}$		-	32	-	S
Dynamic <sup>b</sup>							
Input Capacitance	C <sub>iss</sub>		V <sub>GS</sub> = 0 V V <sub>DS</sub> = -15 V, f = 1 MHz	-	3400	4500	
Output Capacitance	C <sub>oss</sub>	$V_{GS} = 0 V$		-	712	890	pF
Reverse Transfer Capacitance	C <sub>rss</sub>			-	580	770	
Total Gate Charge <sup>c</sup>	Qg			-	75	113	
Gate-Source Charge <sup>c</sup>	Q <sub>gs</sub>	V <sub>GS</sub> = -10 V	V <sub>DS</sub> = -15 V, I <sub>D</sub> = -10 A	-	9.5	-	nC
Gate-Drain Charge <sup>c</sup>	Q <sub>gd</sub>			-	19	-	
Gate Resistance	R <sub>q</sub>		f = 1 MHz	1	2	3	Ω
Turn-On Delay Time <sup>c</sup>	t <sub>d(on)</sub>			-	20	25	
Rise Time <sup>c</sup>	tr	$V_{DD} = -15 \text{ V}, \text{ R}_{\text{L}} = 1.5 \Omega$ $\text{I}_{\text{D}} \cong -10 \text{ A}, \text{ V}_{\text{GEN}} = -10 \text{ V}, \text{ R}_{\text{g}} = 1 \Omega$		-	146	189	ns
Turn-Off Delay Time c	t <sub>d(off)</sub>			-	57	75	
Fall Time <sup>c</sup>	t <sub>f</sub>			-	20	25	1
Source-Drain Diode Ratings and Char							1
Pulsed Current <sup>a</sup>	I <sub>SM</sub>			-	-	-84	А
	V <sub>SD</sub>	$I_{\rm F} = -3$ A, $V_{\rm GS} = 0$ V		-	-0.75	-1.2	v

Notes

a. Pulse test; pulse width  $\leq$  300 µs, duty cycle  $\leq$  2 %.

b. Guaranteed by design, not subject to production testing.

c. Independent of operating temperature.

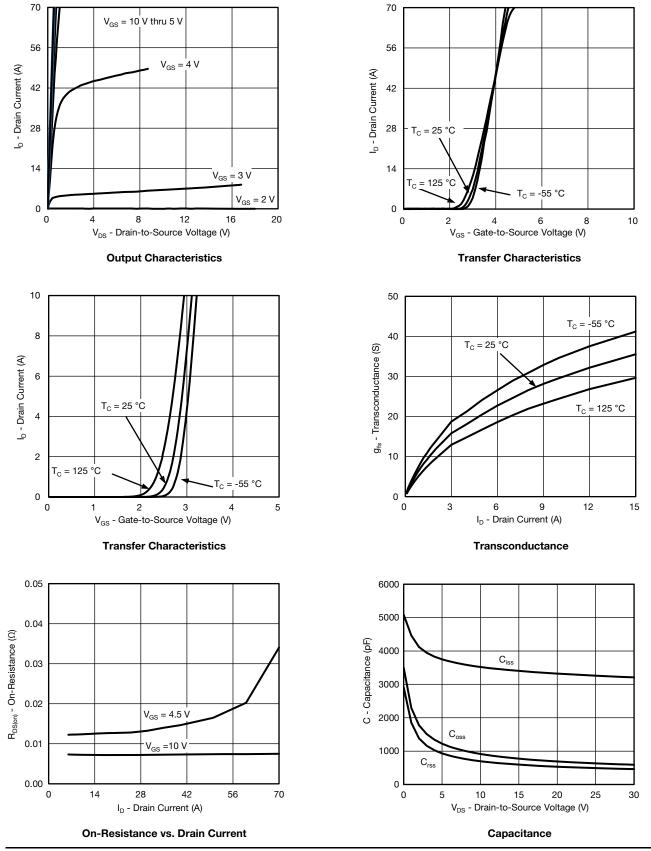
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



S15-1806-Rev. A, 10-Aug-15

Document Number: 74794

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<sup>3</sup> 

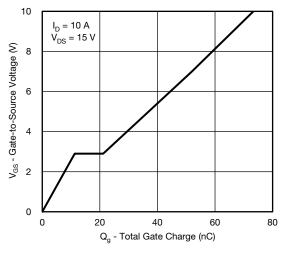
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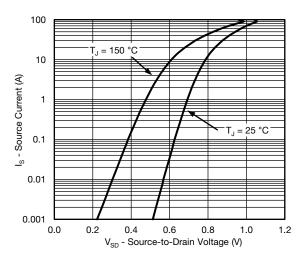
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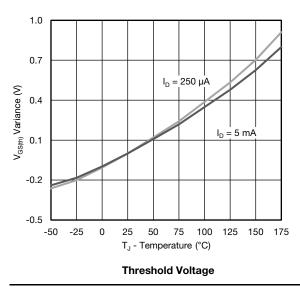
## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

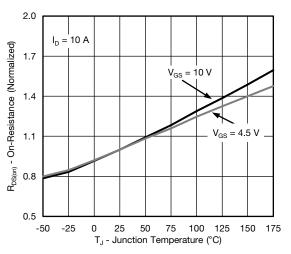


Gate Charge

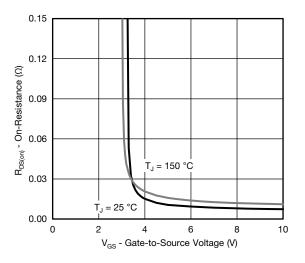


Source Drain Diode Forward Voltage

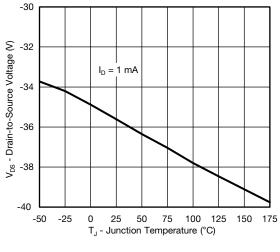




**On-Resistance vs. Junction Temperature** 



**On-Resistance vs. Gate-to-Source Voltage** 



Drain Source Breakdown vs. Junction Temperature

S15-1806-Rev. A, 10-Aug-15

4

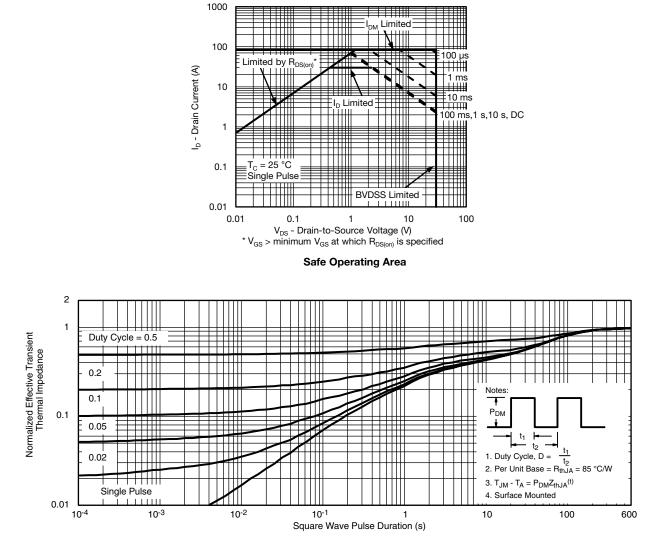
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#### **THERMAL RATINGS** ( $T_A = 25 \text{ °C}$ , unless otherwise noted)



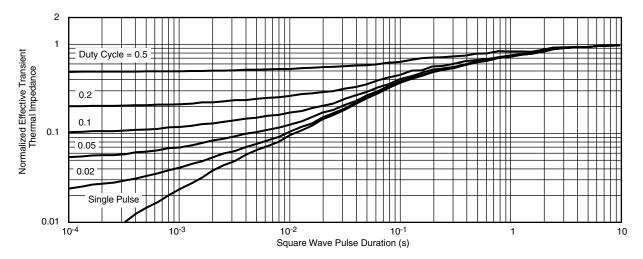
Normalized Thermal Transient Impedance, Junction-to-Ambient



# SQ4483EY

## Vishay Siliconix

## **THERMAL RATINGS** ( $T_A = 25 \text{ °C}$ , unless otherwise noted)



#### Normalized Thermal Transient Impedance, Junction-to-Foot

#### Note

· The characteristics shown in the two graphs

- Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)

- Normalized Transient Thermal Impedance Junction-to-Foot (25 °C)

are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

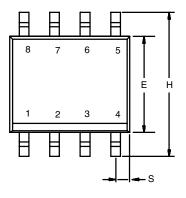
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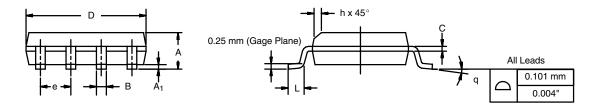


# Package Information

Vishay Siliconix

# SOIC (NARROW): 8-LEAD JEDEC Part Number: MS-012





	MILLIMETERS		INCHES		
DIM	Min	Мах	Min	Max	
A	1.35	1.75	0.053	0.069	
A <sub>1</sub>	0.10	0.20	0.004	0.008	
В	0.35	0.51	0.014	0.020	
С	0.19	0.25	0.0075	0.010	
D	4.80	5.00	0.189	0.196	
E	3.80	4.00	0.150	0.157	
е	1.27	BSC	0.050 BSC		
н	5.80	6.20	0.228	0.244	
h	0.25	0.50	0.010	0.020	
L	0.50	0.93	0.020	0.037	
q	0°	8°	0°	8°	
S	0.44	0.64	0.018	0.026	
ECN: C-06527-Rev. I, 11-Sep-06 DWG: 5498					

# **Application Note 826**

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**RECOMMENDED MINIMUM PADS FOR SO-8** 



Recommended Minimum Pads Dimensions in Inches/(mm)

Return to Index



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